Syntacore™
Custom cores and tools

Syntacore open-source and commercial RISC-V solutions

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Executive director

Outline

- Company intro
- RISC-V compatible IP
- Customization services
- Evaluation

Syntacore introduction

Semiconductor IP company, founding member of RISC-V foundation

Develops and licenses state-of-the-art RISC-V cores

- Immediately available, silicon-proven and ships in volume
- 7+ years of focused RISC-V experience
- Core team comes from 10+ years of highly-relevant background
- SDKs, samples in silicon, full collateral

Turnkey service to specialize CPU IP for customer requirements

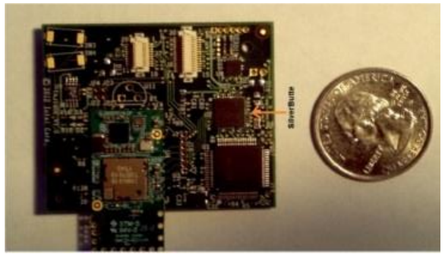
- One-stop workload-specific customization for 10x improvements
  - with tools/compiler support
- IP hardening at the required library node
- SoC integration and SW migration support

Company background

Est 2015 , ~100 EE

HQ in EU (Cyprus)

- R&D offices in St. Petersburg, Moscow, Russia
- Full-time staff and representatives in APAC, EMEA, US

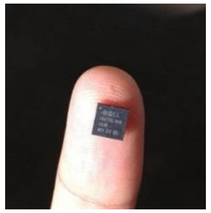


Team background:

- 10+ years in the corporate R&D (major semi MNC)
- Developed cores and SoC are in the mass productions

Expertise:

- High-performance and low-power embedded cores and IP
- ASIP technologies and reconfigurable architectures
- Architectural exploration & workload characterization
- Compiler technologies



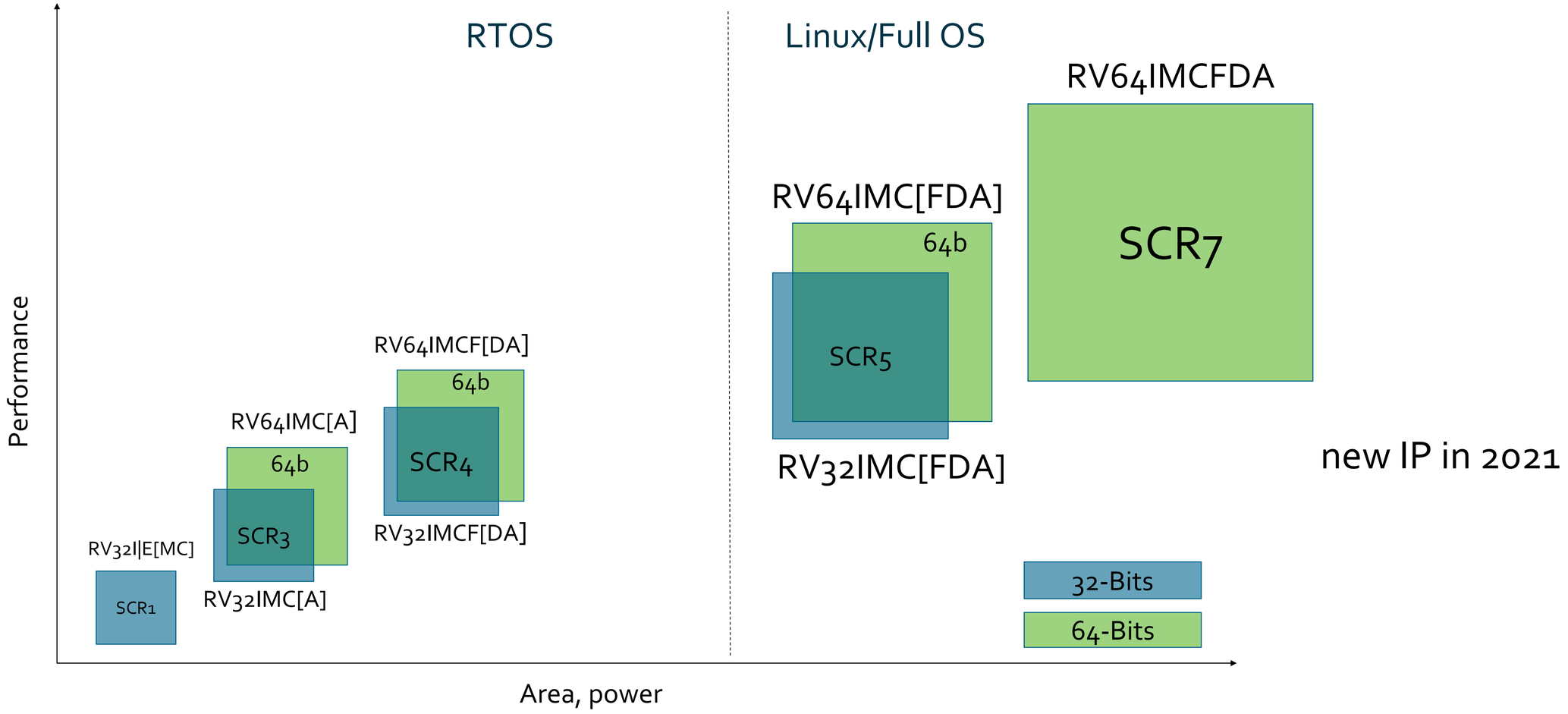
Some current results

- State-of-the-art RISC-V CPU IP line with competitive features
  - ✓ commercially deployed in SoCs up to 5nm
  - ✓ first RISC-V client silicon in 2016, first RISC-V Linux-capable IP in 2016, in full-wafer from 2017

- MPWs and full-wafer production at the clients. Projects examples:
  - ✓ 56-cores heterogeneous SoC @7nm (64bit heterogeneous, NuMA, sophisticated system-level customization)
  - ✓ active battery-less SoC @22nm (SCR1, power-optimization, clock/power domains, ntv-ready)

- Customers in APAC, EMEA, US
  - ✓ References available

Current product line



State-of-the art RISC-V CPU IP

Features			RTOS/ Bare Metal			Linux/ "Full" OS	
			SCR1* (FREE!)	SCR3	SCR4	SCR5	SCR7
Width		32bit	●	●	●	●	
		64bit		●	●	●	●
ISA			RV32I|E[MC]	RV[32|64]IMC[A]	RV[32|64]IMCF[AD]	RV[32|64]IMC[AFD]	RV64IMCAFD
Pipeline type			In-order	In-order	In-order	In-order	Superscalar
Pipeline, stages			2-4	3-5	3-5	7-9	10-12
Branch prediction				Static BP, RAS	Static BP, RAS	Static BP, BTB, BHT, RAS	Dynamic BP, BTB, BHT, RAS
Execution priority levels			Machine	User, Machine	User, Machine	User, Supervisor, Machine	User, Supervisor, Machine
Extensibility/customization			●	●	●	●	●
Execution units	MUL/DIV	area-opt	●	○	○		
		hi-perf	○	●	●	●	●
	FPU				●	●	●
Memory subsystem	TCM [w/ECC|parity]		○	○	○	○	○
	L1$ [w/ECC|parity]			○	○	●	●
	L2$ [w/ECC]					○	○
	MPU			●	●	●	●
	MMU, virtual memory					●	●
Debug	Integrated JTAG debug		●	●	●	●	●
	HW BP		1-2	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl	1-8 adv ctrl
	Performance counters		○	○	○	○	○
Interrupt Controller	IRQs		8-32	8-1024	8-1024	8-1024	8-1024
	Features		basic	advanced	advanced	advanced+	advanced+
SMP support				up to 4 cores with coherency			up to 8-16 cores
I/F options	AHB		●	○	○	○	
	AXI4		○	●	●	●	●
	ACE						○

* Download SCR1 free at www.github.com/syntacore/scr1

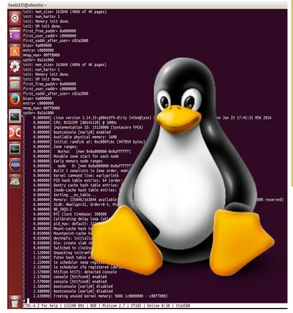
Baseline cores:

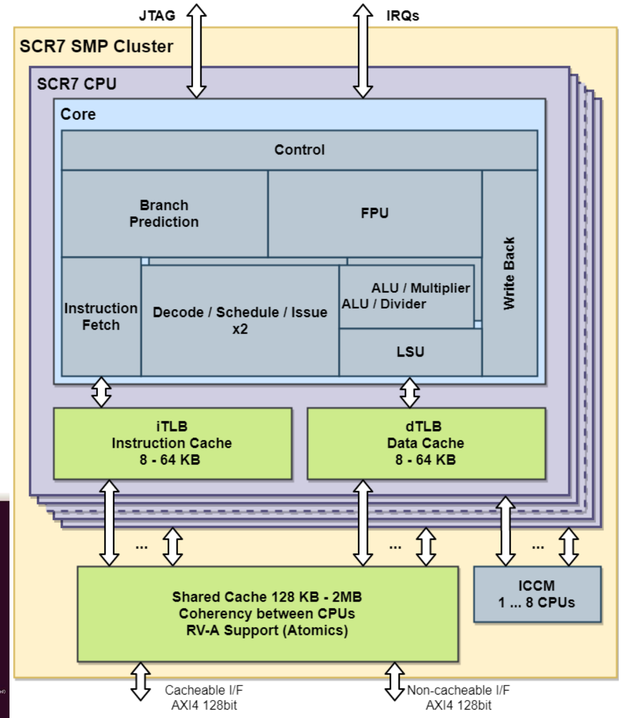
- Clean-slate designs in System Verilog
- Configurable and extensible
- 100% compatible with major EDA flows

RV64 SCR7

Efficient mid-range application core

- RV64GC ISA
- SMP up to 8, later 16 cores
- Flexible uarch template, 10-12 stage pipeline
- Stable SCR7 in production:
  - Decode and dispatch up to two instructions per cycle
  - Out-of-order issue of up to four micro-ops
  - Out-of-order completion, in-order retirement
- M-, S- and U-modes
- Virtual memory support, full MMU, Linux
- 16-64KB L1, up to 2MB L2 cache with ECC
- 1.5 GHz+ @28nm
- Advanced debug with JTAG i/f



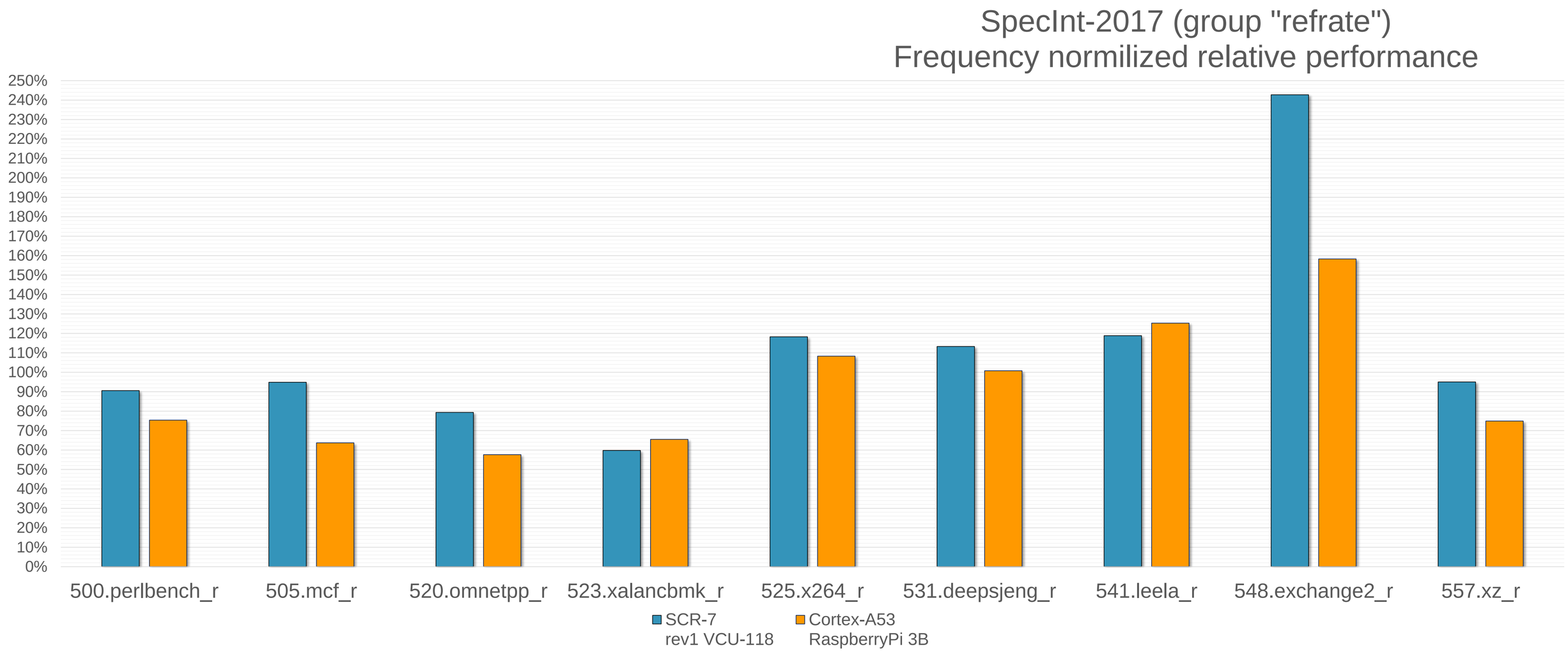


Performance*, per MHz	DMIPS	-O2	3.25
		-best**	3.80
	Coremark	-best**	5.12

* Preliminary data, 2-way implementation, Dhrystone 2.1, Coremark 1.0, GCC 8.1 BM
** O3-funroll-loops -fpeel-loops -fgcse-sm -fgcse-las -flto

SCR7 SpecInt 2017

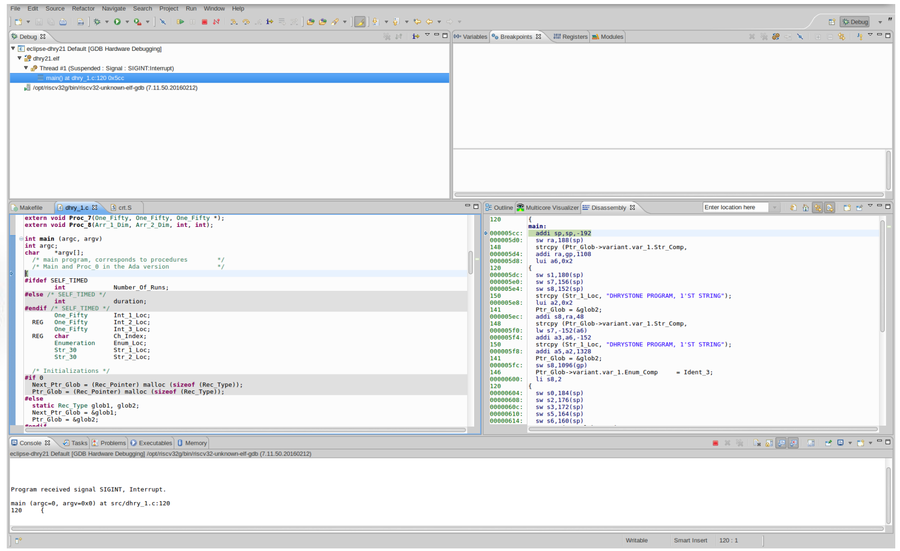
- Geomean +19.83% vs cortex a-53



SCR7 FPGA-based SDK

Fully-integrated system based on the off-the-shelf Xilinx VCU118 dev.kit:
https://www.xilinx.com/products/boards-and-kits/vcu118.html

- Quad-core, 4GB RAM, up to 100-150 MHz, 1GB Ethernet, storage
- Boots upstream Linux kernel 4.19 (5.15 soon), Debian
- Integrated toolchain with IDE (supports Linux targets debug)
  - Windows: https://yadi.sk/d/S1Ub16jKX2xLwQ
  - Linux: https://yadi.sk/d/8ZsMgUx381GKiw

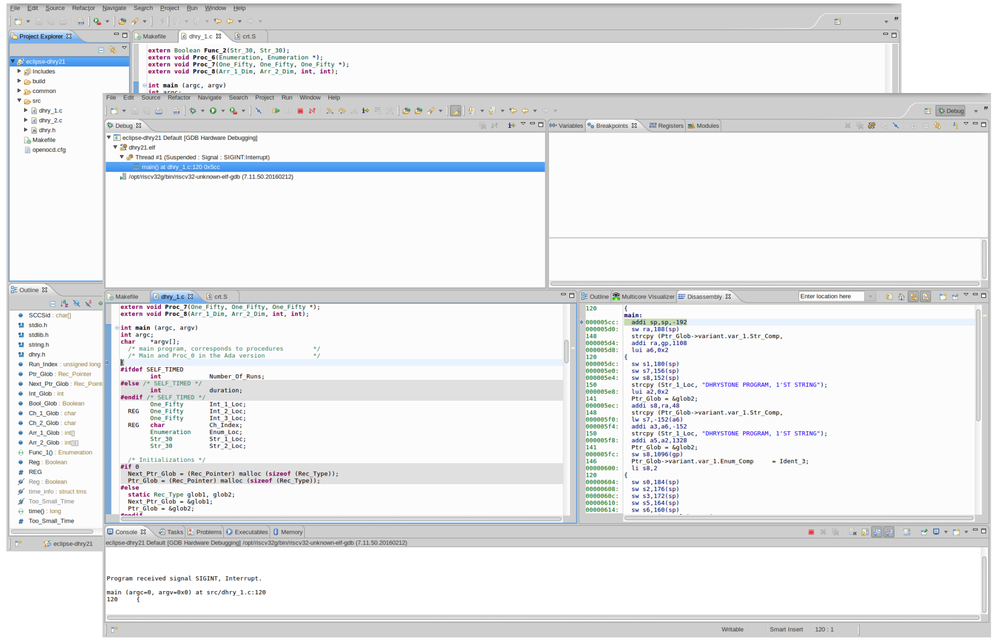


HTG-960 based (VU19P) dev.kit:
http://www.hitechglobal.com/Boards/VirtexUltraScale+_VU19P_Board.htm

Fully featured SW development suite

Stable IDE in production:

- GCC 10.2
- GNU Binutils 2.31.0
- Newlib 3.0
- GNU GDB 8.0.50
- Open On-Chip Debugger 0.10.0
- Eclipse 4.9.0



Hosts: Linux, Windows
Targets: BM, Linux

Also available:

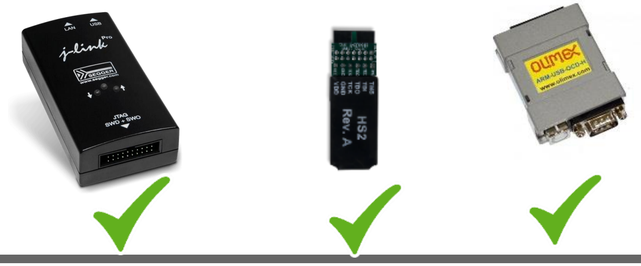
- LLVM 5.0
- CompCert 3.1
- 3rd party vendors

Simulators:

- Qemu
- Spike
- 3rd party vendors

JTAG-based debug solutions:

Supports: Segger J-link, Olimex ARM-USB-OCD family, Digilink JTAG-HS2, more vendors soon



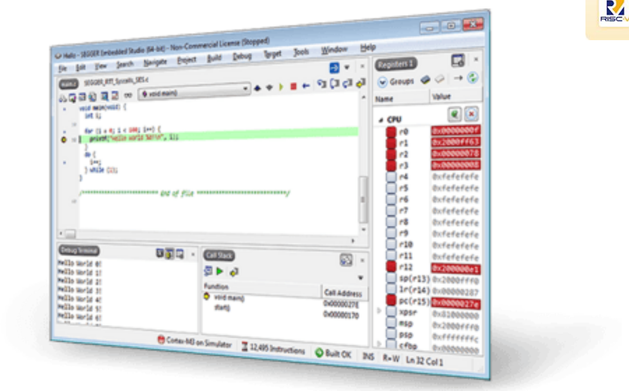
Wide support by 3rd party tools and SW vendors

- Lauterbach Trace32

https://www.lauterbach.com/frames.html?pro/pro__syntacore.html

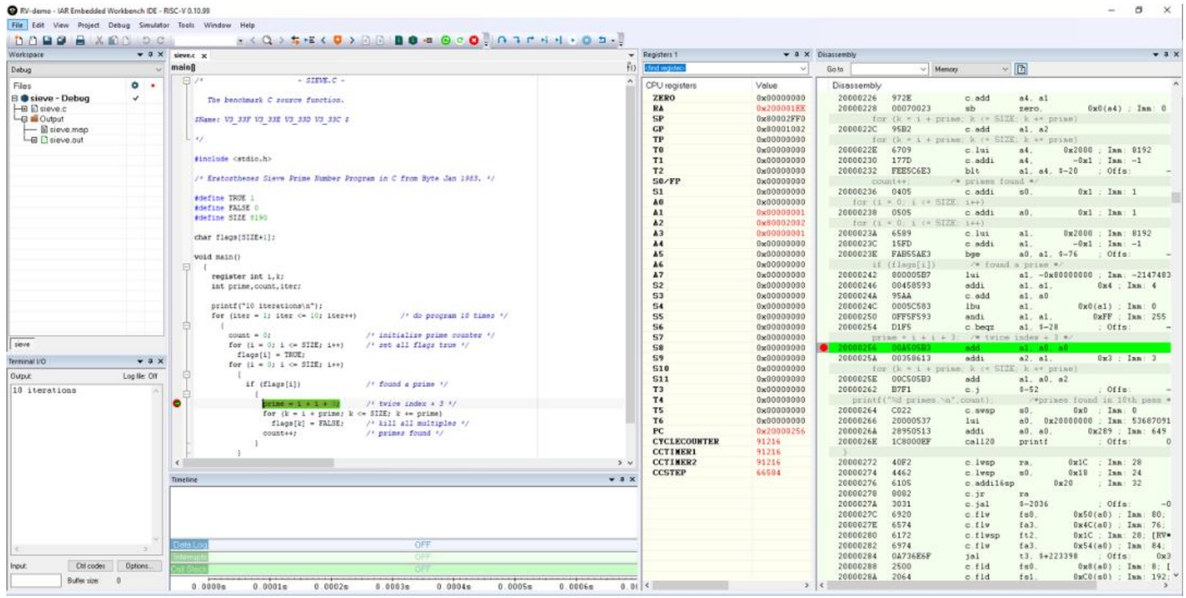
- Segger Embedded Studio

https://wiki.segger.com/Syntacore_SCR1_SDK_Arty



- IAR Embedded Workbench

https://www.iar.com/iar-embedded-workbench/#!?architecture=RISC-V



IP collateral (what is included)

Standard core package (SCR7)

- RISC-V compatible core
  - RV64GC ISA
  - RTL (encrypted for evaluation stage), suitable for simulation and synthesis
  - Netlist for the required FPGA devices (Xilinx/Altera)
- Simulation and verification environment
  - Testbench, Integration verification environment
  - Architectural and compliance tests suites (pre- and post-si)
- Synthesis support harness
  - sample scripts, SDC/timing constraints for the required flow
- Reference instantiation examples
- Back-end support @ required process node (PDK access to be provided)
  - Full cycle: synthesis, floor-planning, netlist verification, PaR/CTS/timing closure, DRC, FEV, DFT)
- Support for 1 tapeout up to a year is included

Tools (pre-built & sources)

- GCC based toolchain
  - complier, debugger, linker, functional simulator, binutils, newlib, openocd
- Eclipse-based IDE (Linux, Windows)

FPGA-based SDK

- Sample FPGA project (open design)
- pre-build FPGA and SW images

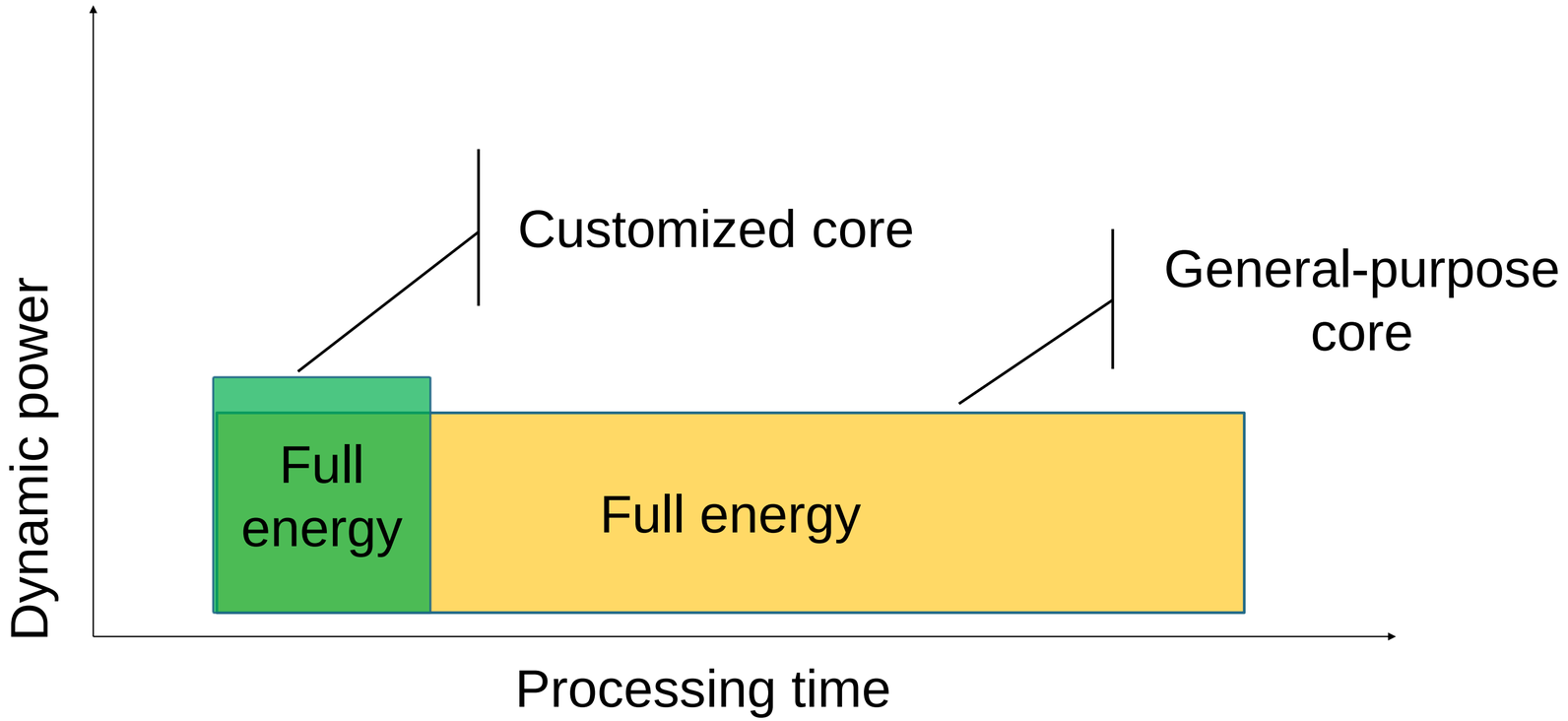
SW:

- First stage bootloader (SC-BL)
- Linux for the SDK board, including BSP
- Tests/application samples

Documentation

- SCRx quick-start guide (user manual)
- SCRx EAS (External architecture specification)
- SCRx ISM (Instruction set manual)
- SCRx SDK guide
- Integration verification environment guide
- Tools guide (IDE & CLI)

Extensibility/customization: how it works



Workload-specific customization

Extensibility features:

- Computational capabilities
  - New functions using existing HW
  - New Functional Units
- Extended storage
  - Mems/RF, addressable or state
  - Custom AGU
- I/O ports
- Specialized system behavior
  - Standard events processing
  - Custom events

Domain examples:

- Computationally intensive algorithms acceleration
- Specialized processors (including DSP)
- High-throughput applications
  - CV/ML/AI
  - Wireless/Comms
  - Network/DPI/real-time processing

SCRx extensibility example

Custom ISA extension for AES & other crypto kernels acceleration for SCR5

- Data
  - RV32G – FPGA-based devkit, g++ 5.2.0, Linux 4.6, optimized C++ implementation
  - Rv32G + custom – same + intrinsics
  - Core i7 6800K @ 3.4GHz, g++ 5.4.0, Linux 64, optimized C++ implementation
- 60..575x speedup @ modest area increase: 11.7% core, 3.7% at the CPU cluster level

Details in paper @EW2018 conference

Platform	Fmax, MHz	Encoding throughput, MB/s			Normalized per MHz, MB/s			RV32G + custom speed-up		
		Crypto-1	Crypto-2	AES-128	Crypto-1	Crypto-2	AES-128			
RV32G	20	0.025	0.129	0.238	0.00125	0.00645	0.0119	575.00	117.74	60.93
RV32G + custom	20	14.375	15.188	14.502	0.71875	0.7594	0.7251			
Core i7	3400	79.115	235.343	335.212	0.02327	0.06922	0.09859	30.89	10.97	7.35
Core i7 + NI	3400			3874.552			1.13957			0.64

Disclaimer: Authors are aware AES allows for more efficient dedicated accelerators designs, used as example algorithm

Getting access/evaluation

SCR1

- Is fully open: https://github.com/syntacore/scr1 and https://github.com/syntacore/scr1-sdk
- SHL-licensed with unrestricted commercial use allowed
  - Commercial SLA-based support is available

SCR 3|4|5|7

- Full package* access is available after simple evaluation agreement

For more info: evaluation@syntacore.com

(*) sufficient for evaluation and tapeout

Summary

Syntacore offers high-quality RISC-V compatible CPU IP

- Founding member, fully focused on RISC-V since 2015
- Silicon-proven and shipping in full-wafer production
- Turnkey IP customization services
  - with full tools/compiler support