RISC-V®

Open Era of Computing

January 2022

Calista Redmond
CEO, RISC-V International

Open source and collaboration
are strategic to software and hardware
across industries and geographies.

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RISC-V is the free and open Instruction Set Architecture

- Open collaboration
- Design freedom
- Strategic future

RISC-V is critical to compete in the Open Era of Computing

Disruptive **Technology**

Barriers	**Legacy ISA**	**RISC-V ISA**
Complexity	1500+ base instructions Incremental ISA	47 base instructions Modular ISA
Design freedom	$$$ – Limited	Free – Unlimited
License and Royalty fees	$$$	Free
Design ecosystem	Moderate	Growing rapidly. Numerous extensions and cores. More design companies on RISC-V than any other architecture
Software ecosystem	Extensive	Growing rapidly. Easy to compile for RISC-V

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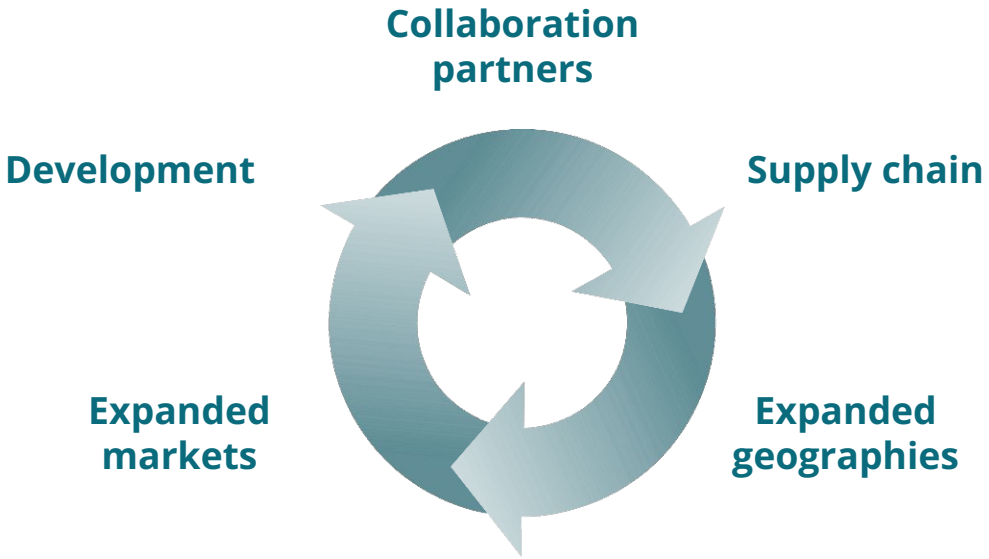
Unconstrained **Opportunity**

Barriers removed

- Design risk
- Cost of entry
- Partner limitations
- Supply chain

RISC-V Business Model



Beyond removing barriers, RISC-V fuels our community to seize growing opportunities

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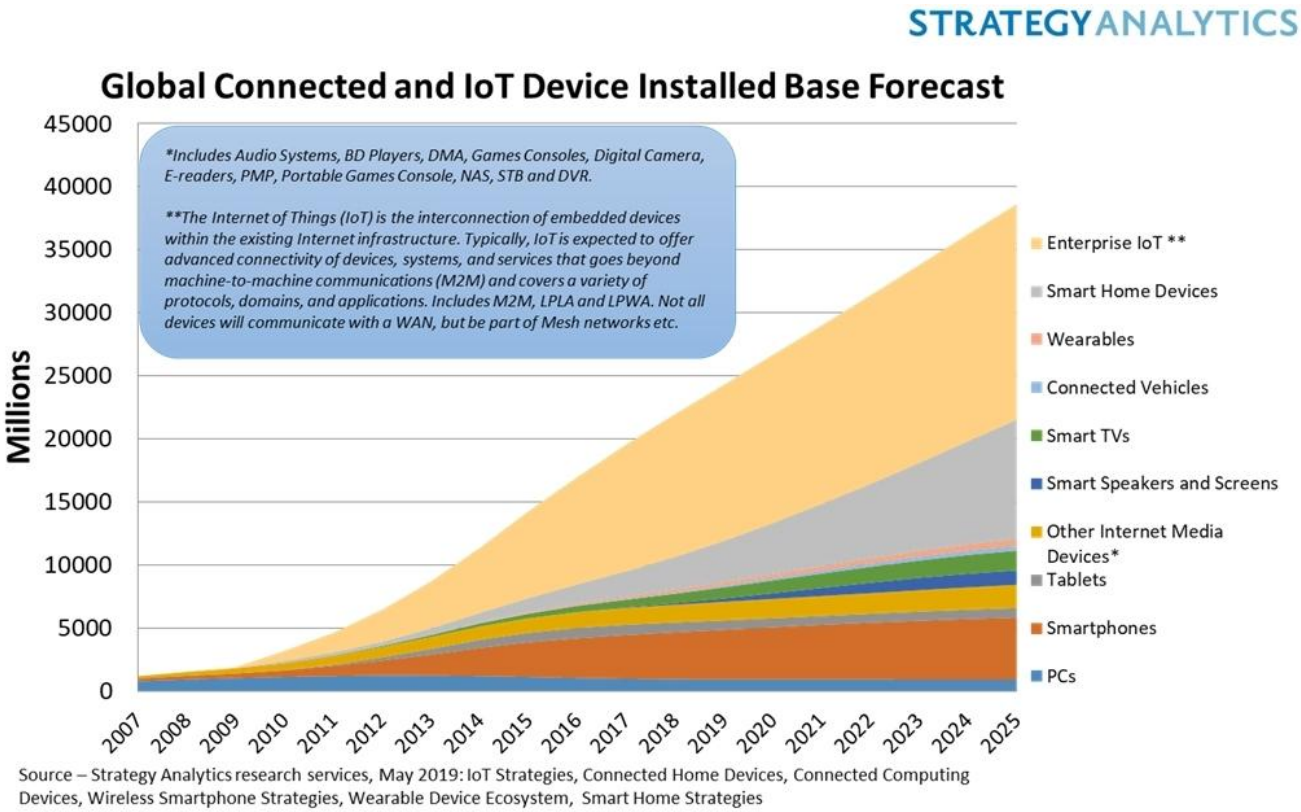
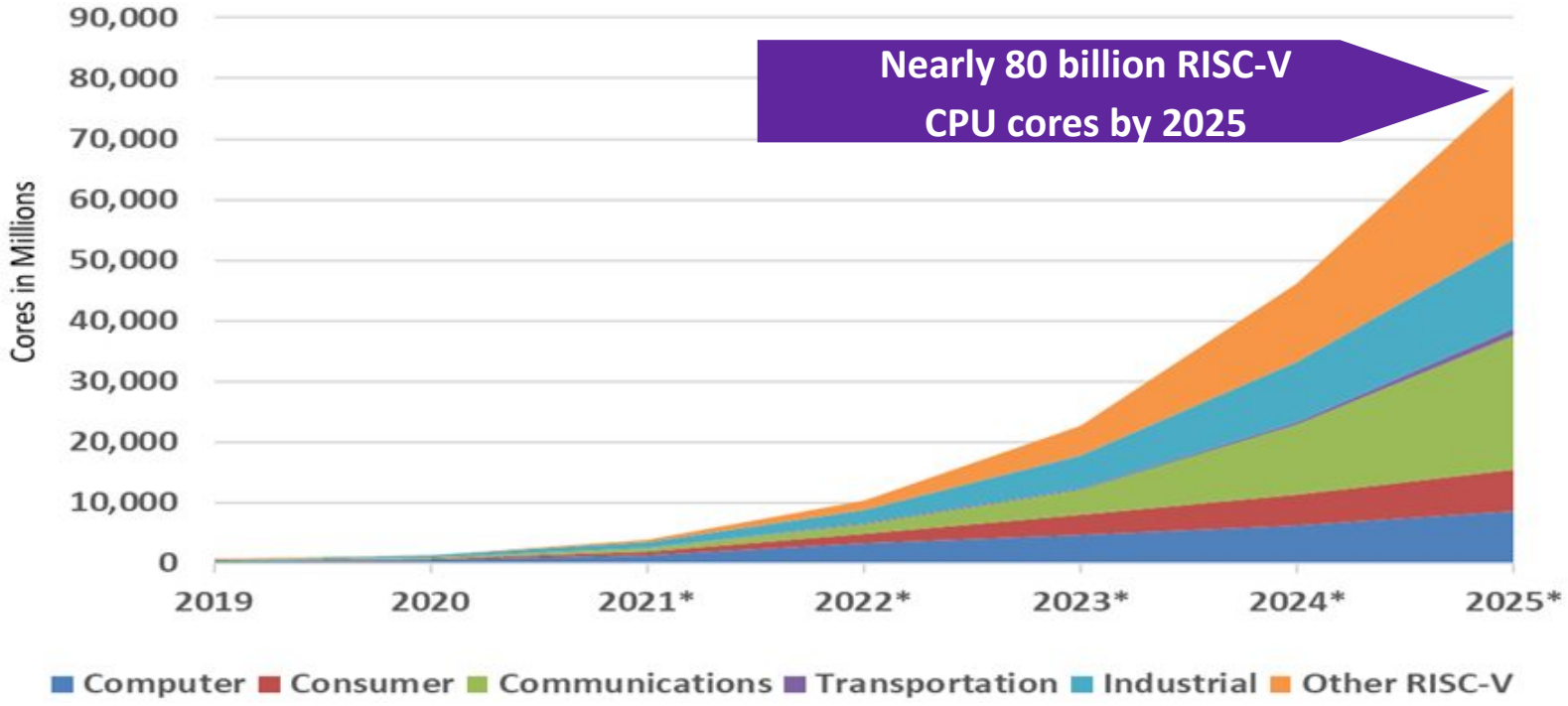
50 billion connected and IoT devices by 2030



Source: Strategy Analytics

The RISC-V CPU core market will grow at 114.9% CAGR, capturing over 14% of all CPU cores by 2025



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Source: Semico Research Corp, March 2021

2 billion RISC-V cores in market in 2021

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"Deloitte Global predicts that

the market for RISC-V processing cores will double in 2022 from what it was in 2021, and that it will double again in 2023,

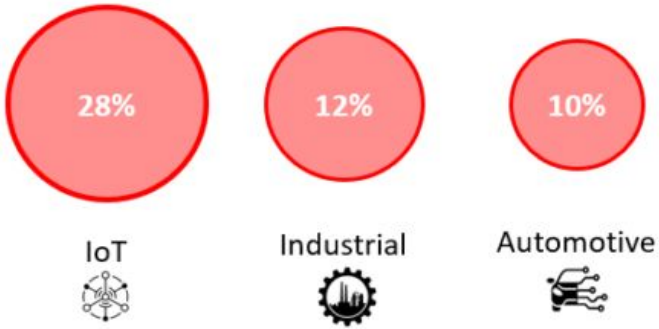
as the served addressable market available for RISC-V processing cores continues to expand."

December 2021

industry adoption

Semiconductor IP market size, 2020 vs 2025

RISC-V Penetration Rate by 2025



"The rise of RISC-V cannot be ignored… RISC-V will shake up the $8.6-Billion semiconductor IP market."

-- William Li, Counterpoint Research

Advantages RISC-V offers

Source: Counterpoint Research, September 2021

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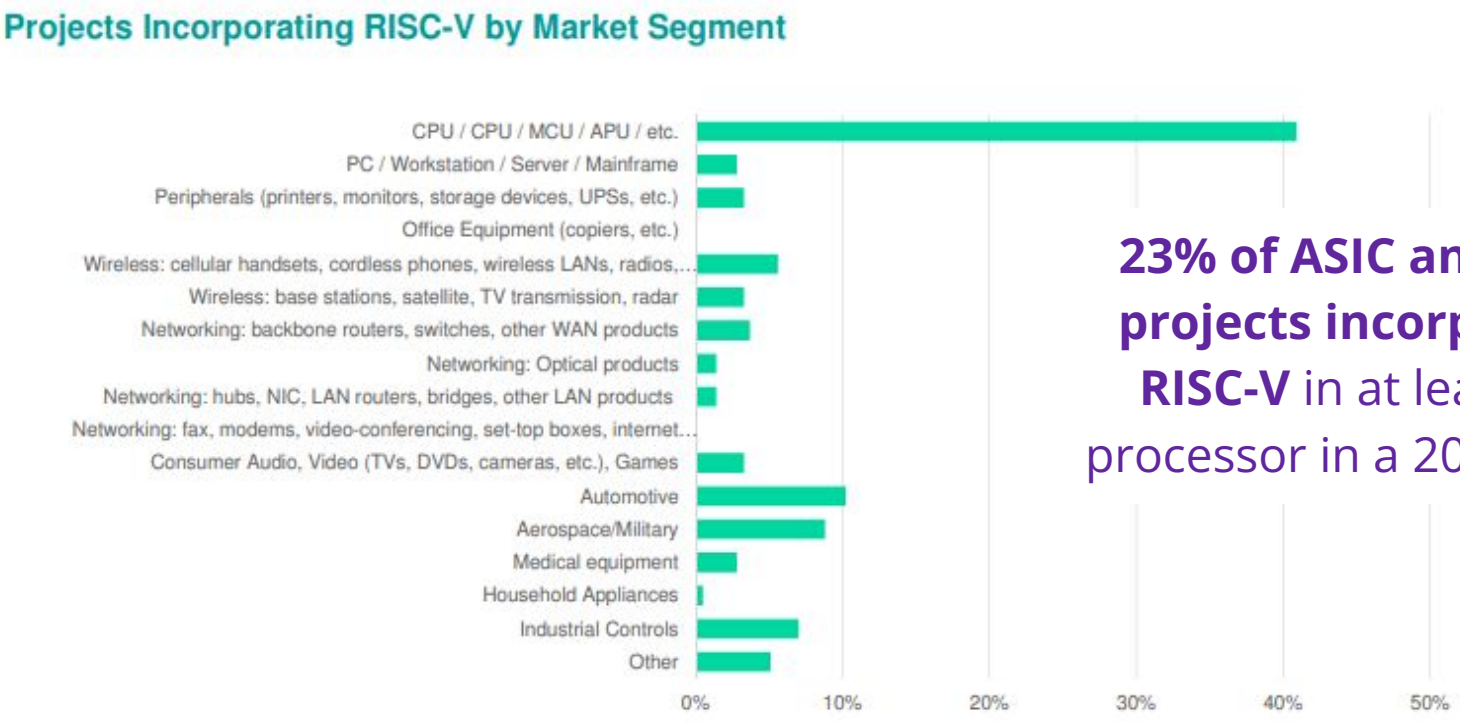
Today, nearly a quarter of designs incorporate RISC-V



23% of ASIC and FPGA projects incorporated RISC-V in at least one processor in a 2020 study.

Source: Tech Design Forum, November 2020

- **Alibaba** RISC-V Xuantie processor line including four open sourced processors for cloud and edge servers
- **Imagination** RISC-V CPU family, for both the discrete CPU and heterogeneous computing markets
- **Seagate** hard disk drive controller with high-performance RISC-V CPU.
- **Ventana** performance chiplet approach to data center SoC design
- **Intel** Nios processor based on RISC-V, designed for performance.

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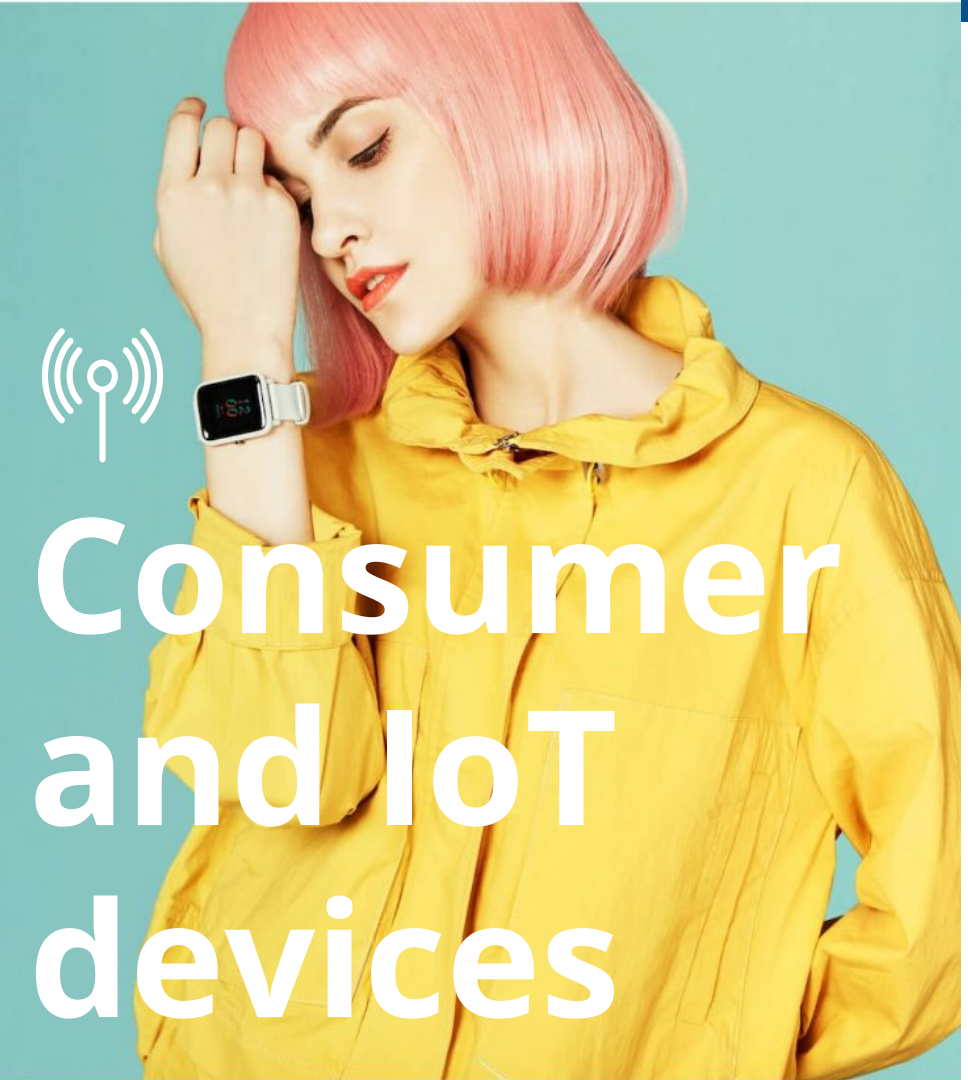
Telecom & Communications

- **Andes** 64-bit RISC-V processor has been adopted by SK Telecom for the development of AI products.
- **Alibaba** PLCT Lab has ported Android 10 onto its in-house 64-bit RISC-V core emulated in QEMU
- **Google** Pixel 6 Titan M2 in-house designed RISC-V processor, with extra speed and memory, and even more resilient to advanced attacks.

Automotive

- **Imagination Technologies** GPU can be linked together by a RISC-V core for ASIL-B level designs with ISO26262 safety critical certification.
- **IAR Systems** extended the functional safety version of its Embedded Workbench software tool chain to the RISC-V core of Nsitexe, subsidiary of automotive leader Denso.
- **Renesas and SiFive** jointly develop next generation RISC-V SoCs for automotive
- **Renesas and NSI-TEXE** announce automotive SoC with RISC-V-based parallel co-processor
- **Europe's GaNext project** to simplify designing power converters with GaN power semiconductors while improving efficiency and compactness for systems such as electric vehicle chargers.

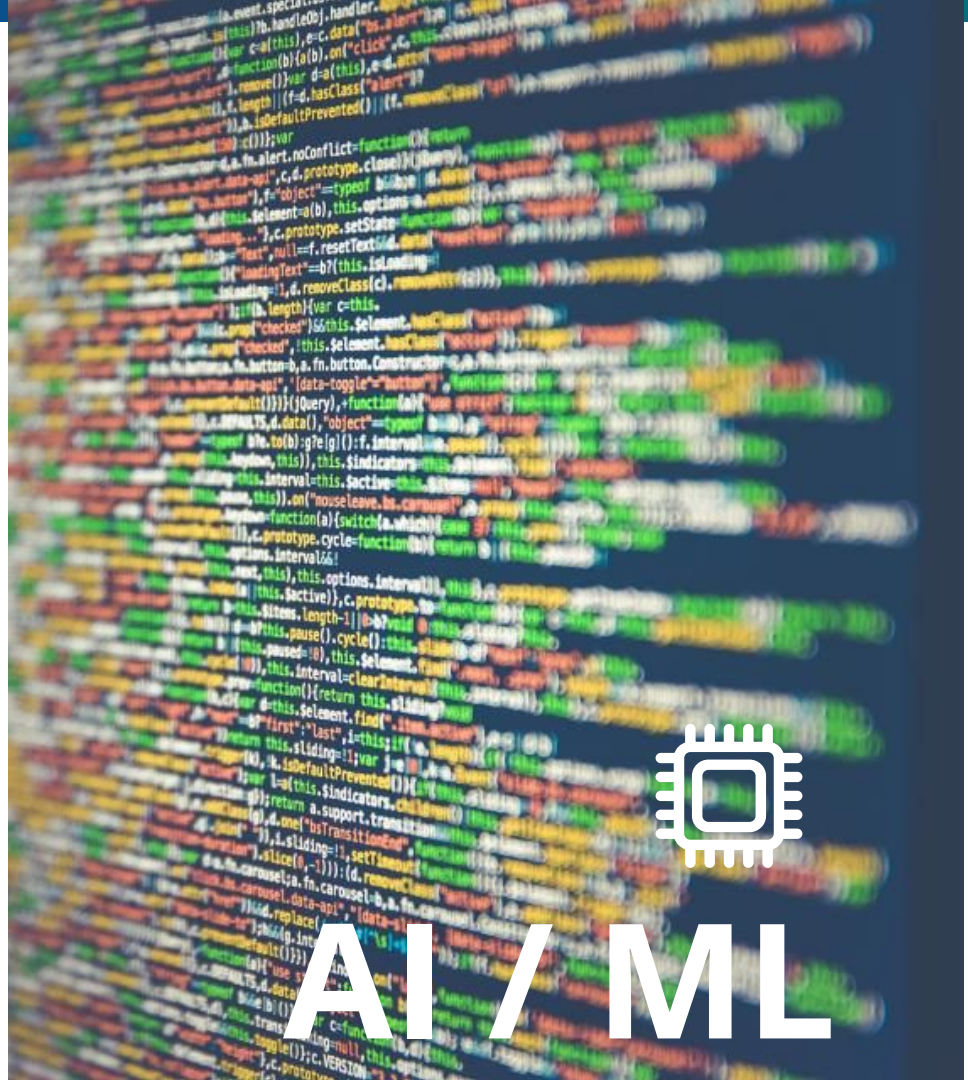


Consumer and IoT devices

- **Huawei** Hi3861 RISC-V board for Harmony OS developers for the IoT market
- **Zepp Health** / Huami wearable manufacturer OS supporting RISC-V Reference Models for RISC-V P extension
- **GreenWaves** ultra-low power GAP9 hearables platform for scene-aware and neural network-based noise reduction.
- **Microchip** released the first SoC FPGA development kit based on the RISC-V ISA.
- **RIOS Lab** announced PicoRio, an affordable RISC-V open source small-board computer.
- **SiFive** world's fastest development board for RISC-V Personal Computers.

Artificial intelligence spans many areas from Industrial IoT to financial

- **Esperanto** Emerges From Stealth With 1,000-Core RISC-V AI Accelerator.
- **StarFive** released the world's first RISC-V AI visual processing platform
- **Andes** released superscalar multicore and L2 cache controller processors.
- **NVIDIA CUDA** support on the Vortex RISC-V GPGPU enables scaling from 1-core to 32-core GPU based on RV32IMF ISA with OpenCL 1.2 graphics API support.



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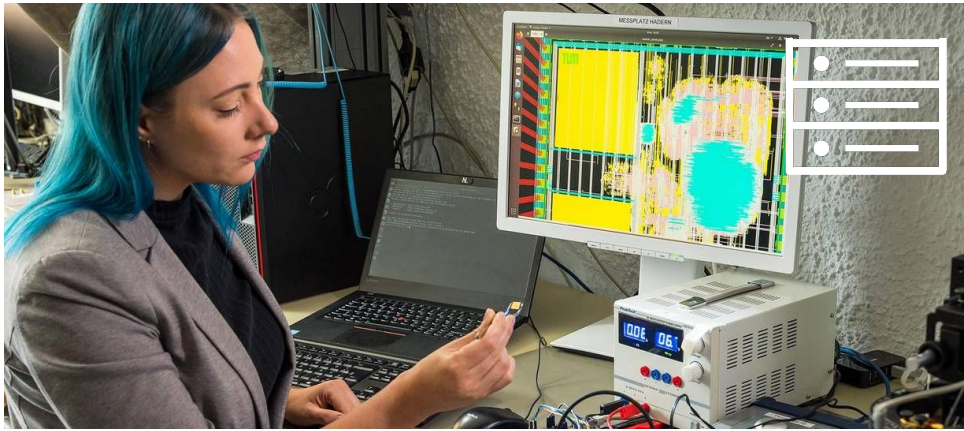
Edge Computing

A distributed, open architecture decentralizes processing power, reduces latency, and supports IoT performance in low bandwidth environments at low power.

- **Seeed Studio**'s new development, the Sipeed MAIX, a RISC-V 64 AI board for Edge Computing makes it possible to embed AI to any IoT device.
- **Micro Magic** announced an incredibly fast 64-bit RISC-V core achieving 5GHz and 13,000 CoreMarks at 1.1V.
- **Western Digital** SweRV Core enables spectrum of compute at the edge

High Performance Computing

- **European Processor Initiative** RISC-V accelerator with first chip Sep 2021
- **Technical University of Munich** (TUM) quantum cryptography chip for quantum computing security demands
- **Tactical Computing Labs** HPC-centric software test suite for GCC and LLVM
- **Cortus** is developing a high-performance RISC-V Out-of-Order processor core for the European eProcessor project.
- **De-RISC** market-ready HW-SW platform for a multi-core RISC-V system-on-chip for safety critical aerospace applications



Johanna Baehr of TUM heads a team that has hidden four hardware Trojans on this chip - malicious functions that are integrated directly into the circuits.

Image: Astrid Eckert / TUM

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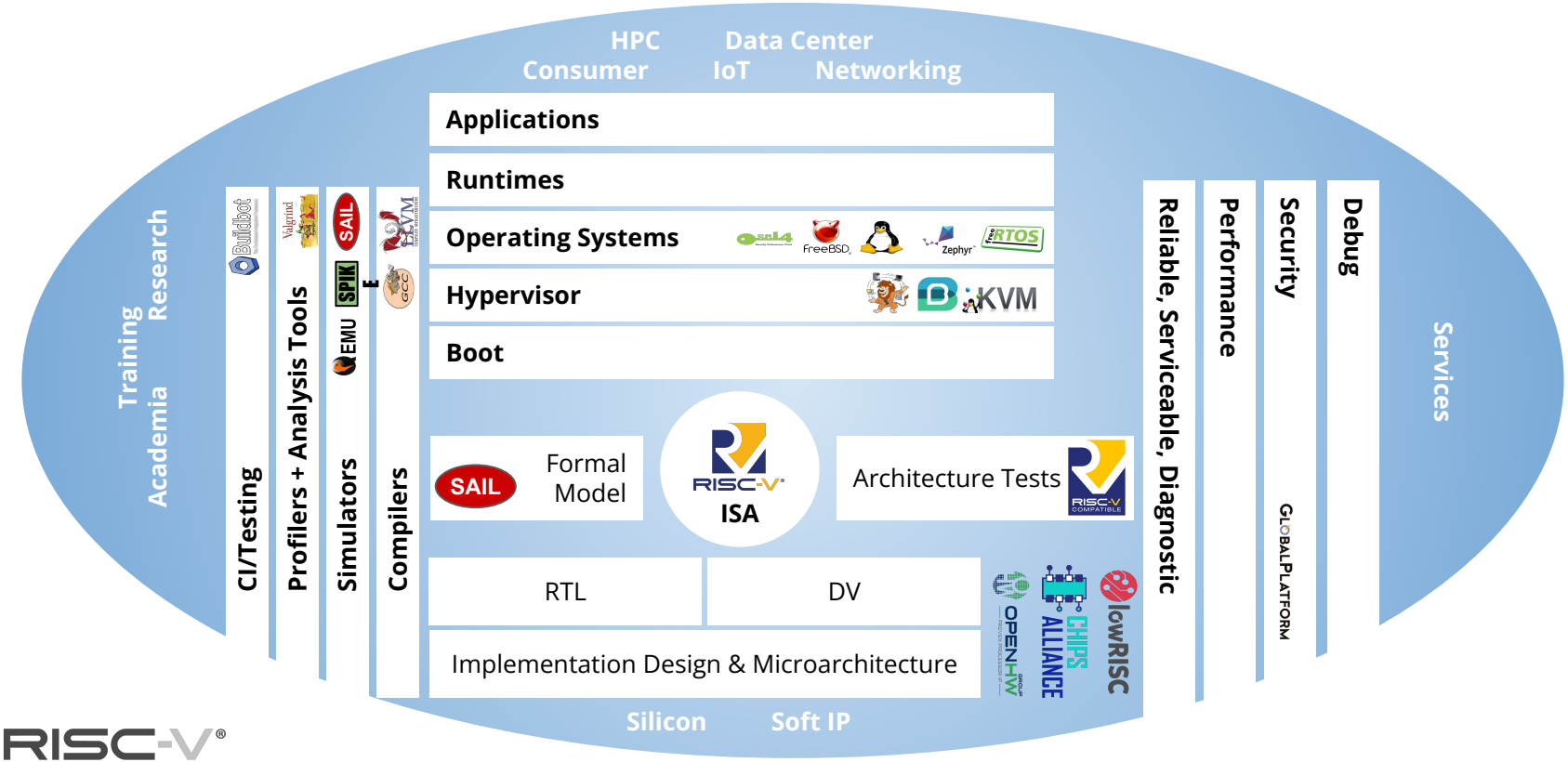
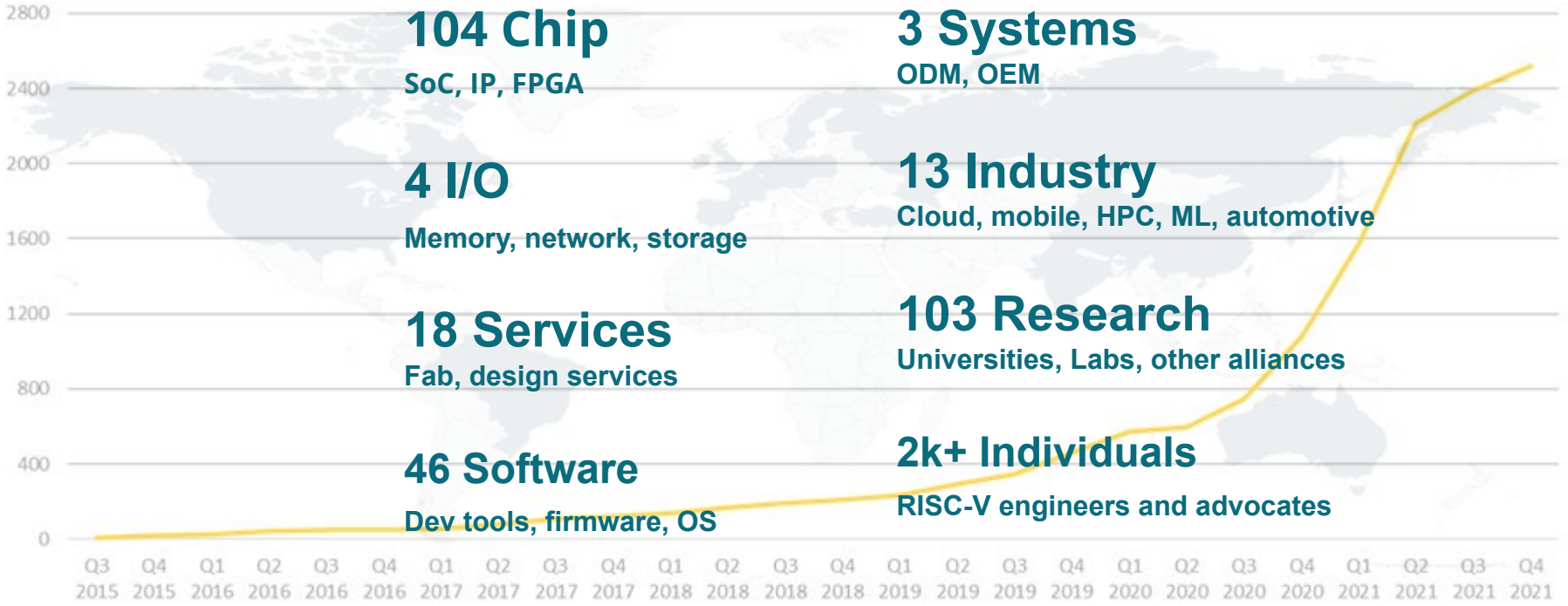
A community collaborating across the industry



More than 2,500 RISC-V Members
across 70 Countries



104 Chip
SoC, IP, FPGA

4 I/O
Memory, network, storage

18 Services
Fab, design services

46 Software
Dev tools, firmware, OS

3 Systems
ODM, OEM

13 Industry
Cloud, mobile, HPC, ML, automotive

103 Research
Universities, Labs, other alliances

2k+ Individuals
RISC-V engineers and advocates

RISC-V membership rapid growth continues by more than 130% in 2020 and again in 2021

Technical Deliverables

Technical **governance**
Build **technical deliverables**
Work groups

Compatibility & Verification

Testing and compatibility **resources**
Compatibility **tests**

Visibility

Amplify member news, content, and success with press and analysts
Original content programs
RISC-V, industry, and regional **events**

Learning & Talent

Multi-level **online learning**
Connecting **universities** with labs, tests, and curricula
RISC-V **Training Partners**
Jobs and internships

Advocacy + Alliances

RISC-V **Ambassadors**
Geo and industry **alliances**
Local developer groups and events

Marketplace Exchange

Online marketplace of providers, products, services, and learn
Technical **developer forums**

RISC-V delivers incredible member support

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Progress RISC-V Roadmap

Industry Adoption

2010 – 2016
- Test Chips
- Software tests
- Linux port

2017
- Proof of Concept SoCs
- Minion processors for power management, communications
- Bare metal software

2018
- IoT SoCs
- Microcontrollers
- RTOS, Firmware
- Development tools
- Technical Steering Committee, HPC SIG, GlobalPlatform partnership

2019
- AI SoCs, Application processors, Linux Drivers, AI Compilers
- Dev Board program
- Development Partners
- RISC-V Labs, Security response process, AI SIG, Graphics SIG, Android SIG, Communications SIG

2020
- Proliferation of RISC-V CPUs across performance and application spectrum
- RISC-V dominant in universities
- Strategic and growing adoption in HPC, automotive, transportation, cloud, industrial, communications, IoT, enterprise, consumer, and other applications

2021
- ISA Definition
- RISC-V Foundation

2022
- RV32

2023
- RV32I and RV64I Base instructions: Integer, floating point, multiply and divide, atomic, and compact instructions
- Priv modes, Interrupts, exceptions, memory model, protection, and virtual memory

2024
- Arch compatibility framework,
- Processor trace

2025
- Zfinx
- ZiHintPause
- BitManip
- Vector
- RISC-V Profiles & Platforms
- Crypto Scalar
- Virtual Memory
- Hypervisor & Advanced interrupt architecture
- Cache mgt ops
- Code size reduction*
- Trusted Execution Environment*
- P (Packed SIMD)*

Technical Deliverables

- RV32E and RV64E
- 64 bit and 128 bit addresses*
- Vector Atomic and quad-widening*
- Quad floating point in integer registers*
- Crypto Vector*
- Trusted Execution phase 2*
- Jit pointer masking & I/D synch*
- BitManip phase 2*
- Cache management phase 2*
- … and more

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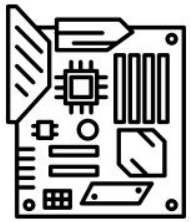
** On track, subject to change*

RISC-V Technical Programs



RISC-V Developer Boards
Available to spur innovation, provide hands-on education, and engage early adopters to test and develop.

RISC-V Development Partner
Recognizes the investment and dedication of organizations making significant technical contributions to RISC-V.

RISC-V Lab
Institutions that host a lab with RISC-V hardware for CI/testing and general availability sandboxing.

RISC-V Compatible
Architectural Tests created to help ensure that software written will run on implementations that comply with that profile. Branding available for compatibility.

RISC-V Platform
A common, reusable runtime environment that operating systems and applications can target to improve portability and reuse. Provides interoperability assurance.

RISC-V Profiles
Refers to a base ISA and one or more extensions that are specified as a group so that applications can be compiled once, run on different implementations, and get the same results.

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https://wiki.riscv.org/display/TECH

Amplifying success and engaging community

Events

RISC-V and Industry events

- Local, regional, and global events
- Speaking opportunities
- Showcase and announce RISC-V solutions
- Networking

RISC-V Blog

- Leadership and industry commentary, as well as technical information on your work with RISC-V.
- Members submit content to publish on riscv.org with a link to the member website.

Case Studies

- Elevate technical conversations to business objectives and challenges, showing adoption of RISC-V.
- Case studies on riscv.org are shared to media channels and analysts.

Social Amplification

- Members submit original content for posting on RISC-V social channels
- Members and the community submit content for re-sharing.
- Amplify member announcements via social

Press and Analysts

- Share member and community news "In the News"
- Provide RISC-V quotes for member press releases
- Participate in media panels and interviews.

RISC-V Exchange

- Promote member and community solutions
- Connect developer community

RISC-V Ambassadors

- Technical leaders engaged deeply and visibly in engineering community

RISC-V Alliances

- Technical and strategic relationships across industries, geographies, and technical domains providing mutual community support

RISC-V Talent

- Open Hardware Diversity Alliance
- RISC-V Mentorships and Careers
- University resources
- Online Courses
- Training Partners

Engage!
- RISC-V Marketing Committee
- RISC-V Events Committee
- RISC-V Content Committee
- RISC-V Academia + Training SIG

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Benefits of engaging in RISC-V

- ✔ **Accelerate technical traction** and insight
- ✔ **Contribute** technical priorities, approaches, and code
- ✔ Gain strategic and **technical advantage**
- ✔ **Increase visibility**, leadership, and market insight
- ✔ Fill and increase **engineering skills**, retain and attract talent
- ✔ Build **innovation partner** network and customer pipeline
- ✔ **Deepen, engage, and lead** in local and industry developer network
- ✔ **Showcase RISC-V products**, services, training, and resources

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RISC-V is a community of passionate, dedicated, and invested stakeholders

As individuals
As companies
As universities
As public institutions and non-profits
As nations

As one Global, connected movement

Build RISC-V into your company strategy, and your personal mission

Thank You

www.riscv.org

@risc_v

risc-v-international
calistaredmond

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Back-up slides

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- Grew RISC-V **Membership 130%+**, 2.4k+ members
- Streamlined technical governance, processes, and documentation -- ratified **16 specifications**
- **Launched the Open Hardware Diversity Alliance**, as well as grew **alliances by 37%** with dozens of technical, industry, and local alliances
- Launched RISC-V **online courses with 8,842 enrollments** in the first 9 months, announced our third course today!
- Connected the community through **90 events** including the **RISC-V World Conference China with 1,300+ in-person and 20,000+ online**, our biggest event ever

global collaboration

RISC-V strengthened community in 2021

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Dedicated Community

Services Fab, design services

I/O Memory, network, storage

Software Dev tools, firmware, OS

Press and Analysts

Individual Advocates

Chip SoC, IP, FPGA

Universities and Research

Industry cloud, mobile, HPC, ML, automotive

Investors and Funding sources

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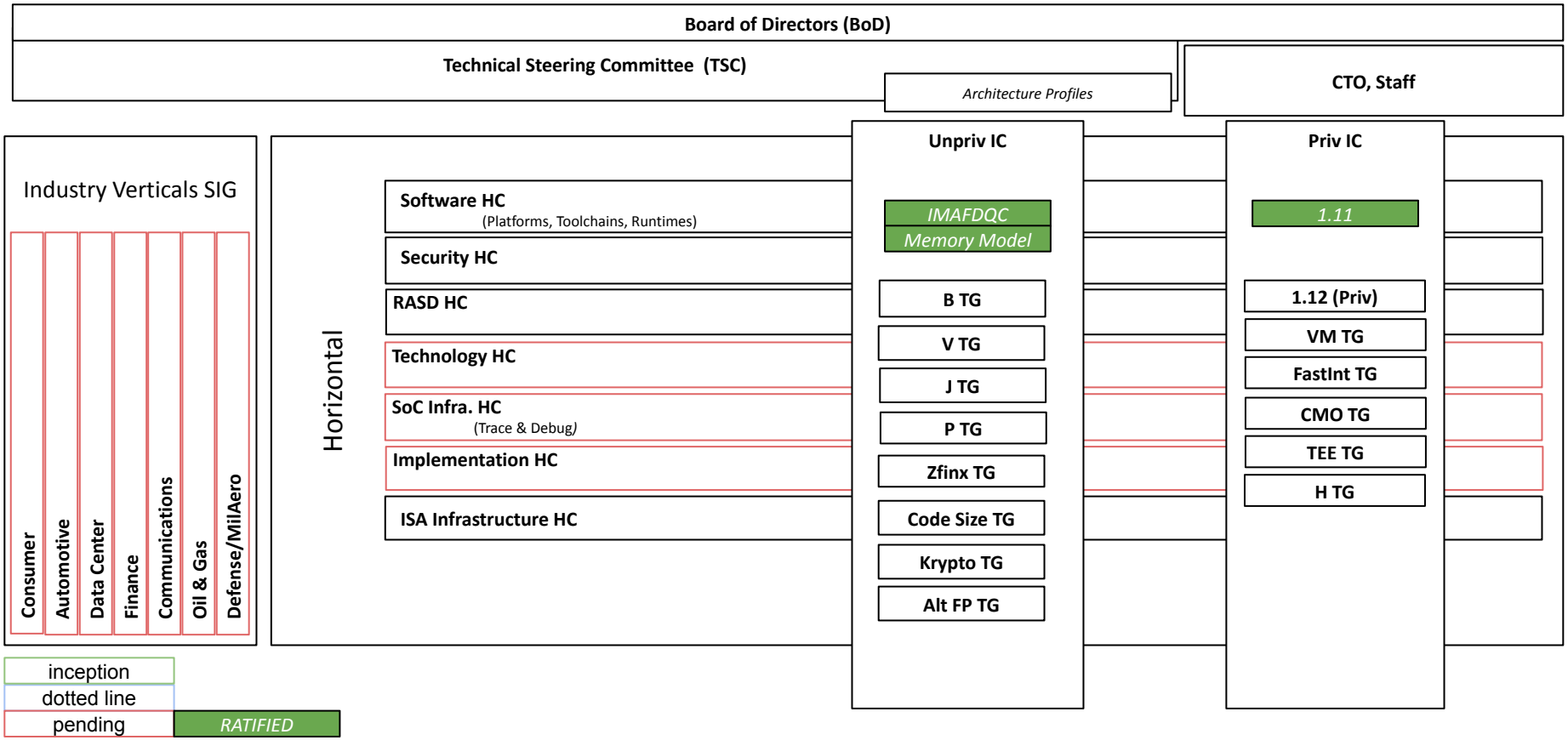
Technical Organization



Membership Options

RISC-V Membership details may be found online here

Premier Member Benefits

- Board seat and Technical Steering Committee seat included for $250k level
- Technical Steering Committee seat included for $100k level
- Eligible to lead workgroup and/or committee

- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Premier members
- Solution / Product listing highlighted on RISC-V Exchange, noted with member level
- 4 case studies a year
- 2 blogs per month
- 2 social media spotlights per month
- Spotlight member profile
- Event sponsorship discount

Strategic Member Benefits

- 3 Board reps elected for the Strategic tier, including Premier members that do not otherwise have a board seat
- Eligible to lead workgroup and/or committee

- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Strategic members
- Solution / Product listing highlighted on the RISC-V Exchange, noted with member level
- 1 case study a year
- 1 blog per month
- 1 social media spotlight per month
- Event sponsorship discount

Community Member Benefits

- Two Board representatives
- 1 Community Board representative, elected
- 1 Individual Board representative, elected

- Member logo / name listing on RISC-V website, by member level
- 1 case study a year
- 1 blog per quarter
- 1 social media spotlight per quarter
- Event sponsorship discount

Premier Requirements

- Membership open to any type of legal entity
- $250k Annual membership fee that includes Board seat and TSC seat
- $100k Annual membership fee that includes TSC seat

Strategic Member Requirements

- Membership open to any type of legal entity
- Annual membership fee based on employee size
  - 5,000+ employees: $35k
  - 500-5,000 employees: $15k
  - <500 employees: $5k
  - <10 employees & company <2 yrs old: $2k

Community Requirements

- Membership open to
  - academic institutions,
  - non-profits,
  - individuals not representing a legal entity
- No annual membership fee

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