# Optimizing Efficiency in Extended SIMD RISC-V Based Architectures through Minimization of Idle Computational Cores

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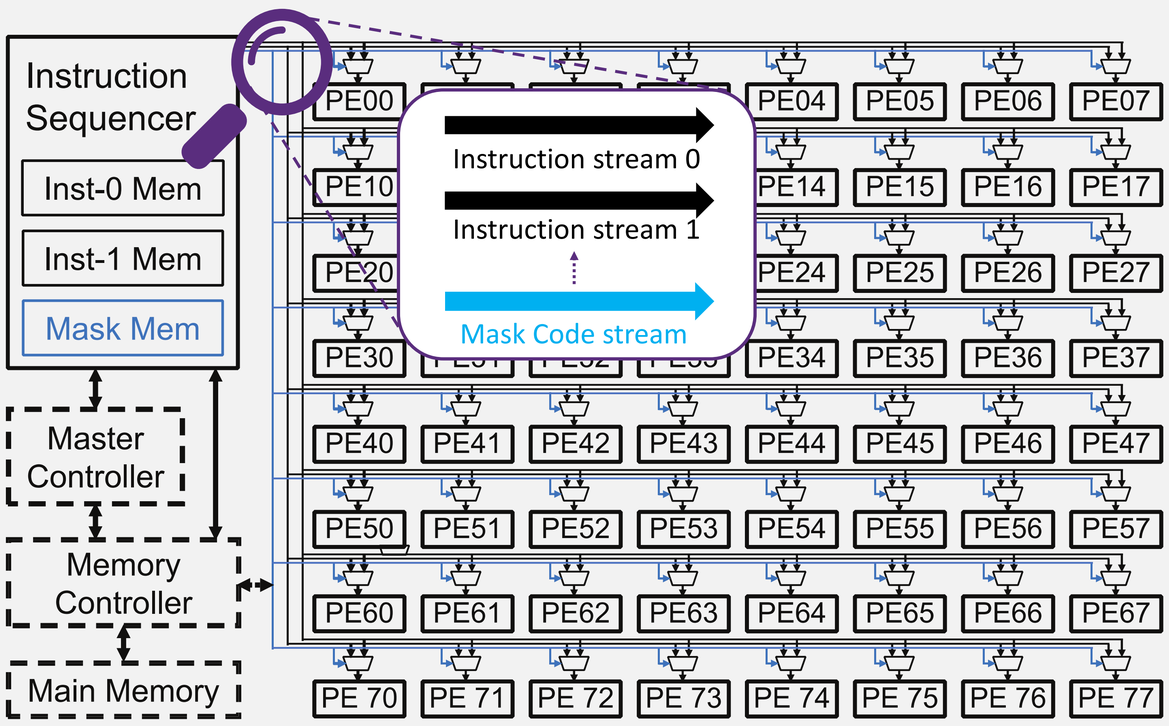
## 1. Motivation & Target

- Introduce **DIMD (Dual Instruction Multiple-Data)**, **Torus/Mesh Interconnect**, and **HBM (High Bandwidth Memory) and Memory Hierarchy**.
- SIMD processors often suffer from **Idle time** caused by **data transfer** & limited number of instructions at same time. How can we deal with them ?

## 2. Architecture Overview

### DIMD (Dual Instruction Multiple-Data)

Issue 2 instructions with mask code to all PE at same cycle.
Then each PE determine which instruction should be executed.

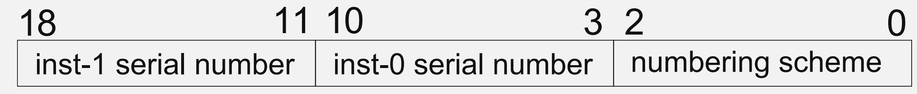


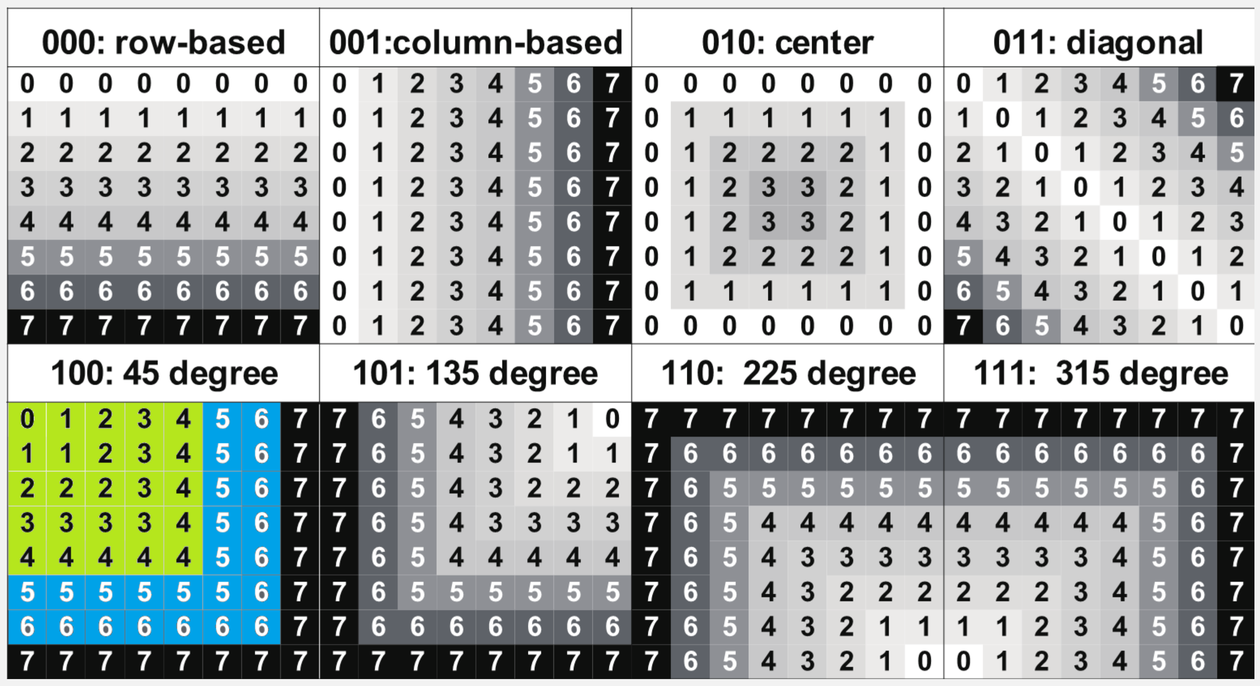

**Benefits**

Reduce idle time caused by limited number of instructions at SIMD.
Effective for stencil computation, FFT, etc.

### Format of mask code

Mask code consists of **serial numbers** and **numbering scheme**.

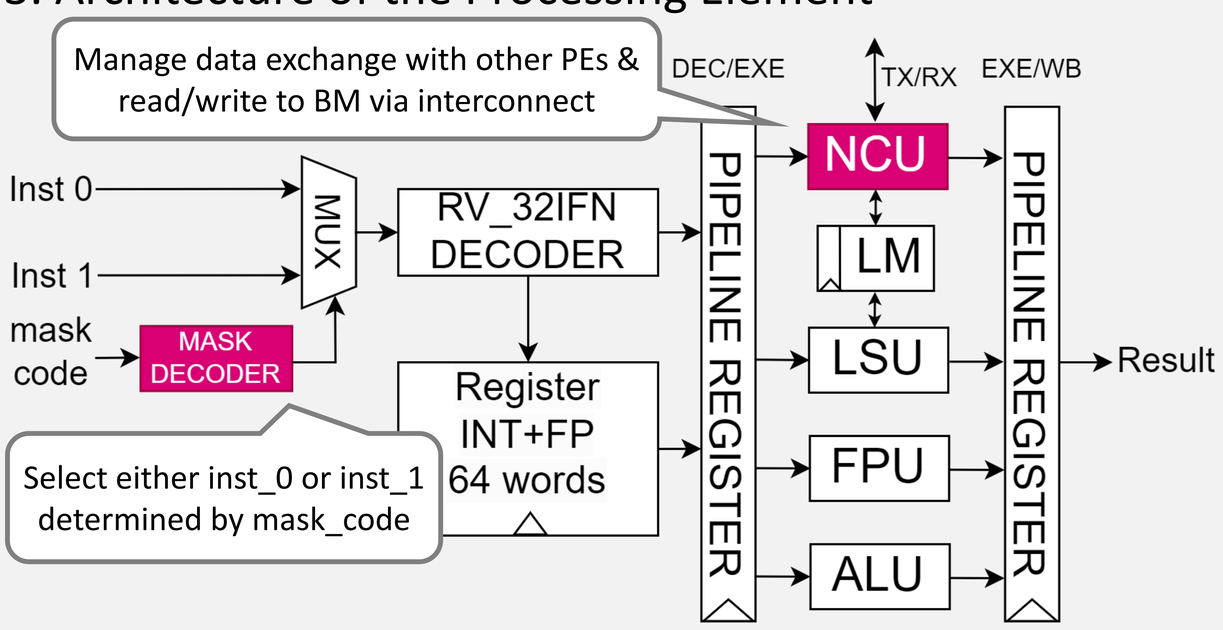



### Example of Operation

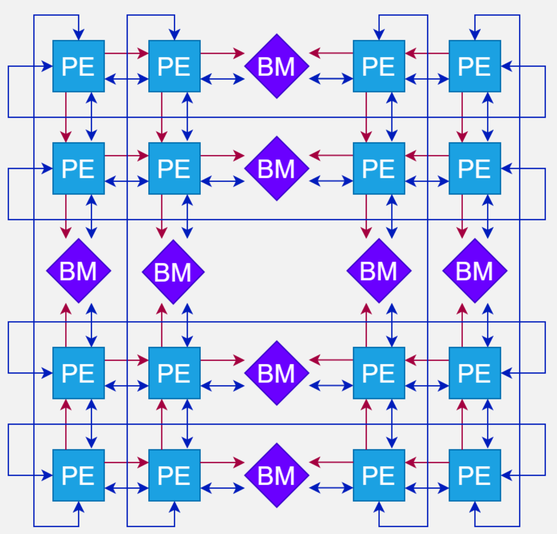
01100000 00011111 100 — Inst-0 — Inst-1 — Inst-idle

## 3. Architecture of the Processing Element



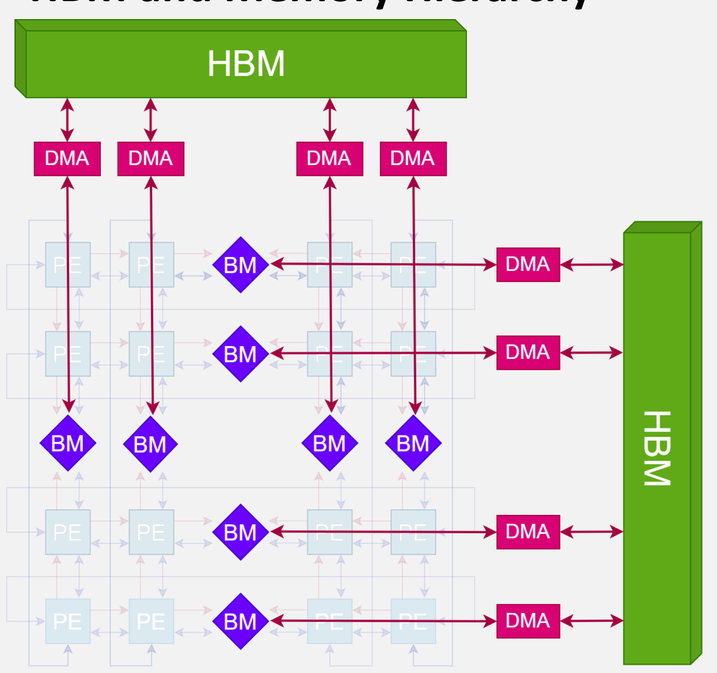

Adopt **RISC-V** as PE's ISA. We've fully designed processor dedicated to PE operations.

### Torus/Mesh Interconnect

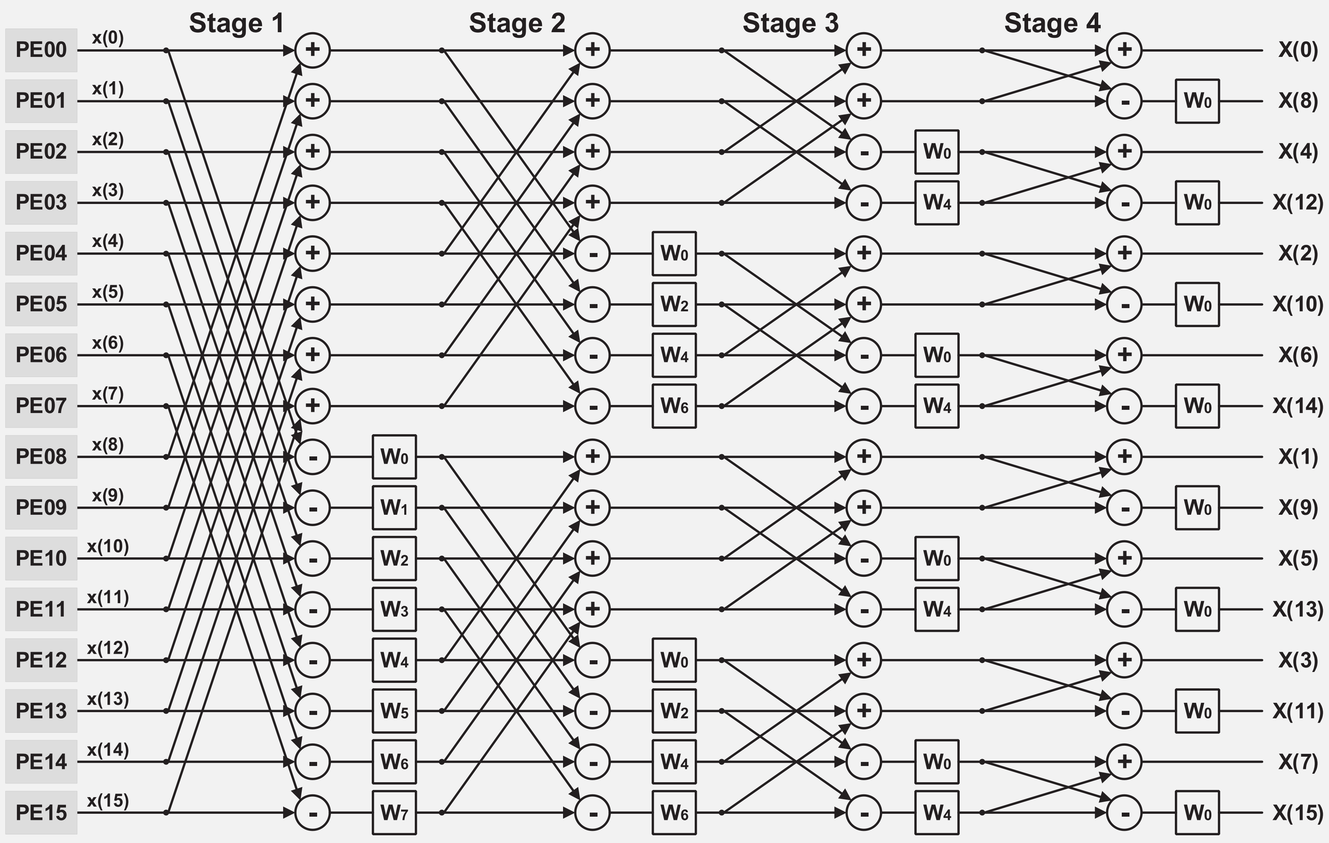



**Address line : Simplex Mesh**
**Data line : Duplex Torus**

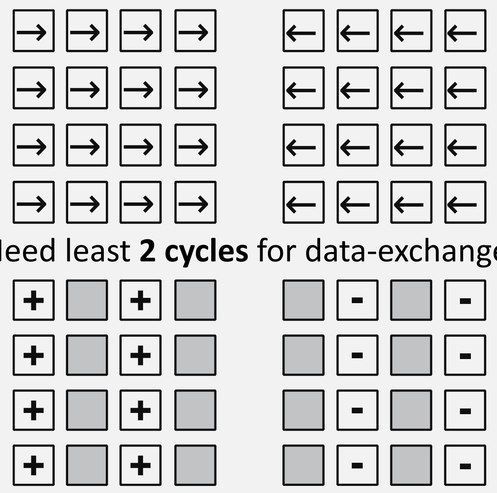
### HBM and Memory Hierarchy



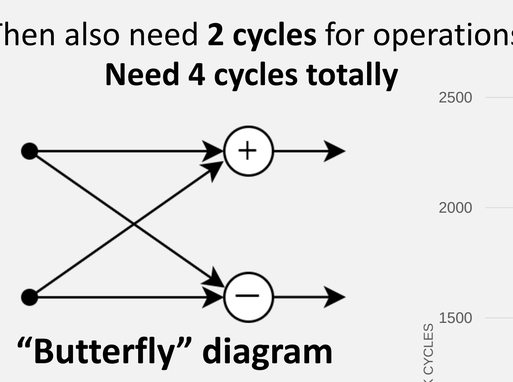

## 4. Comparison of FFT performance with SIMD




### "Butterfly" at FFT on SIMD

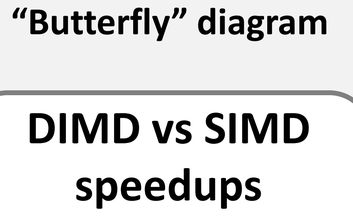


Need least **2 cycles** for data-exchange



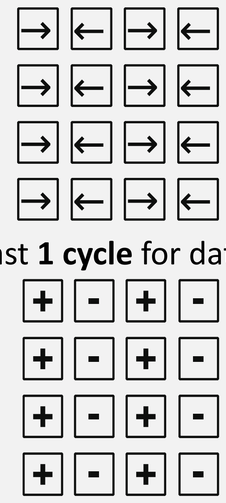
Then also need **2 cycles** for operations

**Need 4 cycles totally**

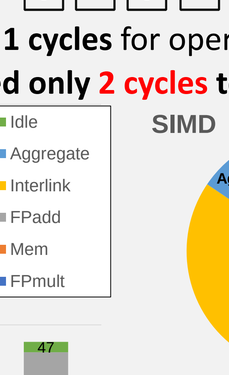


**"Butterfly" diagram**

### "Butterfly" at FFT on DIMD

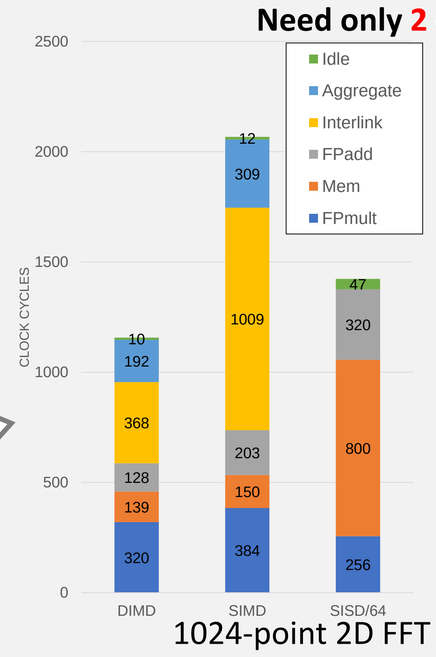


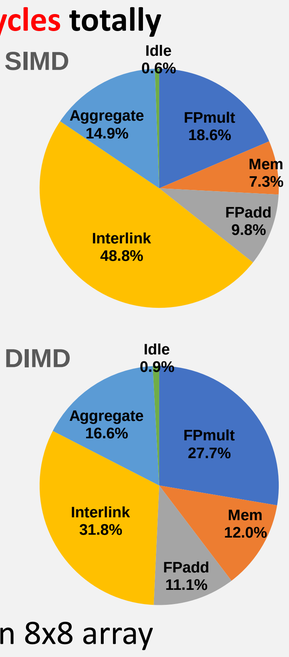
Need least **1 cycle** for data-exchange



Need **1 cycles** for operations

**Need only 2 cycles totally**




1024-point 2D FFT on 8x8 array


We are pursuing to implement this architecture on high-end FPGA, Xilinx ALVEO U280.
Estimating we can achieve more than 400 PEs scale many core processors.

**DIMD vs SIMD speedups**

**178% faster**