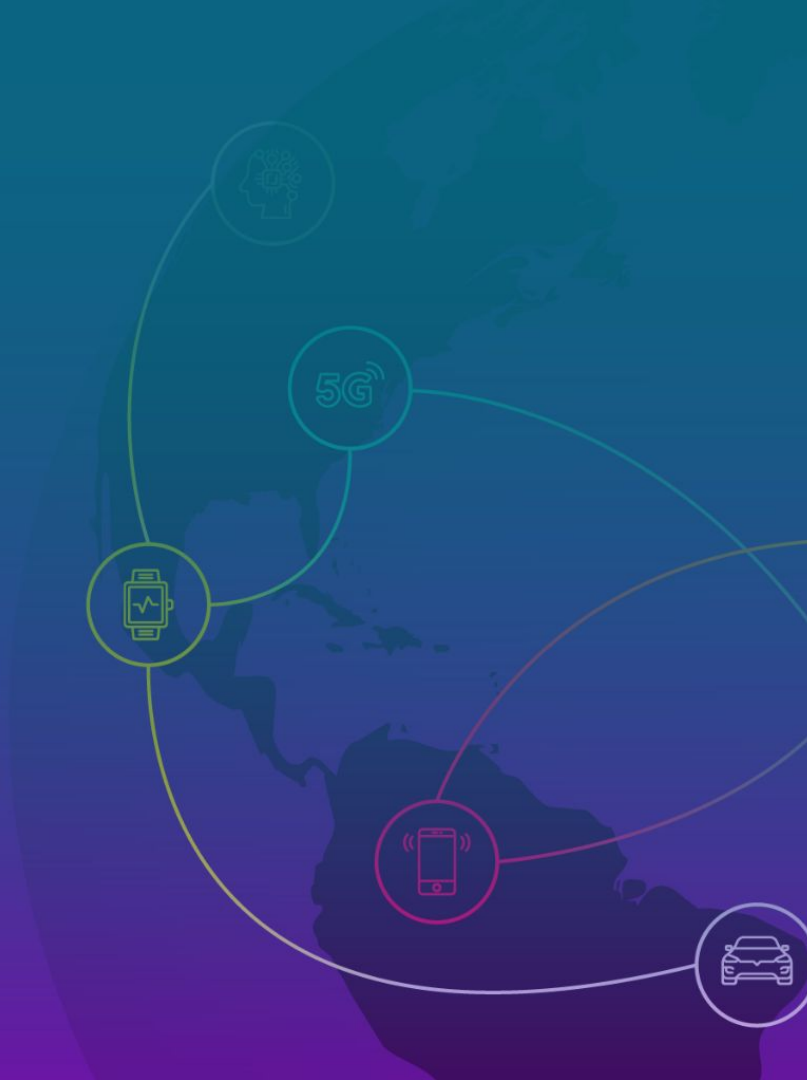
RISC-V®

Everywhere



The Road Ahead

Mark Himelstein
CTO, RISC-V International

RISC-V Day Japan 2023
June 2023

Overview

- RISC-V Overview
- Why People Use RISC-V
- Embedded
- Portability
- Embedded & Real Time ISA Extensions
- SW ecosystem

The definition of open computing is RISC-V

RISC-V is the most prolific and open Instruction Set Architecture in history

- RISC-V is inevitable
- RISC-V enables the best processors
- RISC-V is rapidly building the strongest ecosystem

RISC-V®

10s of Billions of RISC-V cores deployed for profit!

Open Source HW or Open Standard?

- We are officially an Open Standard HW ISA Architecture
- We are an Open Standard that works heavily with Open Source upstream projects (LINUX, GCC, LLVM, etc.)
- We don’t do reference implementations
- Our work product are specifications with support from Golden Models and Basic Tests

Unlike Open Source Software …

- Proprietary Custom Extensions are Encouraged and Welcome
- Products don’t just include the ISA, they can do custom implementations/extensions of/to the ISA
- Copyleft is a non-sequitur
- No restrictions on how the specification can be used
  - Only restrictions on branding

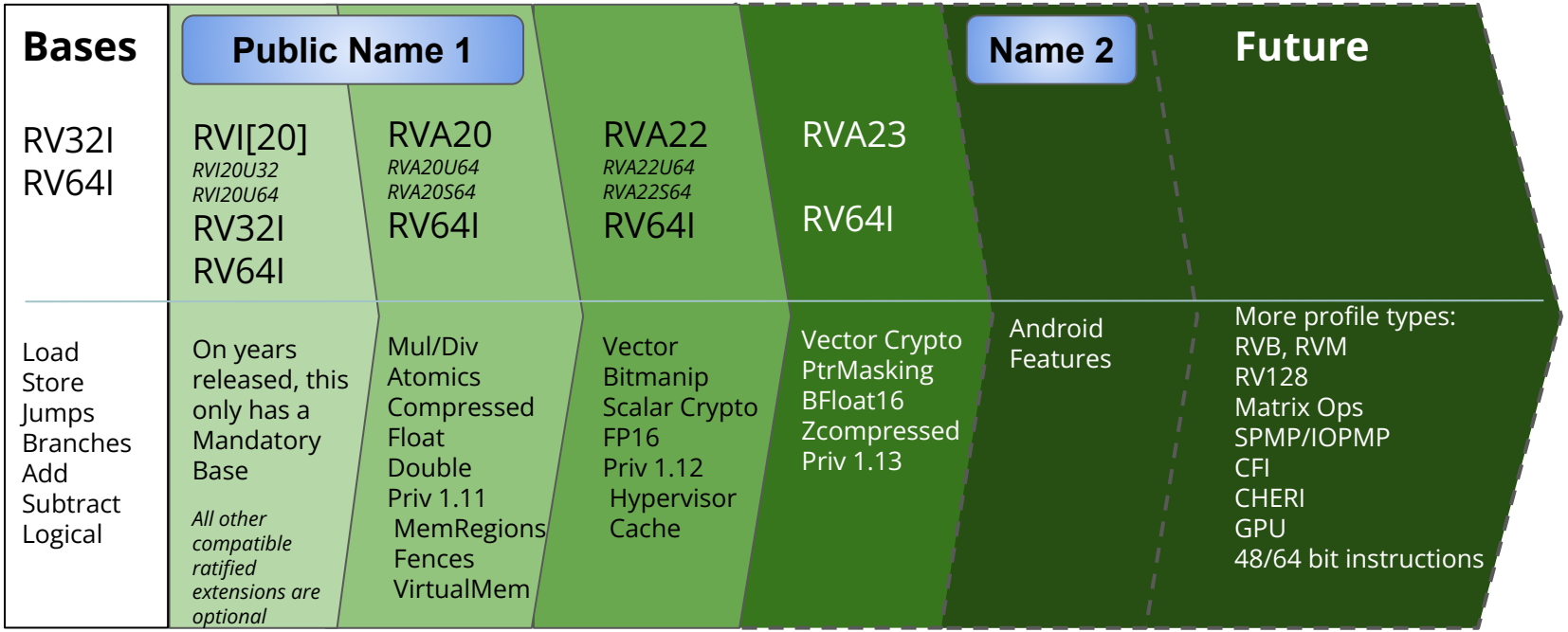
Why RISC-V?

- Flexibility
- Cost
- Ecosystem
- Our position in History
- EDA Renaissance
- Pride of Ownership

Portability

- **Unified common standard and a robust Software Ecosystem**
- **A robust economy around systems and software is reliant on portability**
- Application & Runtime Software
  - Profiles
  - API (e.g. POSIX)
- Operation Systems
  - Platforms
  - Supervisor Execution Environment (SEE)
  - Profiles

Profiles



- *Only a subset of extensions are listed above and it is not an exhaustive list*
- *Some extensions may be optional or non-profile in one profile and be mandatory in another*

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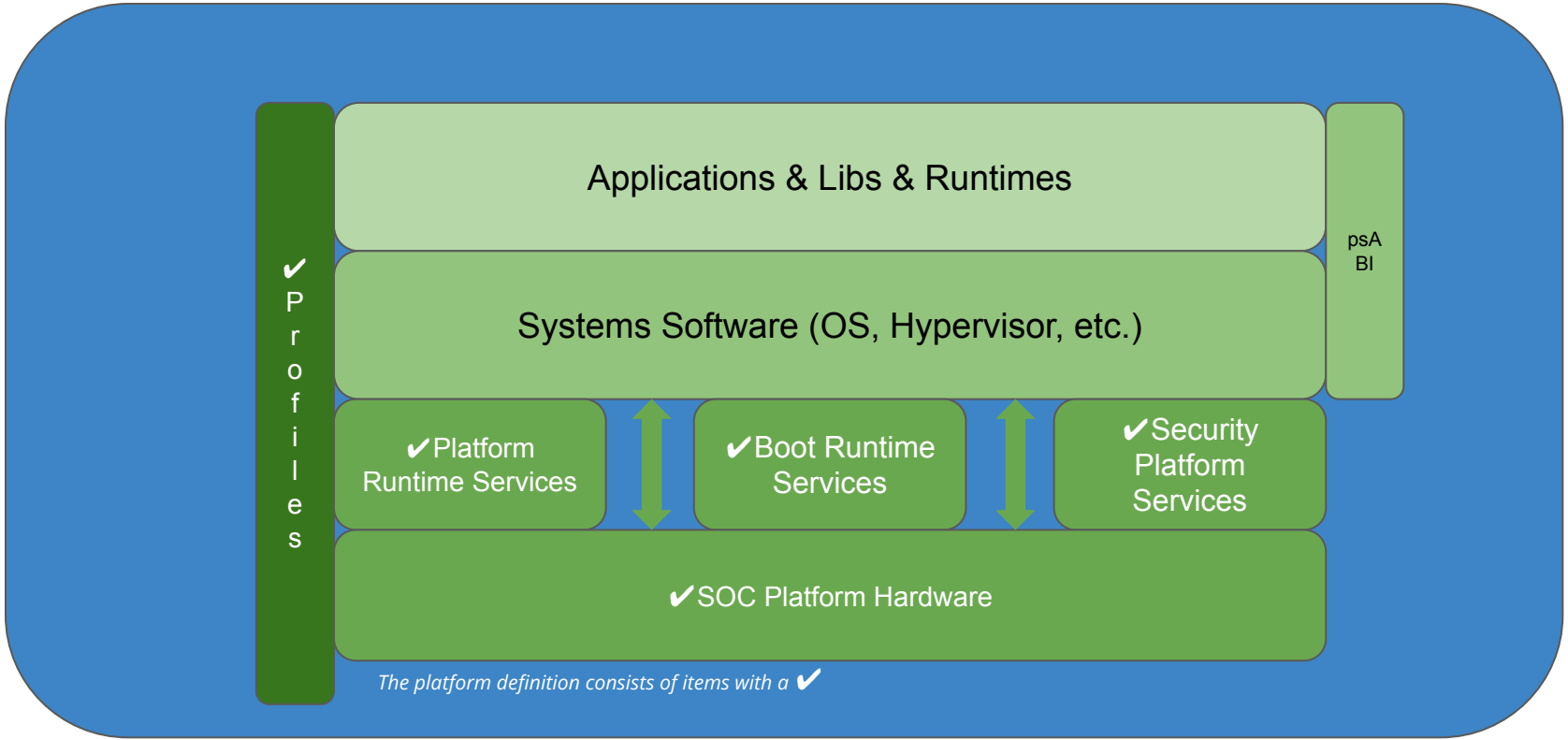
Platforms


✔Profiles
Applications & Libs & Runtimes
Systems Software (OS, Hypervisor, etc.)
psA
Bl
✔Platform Runtime Services
✔Boot Runtime Services
✔Security Platform Services
✔SOC Platform Hardware
The platform definition consists of items with a ✔

ISA Extensions Targeted at Embedded and Real Time

- Extensions: Fast Interrupts, Compressed Instructions (plus Zc*), FP in integer registers, Multiply without divide, Vector for embedded, S mode timer access, S mode w/o MMU, Wait on reservation set, Pause Hint, Physical Memory Protection, Scalar Crypto
- Profile Families: RVI, RVB, RVM
- Bases: RV32I, RV32E, RV64E

What We Have Done This Year

- Ratified ISA Specifications
  - Profiles, Code Size Reduction
- Ratified Fast Tracks
  - Counters, Total Store Ordering, RV32E/RV64E, Non Temporal Hints
- Documentation
  - Unpriv in Asciidoc, Asciidoc Priv draft
- New Task Groups & Special Interest Groups
  - Debug, Trace, and Performance Monitoring (DTPM) TG , Graphics SIG, RISC-V Common Software Interface (RVM-CSI) SIG, Vector (SIMD) SIG, Control Transfer Records TG

What's Coming Soon?

- Profiles
  - RVA23, RVI23, RVB23, RVM23, BOD committee on comprehensive ACTs & Certification
- Platforms
  - Portability for Systems Software (PRS, BRS, Platform Security, SOC HW, Profiles)
- ISA
  - Advanced Interrupts, QOS Register Interface, Control Transfer Records, Debug, Fast Interrupts, I/D Synch, Priv 1.13, Shadow Stacks/Landing Pads, Vector Crypto, Vector FP16
- ISA Fast Tracks
  - CAS, BFloat16, Conditional Ops, Counter Mode FIltering, HW PTE A/D, Maybe Ops, Additional Scalar FP, Counter Delegation,
- Non-ISA
  - IOMMU, Confidential VM extension, IOPMP, Nexus Trace,
- Documentation
  - Full time RVI DOC Architect/Writer approved
  - BOD committee on dev experience (content & UX)
  - Glossary, Navigation

Software Ecosystem

This is our number one priority

Accelerating the Rich RISC-V Ecosystem

Security HPC AI / ML Cloud - Data Center - Storage - Networking Consumer - IoT - Automotive Mobile

Applications

Libraries

Infrastructure

Runtimes

OS

Hypervisor

Boot

Design Tools + Compilers

Ecosystem Standards, upstream / support common tools

ISA Extensions, Profiles, Platforms

Security model, IOMMU, Industry SIGs

SAIL Golden Model

RISC-V ISA

Architecture Tests

Attributes: Debuggable, Secure, Performant, Reliable/Serviceable/Diagnosable

Implementation

RTL | DV

Design & Microarchitecture

Silicon Training Research

Soft IP Academia Services

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Android

- Google Support
  - Tier 1
- Google Requirements
  - Engagement with RISC-V
  - Likely in 2024
  - Much is underway
- Lifetime can be 10 years

RT-Thread on RISC-V

RV32

- HiFive1
- RV32M1_VEGA
- HPM6750
- GD32VF103
- AB32VG1
- CH32V103
- CH32V208
- CH32V307
- CH569
- BL808
- ESP32C3

RV64

- K210
- Allwinner D1
- Allwinner D1S
- QEUME/RISCV64 VIRT

RV-Core

- bumblebee
- QingKeV3
- QingKeV4
- E310
- cv32e40p
- Andes D45
- SMART-EVB for T-Head CPU E9xx Series
- PicoRV32

Software Ecosystem Resources

- Foundational Software Status for each extensions
- Draft spreadsheet of software on RISC-V status (140+ being tracked)
  - Hired RVI Software Ecosystem Director. First task is a comprehensive one stop clearinghouse of RISC-V commercial and open source software status
- RISC-V Ecosystem Landscape
- RISC-V Exchange (100s)
- A new Linux Foundation Project named RISE to accelerate open source software development on RISC-V

Join RISC-V

Change the World!

Questions

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