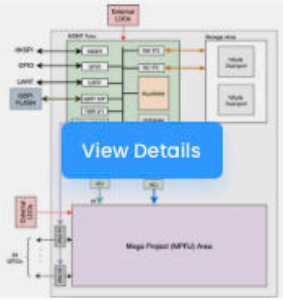
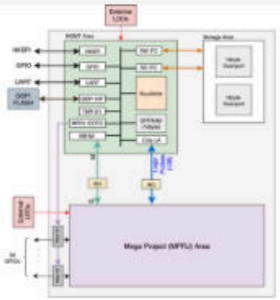


Caravel-SOFA-CHD public

Xifan Tang | https://sites.google.com/site/pegaillardon/home

SOFA-CHD (Skywater Opensource FPGAs)

MPW-1 SKY130 917

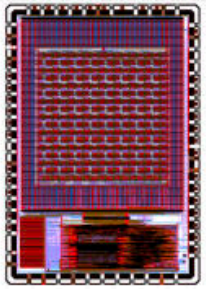


Caravel_RISCV_OSU public

James Stine | https://vlsiarch.ecen.okstate.edu/

Caravel_RISCV_OSU is an implementation of a single-cycle RISC-V processor inside of the Caravel...

MPW-1 SKY130 1.2k

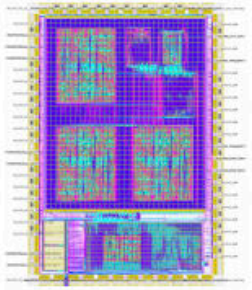


Caravel-OpenFPGA-EF public

Manar Abdelatty | http://efabless.com

A template SoC for Google sponsored Open MPW shuttles for SKY130.

MPW-1 SKY130A 1.8k

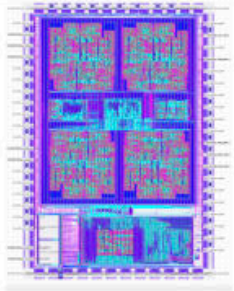


Chameleon SoC public

M. Shalan | http://efabless.com

AHB-Lite based SoC for IBEX

MPW-1 1.2k

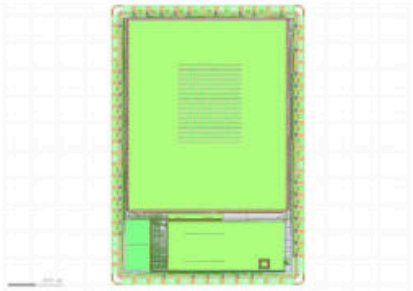


Caravel public

M. Shalan | http://efabless.com

NFive32-Based SoC to validate several open-source projects and IPs.

MPW-1 1.4k

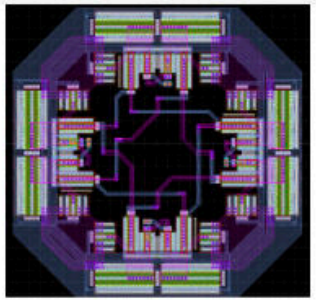


MorphleLogic public

Merik Voswinkel | http://www.fiberhood.org

A test-wafer for testing Mophle Logic reconfigurable hardware for SKY130.

MPW-1 SKY130 1.4k

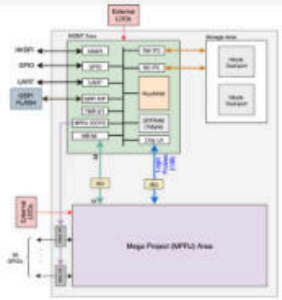


caravel_amsat_txrx_ic public

Thomas Parry | N/A

Amatuer Radio Satellite Transceiver (SKY130) - Caravel Submission

MPW-1 SKY130 2.8k



Softshell public

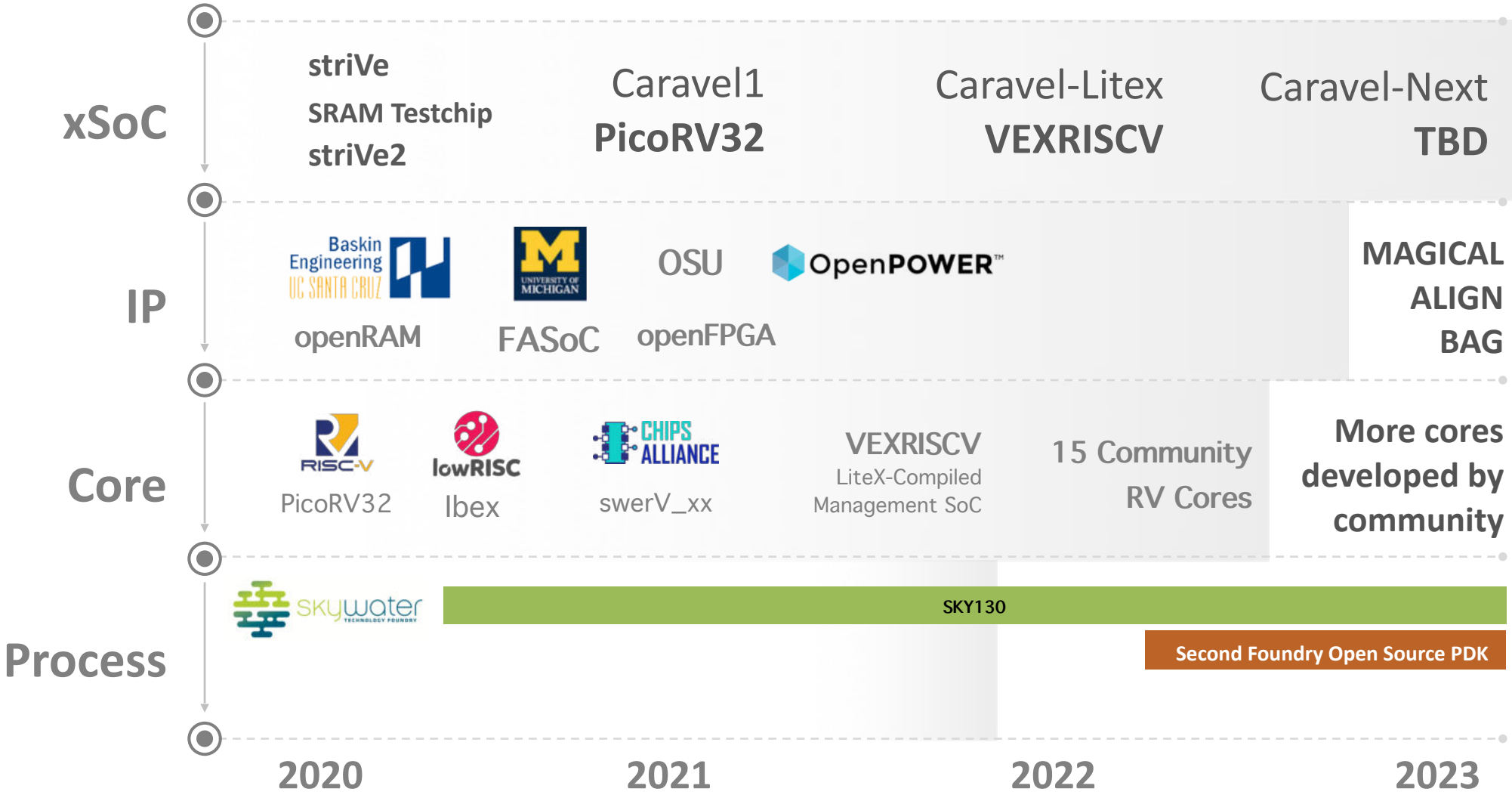
Harrison Pham | https://harrisonpham.com/

Multicore MCU for implementing software defined peripherals.

MPW-1 SKY130 1.7k

Select Open Source Designs

OPEN SOURCE ECOSYSTEM AT WORK



efabless.com

How do we simplify chip design? **#5**

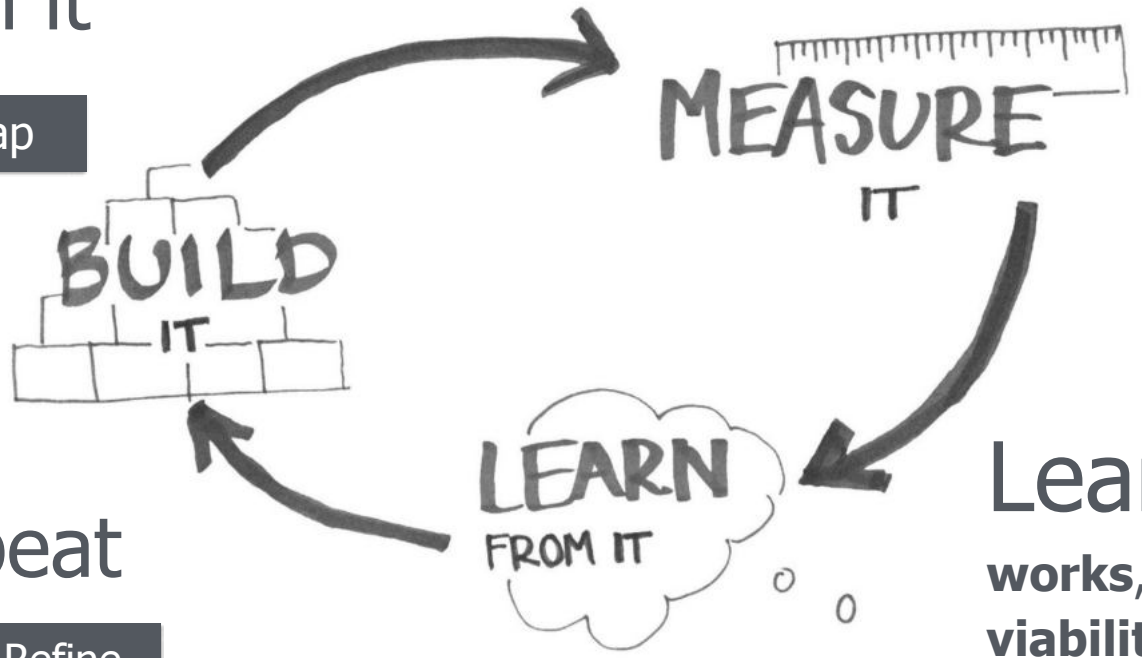
OK - sounds good so far

but … manufacturing cost $$

Enable —Fail fast, learn and repeat

1 Design it

Quick & Cheap



Test It **2**

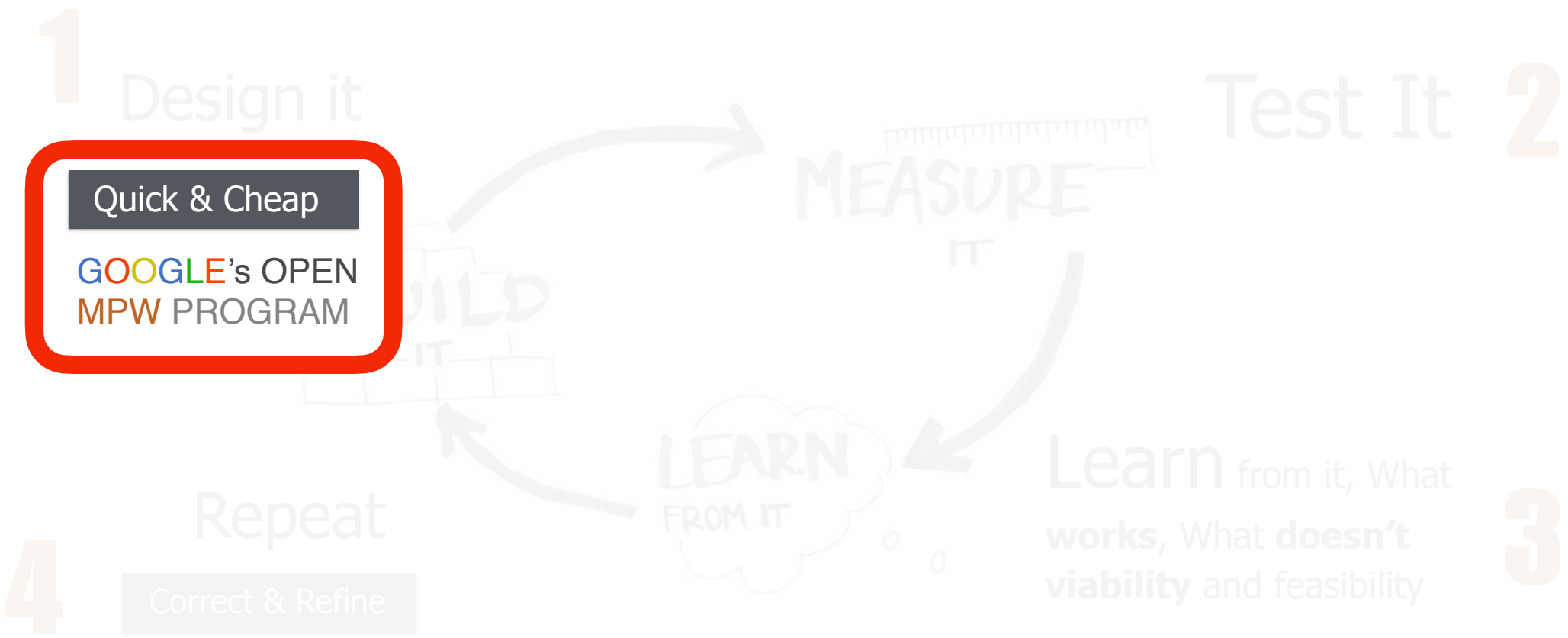
Learn from it, What **works**, What **doesn't**
viability and feasibility **3**

4 Repeat

Correct & Refine

efabless.com

Enable —Fail fast, learn and repeat



Quick & Cheap

GOOGLE's OPEN
MPW PROGRAM

efabless.com

GOOGLE's OPEN MPW PROGRAM

efabless.com
Sponsored by Google

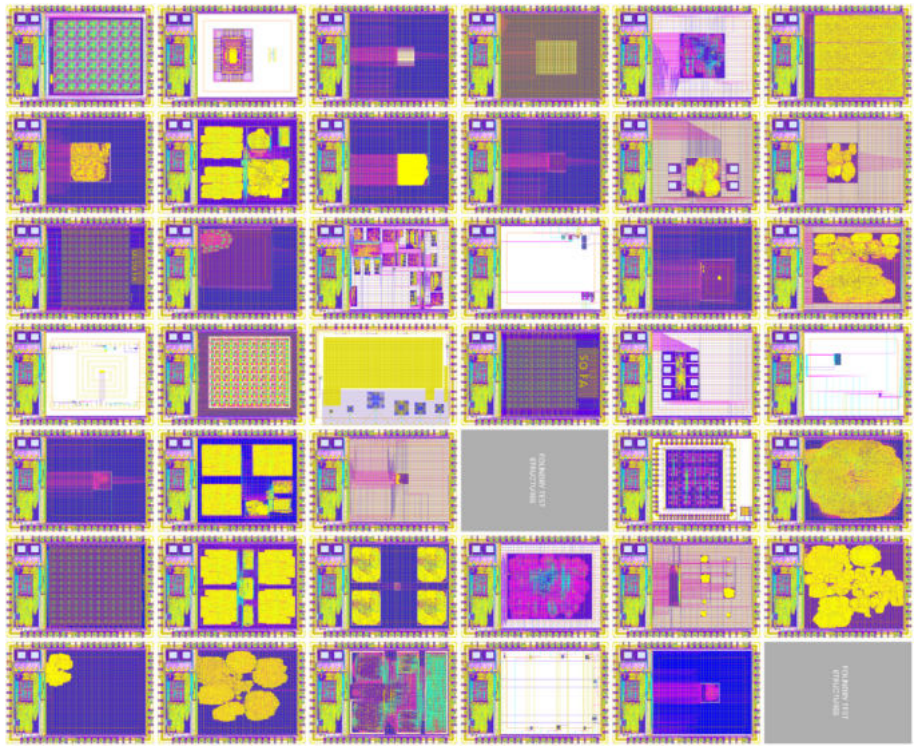
- **Google** is funding **4** manufacturing runs in **2022** - minimum of **40** designs each
- Participants use an Harness SoC (Caravel) with ***10mm2 open area***
- SKY130 Open Source Digital & Analog Design Tools are available
- Participants get ***5 dev boards + 300 WCSP-packaged parts***
- All designs must be public and under an ***open source license***
- All designs must contain information & files to ***reproduce the work***
- Participants are strongly encouraged to try new ideas, ***take risks and iterate***
- All skill and experience levels are welcome to participate

Start here https://ef.link/gmpw

Join the community at https://ef.link/chat

efabless.com

The first shuttle was overbooked: 45 designs submitted in 30 days!



Open MPW Shuttle Program

efabless.com

Sponsored by Google

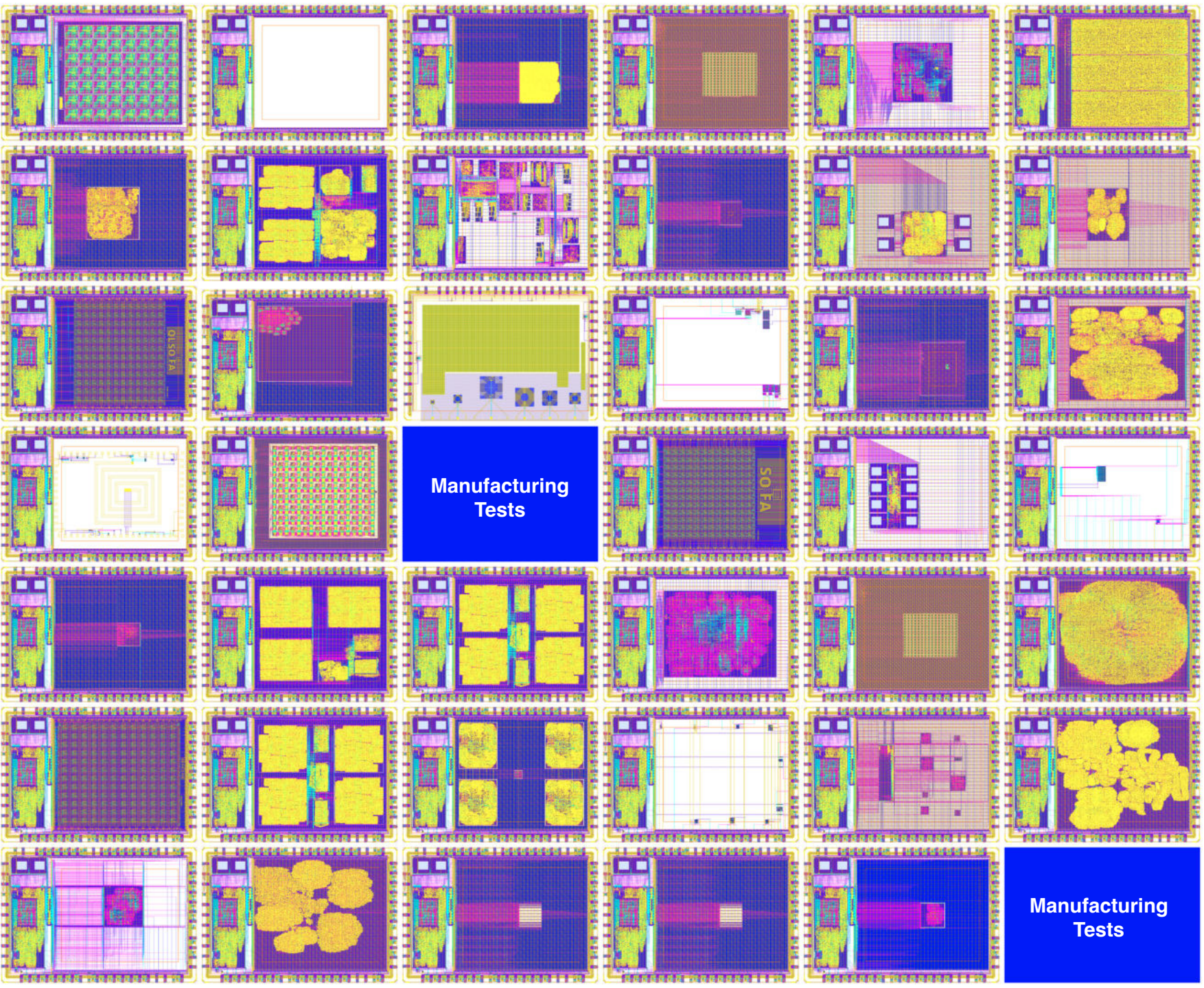
DESIGN TYPES

- 9 x Open processor cores
- 9 x SoC's
- Crypto-currency Miner
- Robotic App Processor
- Amateur Satellite Radio Transceiver
- 7 x Analog/RF
- 5 eFPGA's

MPW ONE

See Projects Here: https://efabless.com/projects/shuttle_name/MPW-1

efabless.com



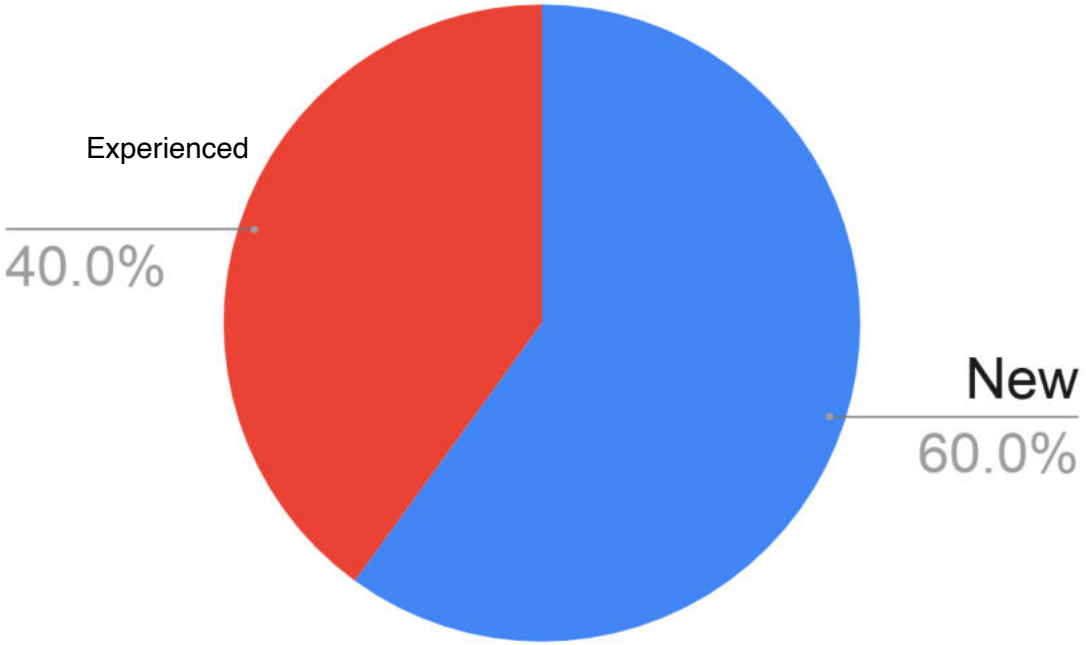
DESIGN TYPES

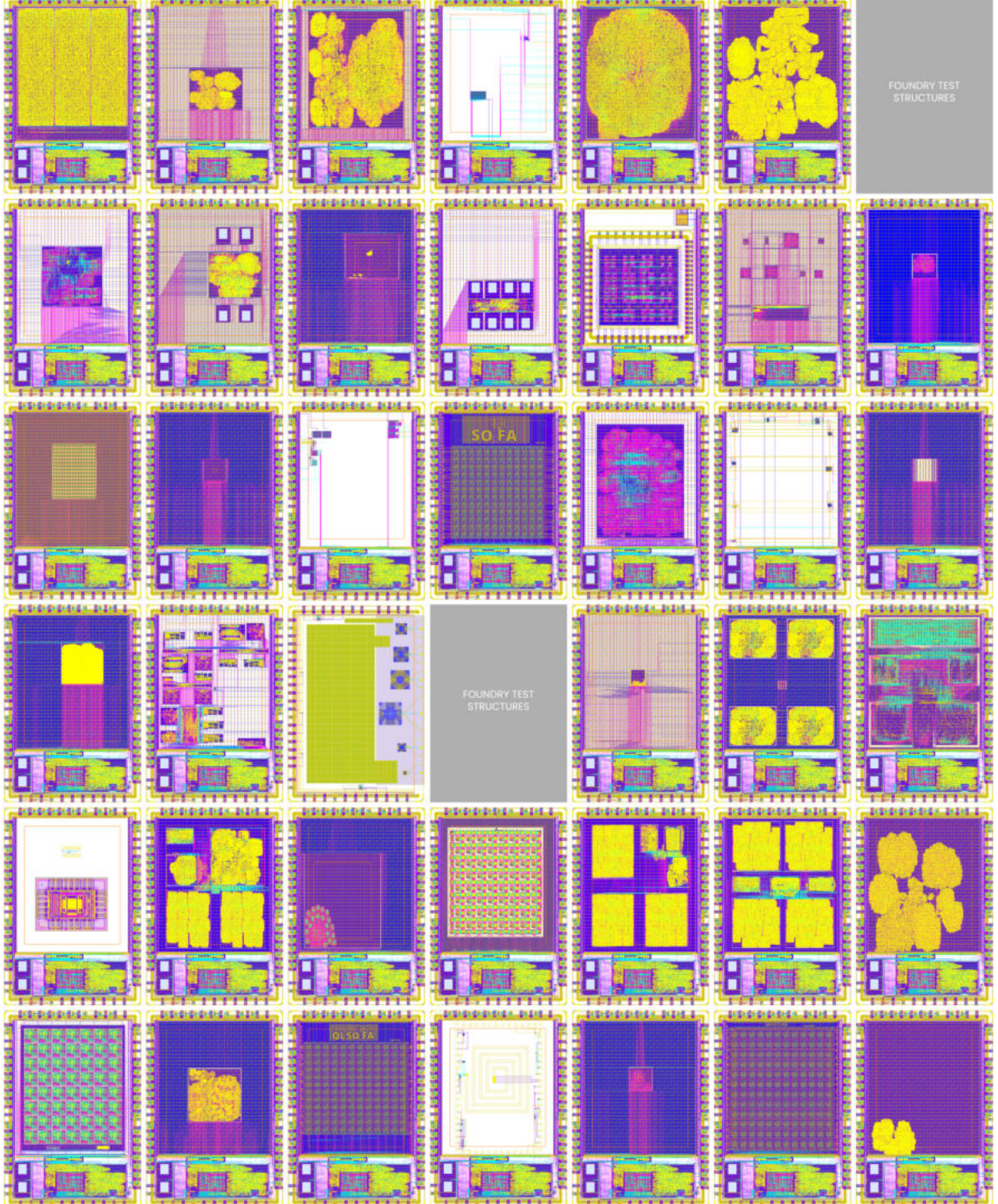
- 9 x Open processor cores
- 9 x SoC's
- Crypto-currency Miner
- Robotic App Processor
- Amateur Satellite Radio Transceiver
- 7 x Analog/RF
- 5 eFPGA's

COMPANIES

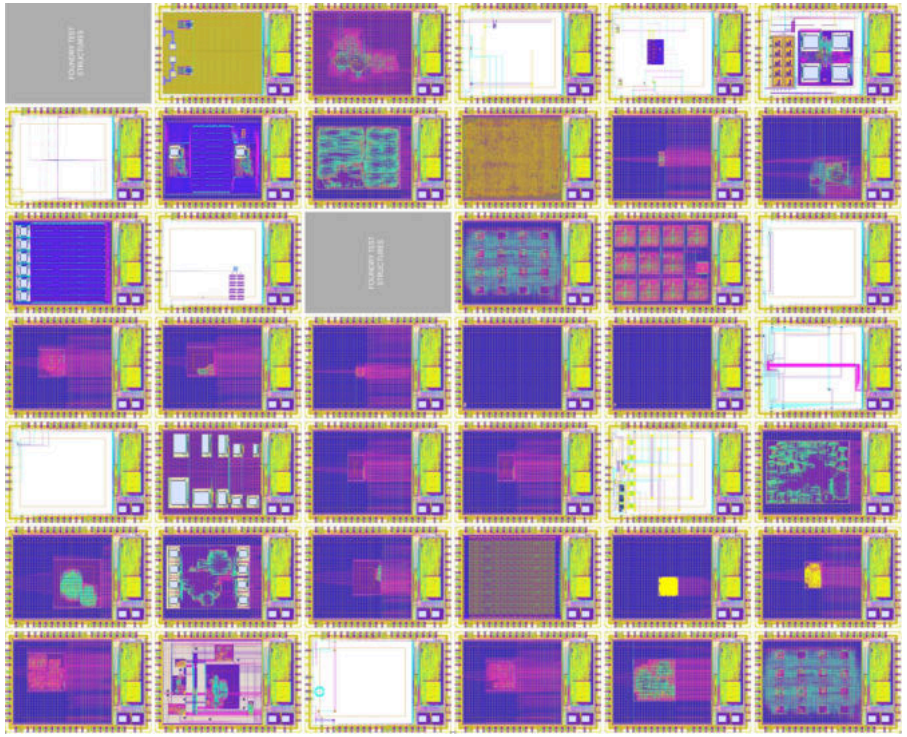
- IBM: OpenPOWER - MicroWatt
- QuickLogic - eFPGA
- Antmicro
- Western Digital - Swerv-EL2
- EFabless
- SpinMemory

60% by first time designers!





And so was the second:
56 designs submitted
in 30 days!



Open MPW Shuttle Program

efabless.com

Sponsored by Google

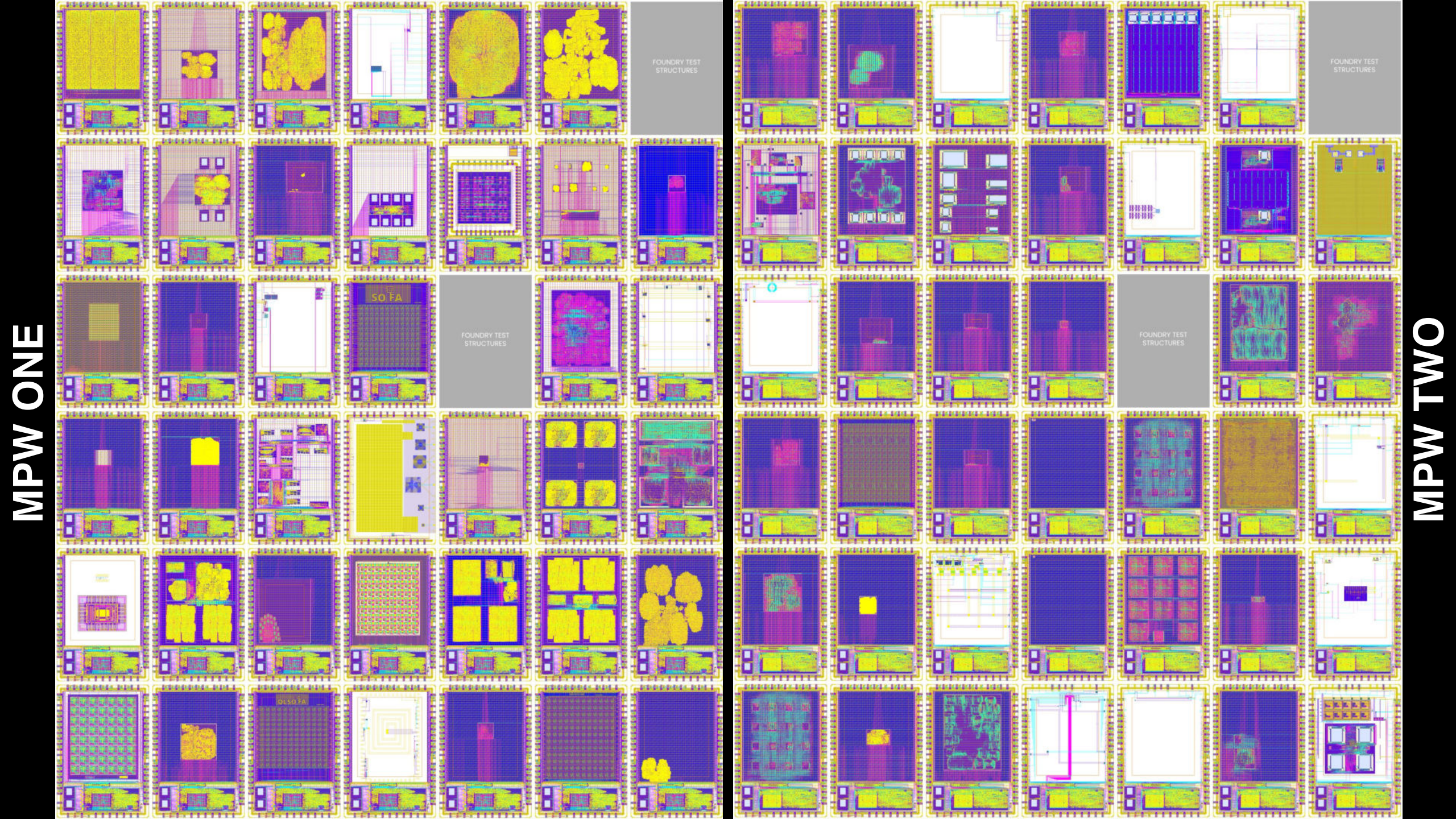
DESIGN TYPES

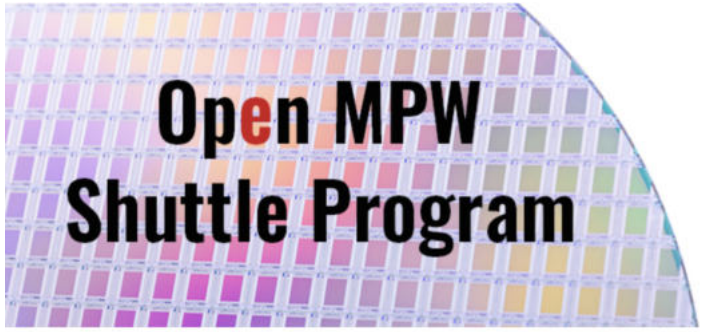
- 11 x Open processor cores
- 11 x SoC's
- Crypto-router
- T2D Converter - LIDAR
- Multi-project harness for Caravel x 16
- 17 x Analog/RF
- 2 eFPGA's

MPW TWO

See Projects Here: https://efabless.com/projects/shuttle_name/MPW-2

efabless.com


MPW ONE
MPW TWO
FOUNDRY TEST STRUCTURES
FOUNDRY TEST STRUCTURES
FOUNDRY TEST STRUCTURES
FOUNDRY TEST STRUCTURES
SO FA
OLSO FA



efabless.com

Sponsored by Google

WELCOME TO THE EFABLESS OPEN MPW SHUTTLE PROGRAM

Universities Put Fabrication into Courses and Drive Research and Early Innovation

Companies Advance and Showcase their Innovations

efabless.com

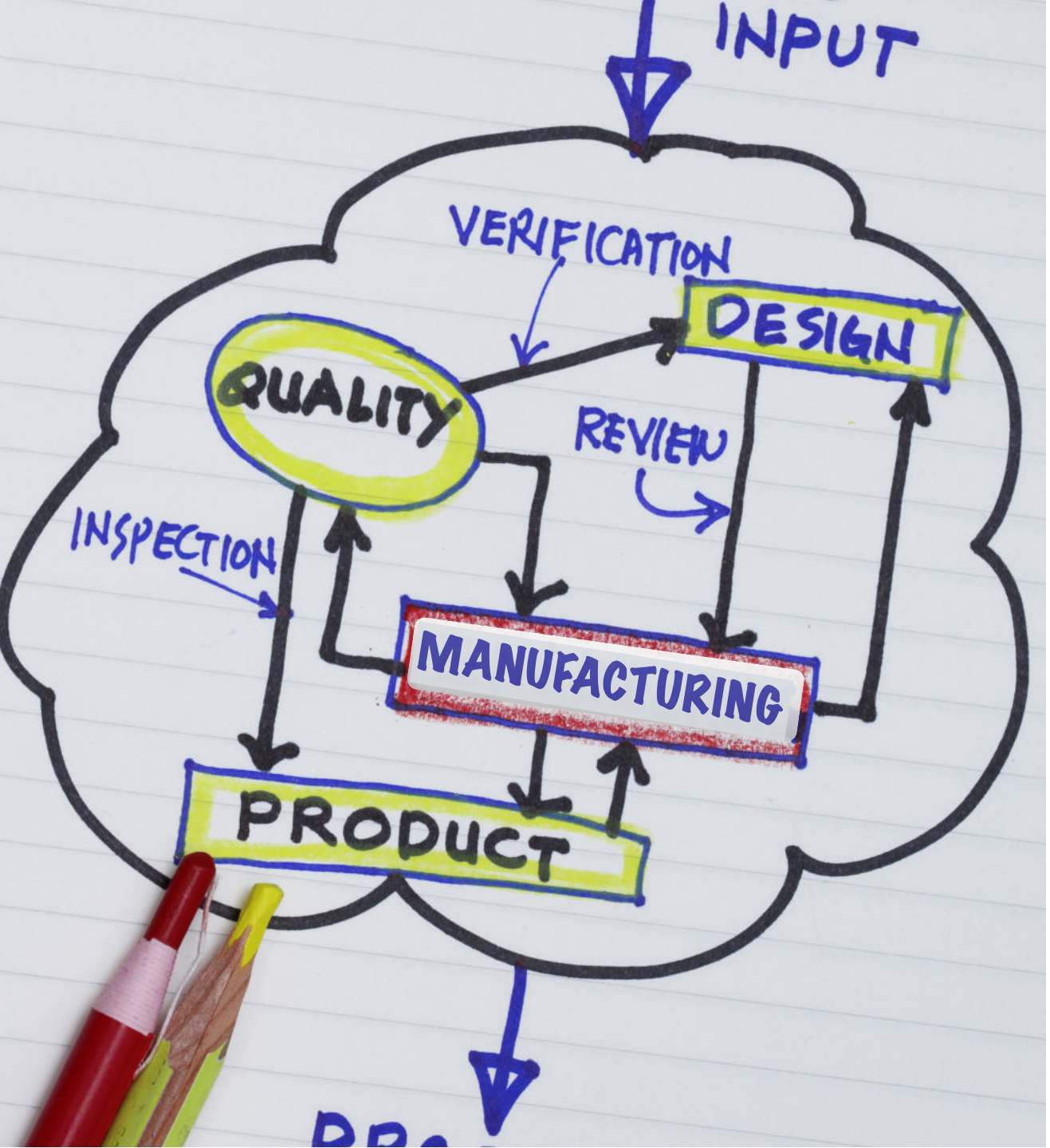
OpenMPW Project Submissions

Always Overbooked

45	56	52	55	77
MPW-1	MPW-2	MPW-3	MPW-4	MPW-5

https://efabless.com/projects

efabless.com

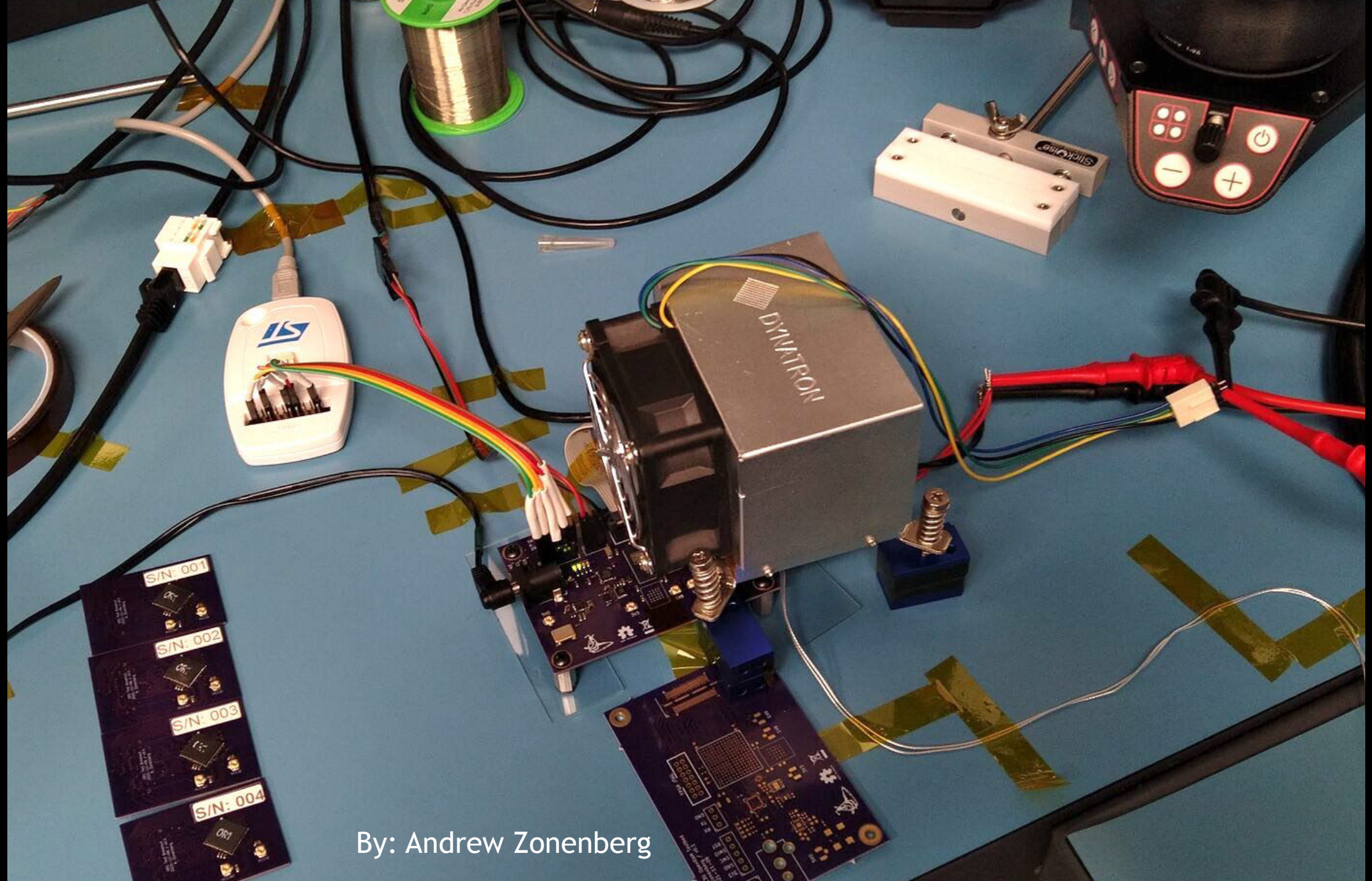

INPUT
VERIFICATION
DESIGN
QUALITY
REVIEW
INSPECTION
MANUFACTURING
PRODUCT


The Community
At Work

SRAM Characterization

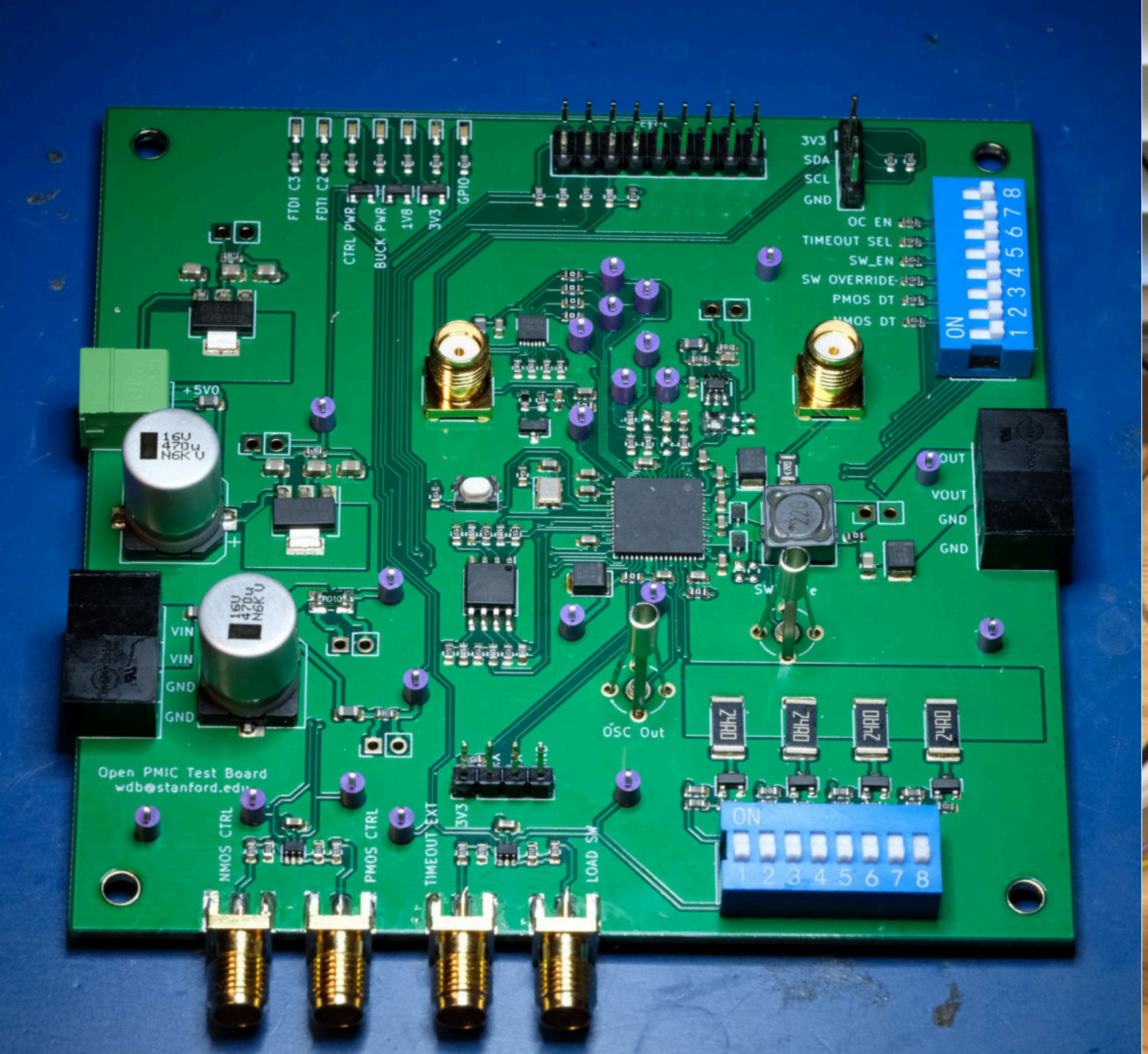
By: Andrew Zonenberg

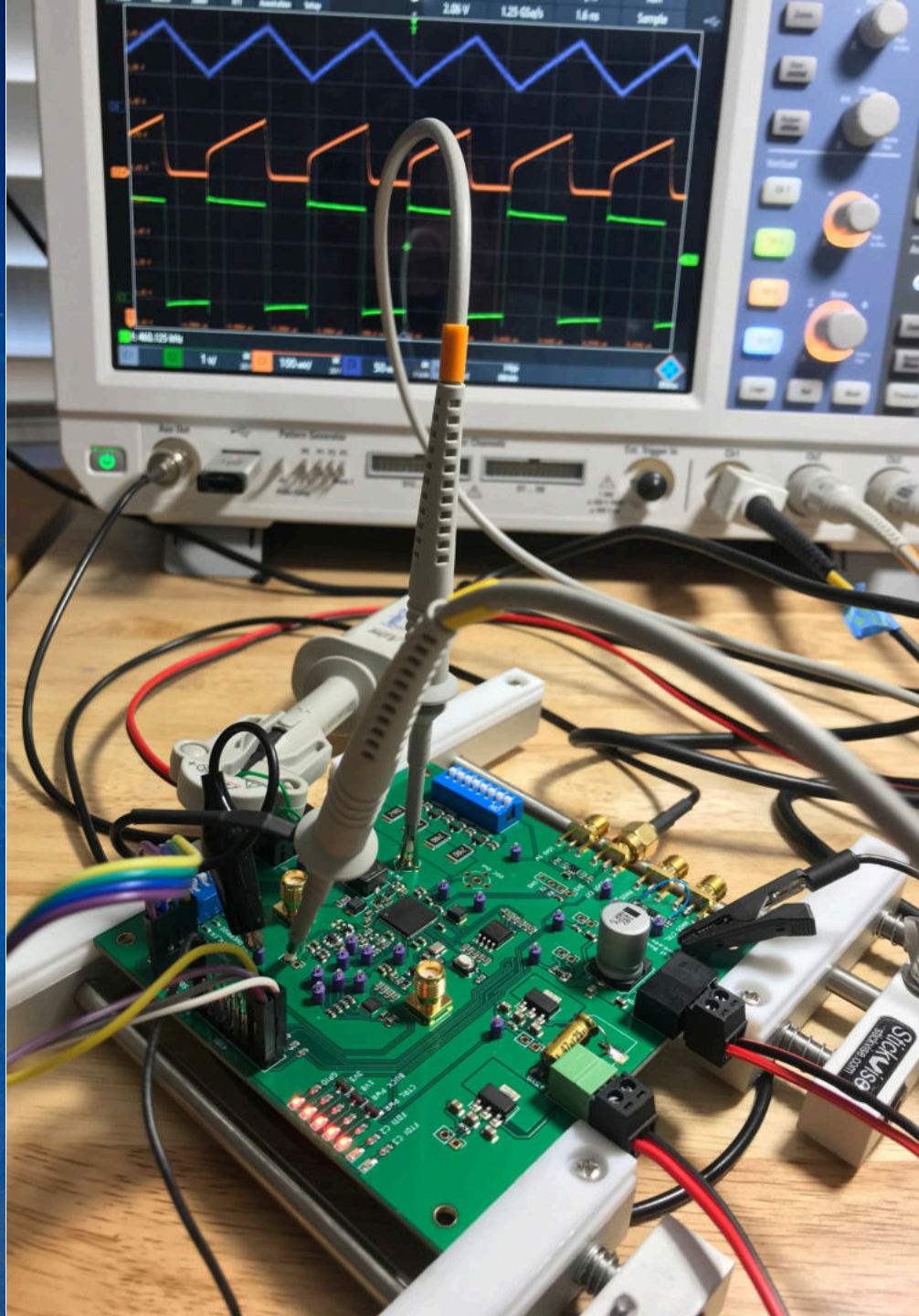
SRAM Characterization



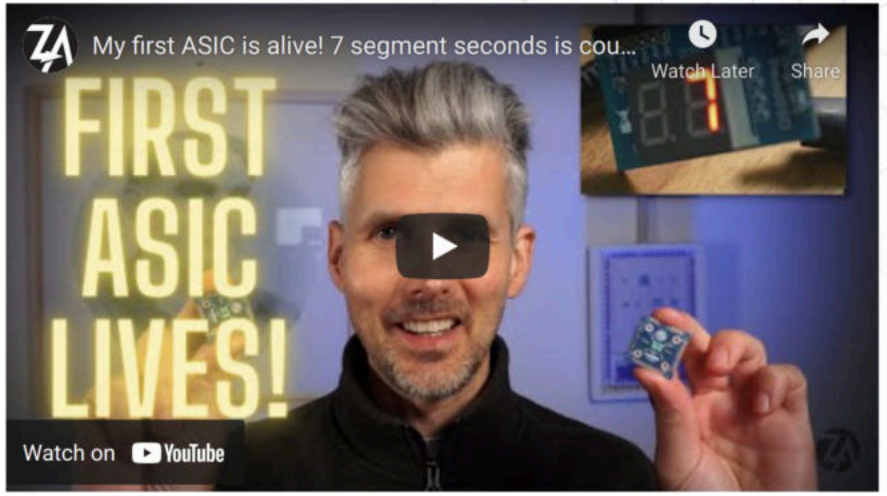
By: Andrew Zonenberg

Temperature Control

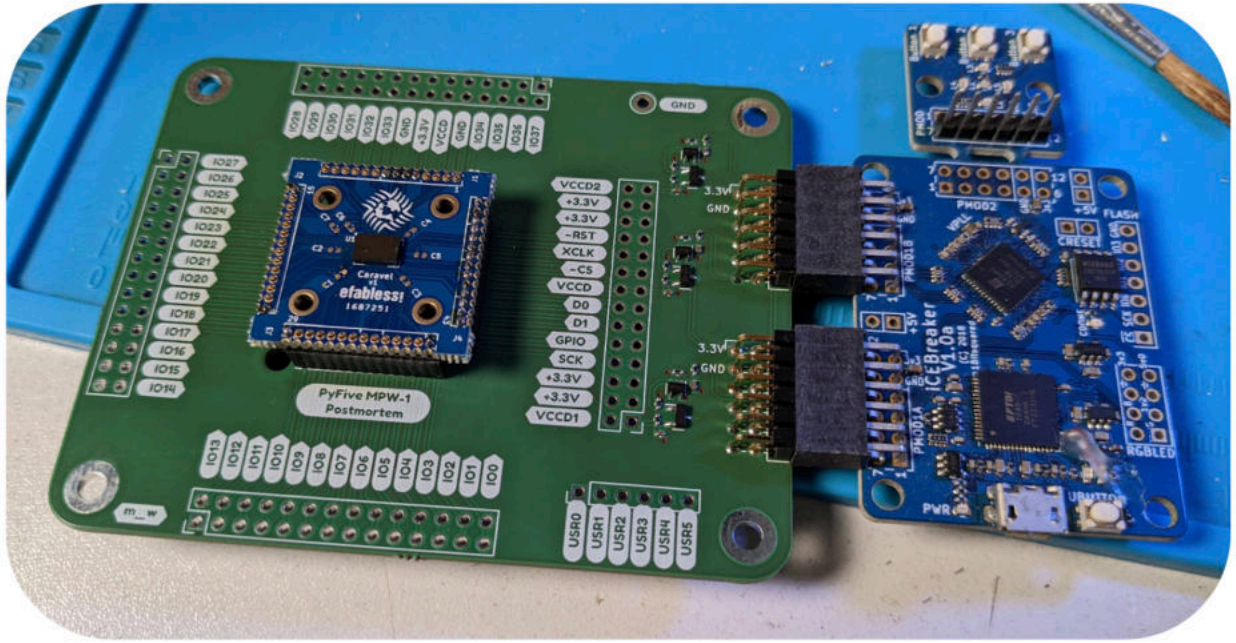

FTDI C3
FDTI C2
CTRL PWR
BUCK PWR
1V8
3V3
GPIO
3V3
SDA
SCL
GND
OC EN
TIMEOUT SEL
SW_EN
SW OVERRIDE
PMOS DT
NMOS DT
ON
1 2 3 4 5 6 7 8
+5V0
16U
470u
N6K U
VIN
VIN
GND
GND
OUT
VOUT
GND
GND
OSC Out
74HC
Open PMIC Test Board
wdb@stanford.edu
NMOS CTRL
PMOS CTRL
TIMEOUT EXT
3V3
LOAD SW
ON
1 2 3 4 5 6 7 8



- www.zerotoasiccourse.com/post/mpw1-bringup/
- github.com/mattvenn/mpw1-bringup



youtu.be/f_G5ad8SbHo



bit.ly/cicc22-edu-goog

Slide provided by: Tim Ansell

efabless.com

All my ASIC designs for Google MPW1 are working!

Zero To ASIC Course

1.1K views • 1 month ago

youtu.be/IdOvywOSSmI

bit.ly/cicc22-edu-goog

Slide provided by: Tim Ansell

Woowzaaa!!
I'm Caravel !!

bit.ly/cicc22-edu-goog

efabless.com

Volodymyr Pikhur @vpikhur · 15h

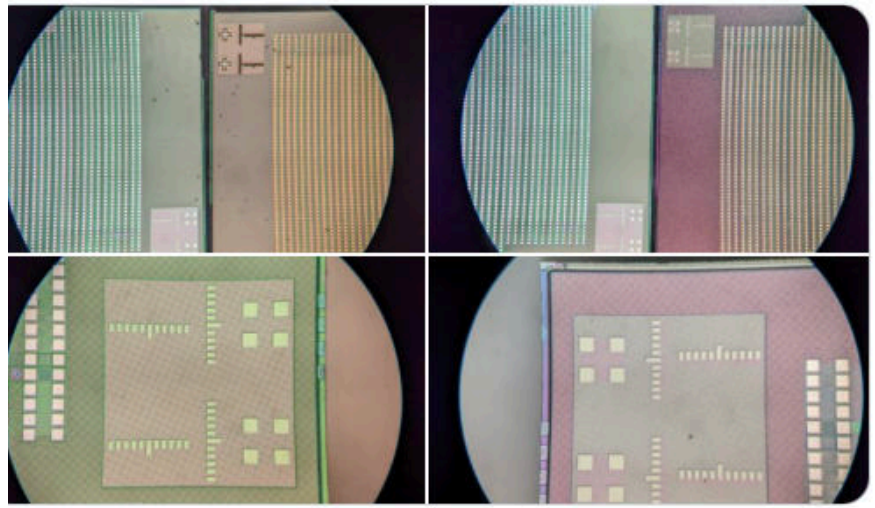
Replying to @vpikhur

Loaded 10 samples into RIE (reactive ion etcher) to strip top polyimide layer. I use a 50/50 mix of oxygen and argon gas.

1 1 4

olodymyr Pikhur @vpikhur · 15h

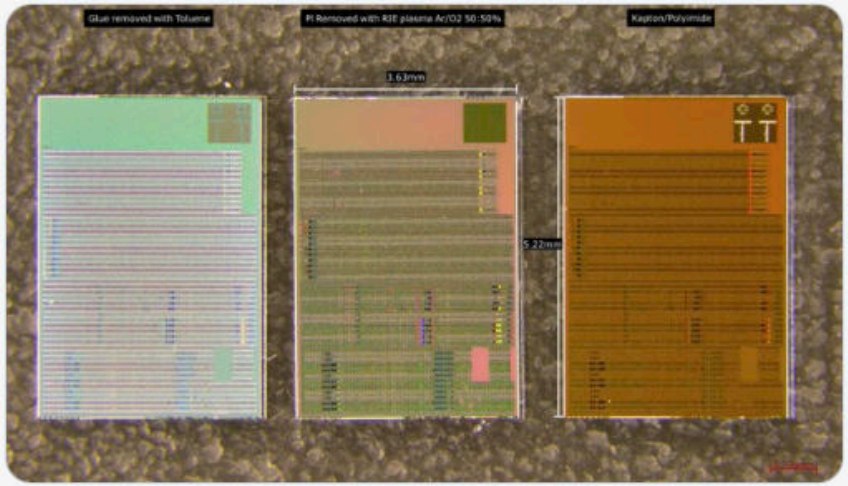
ter polyimide is removed there is adhesive/glue layer remaining. Adhesive n't be removed with normal solvents such as acetone or isopropyl cohol. Very non-polar solvent such as Toluene does the job.



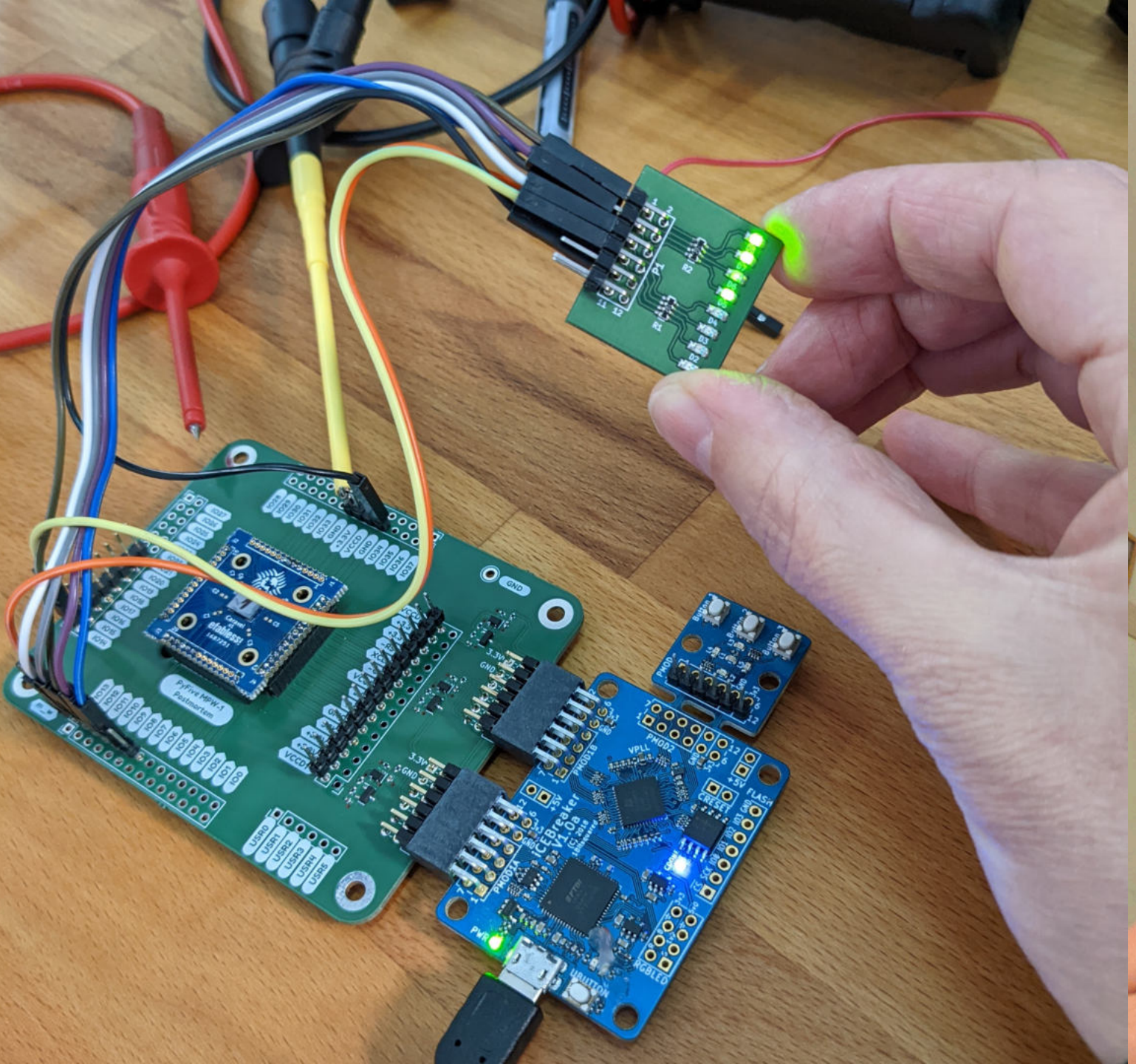
1 4 8

Volodymyr Pikhur @vpikhur · 15h

All 3 under stereo microscope with approximate die dimensions.



1 1 6


iCEBreaker
V1.0a
PMOD1A
PMOD1B
PMOD2
PMOD3
VPLL
CRESET
FLASH
RGBLED
USER0
USER1
USER2
USER3
USER4
USER5
GND
3.3V
+5V


MPW^2

github.com/mattvenn/
multi_project_tools

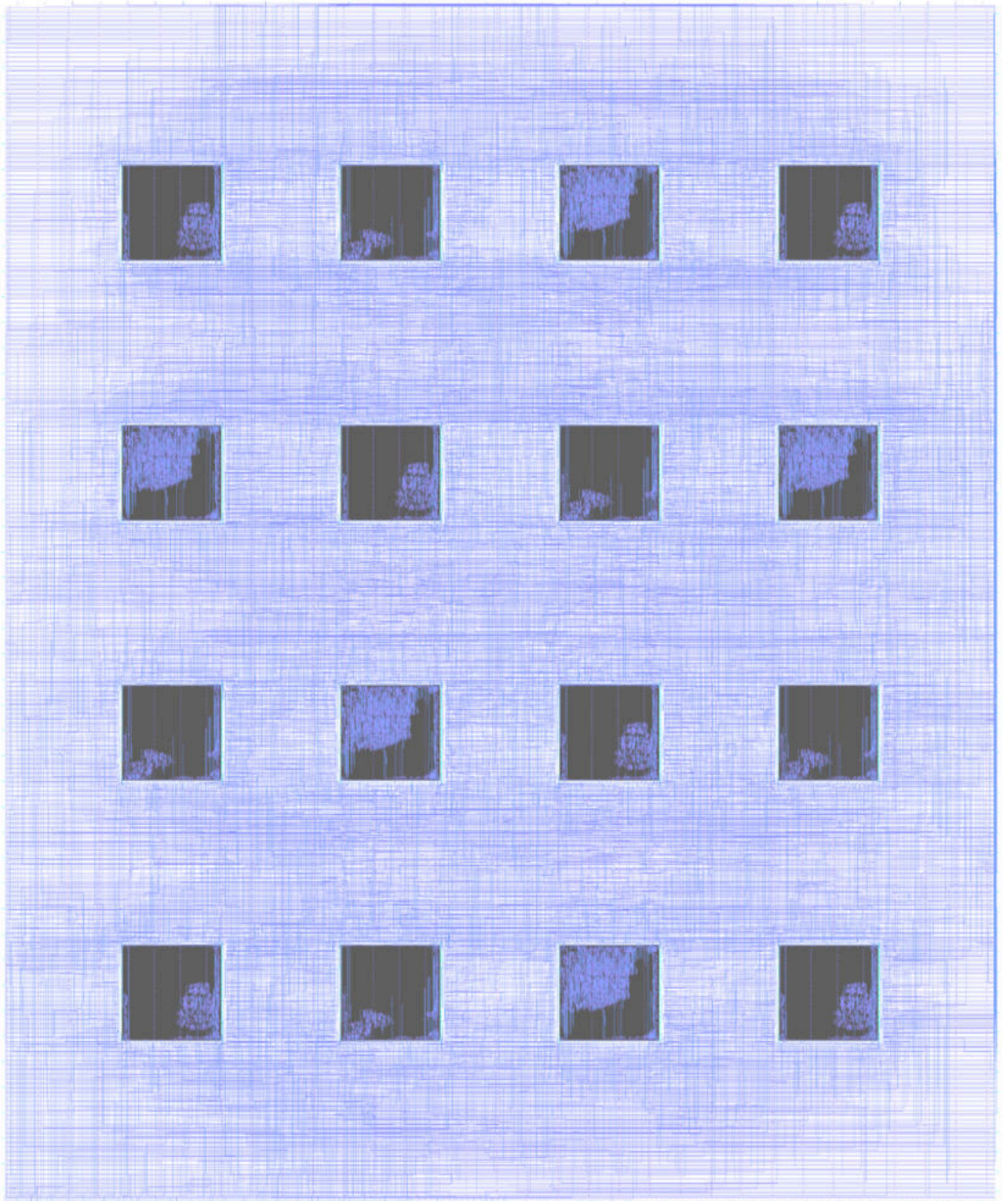
Compatible with

Open MPW *or* chipIgnite
Programs

16 projects in one slot

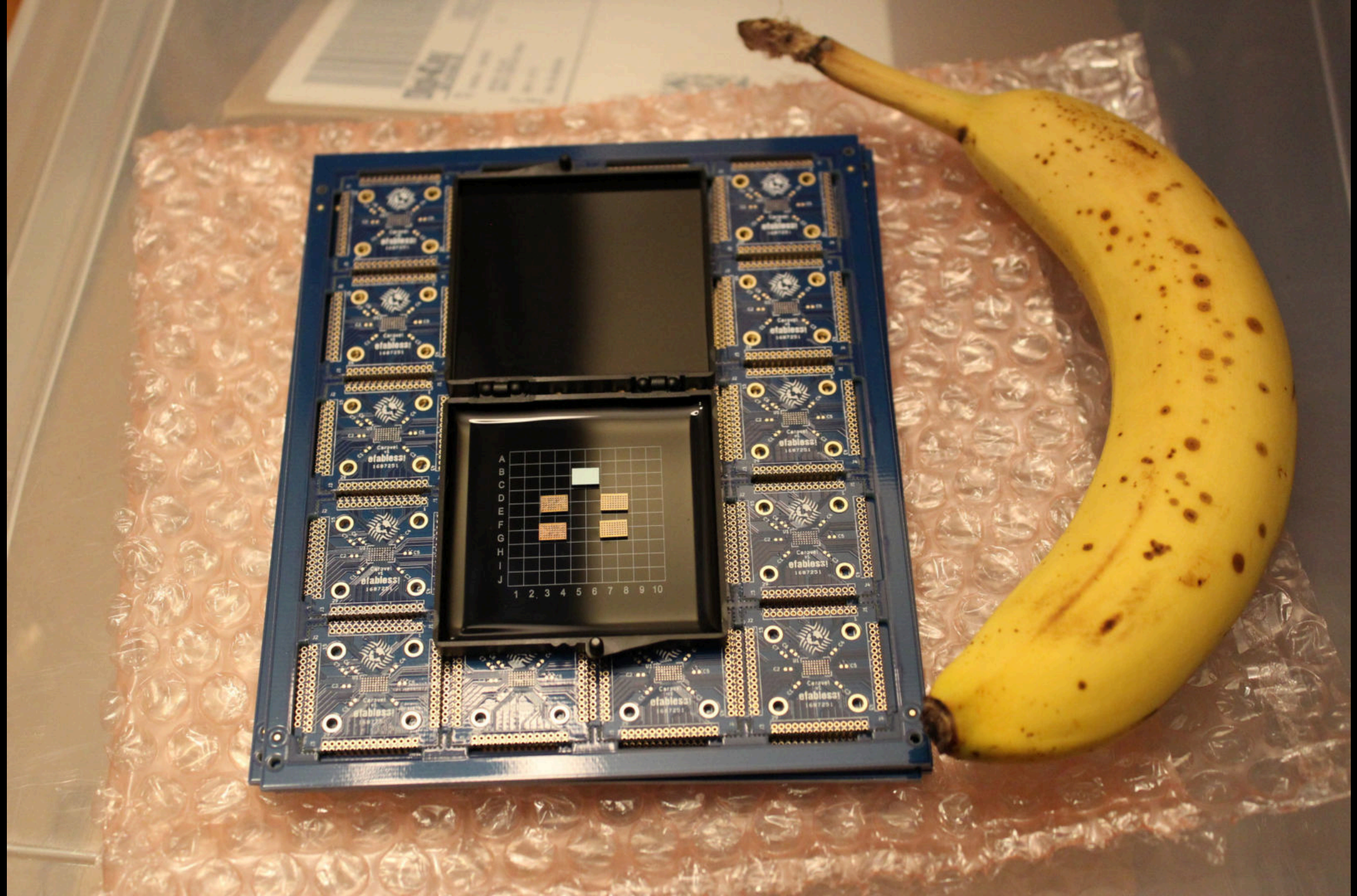
100 ICs ÷ 16 = ~5 ICs each

$9,750 ÷ 16 = ~$610 USD



tansell@google.com

j.mp/suny22-goog


A B C D E F G H I J
1 2 3 4 5 6 7 8 9 10

BUT ....

What if I do not want to open source my design?

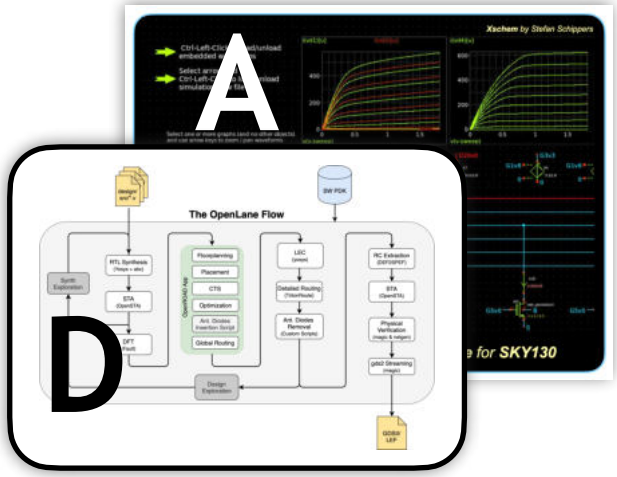
I would like to guarantee my spot on the run.

I need it on my own schedule.

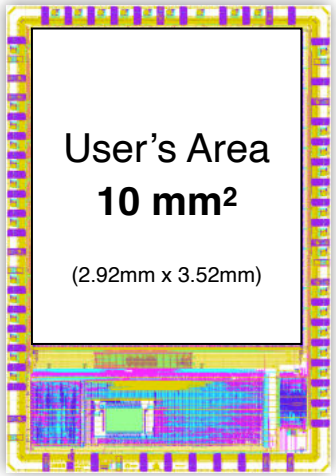
chipIgnite

by efabless.com

OS EDA Digital & Analog



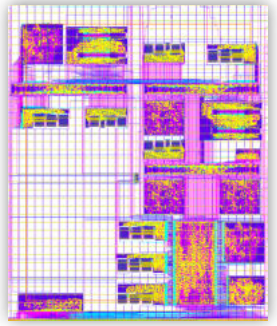
+



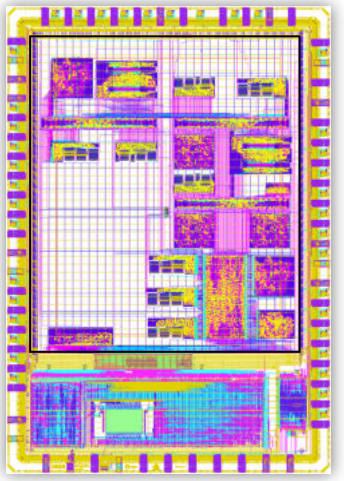
CARAVEL

+

User Design



+



CARAVEL + User Design

MANUFACTURING

chipIgnite

Rapid IC Creation

Start Here

https://ef.link/start-digital

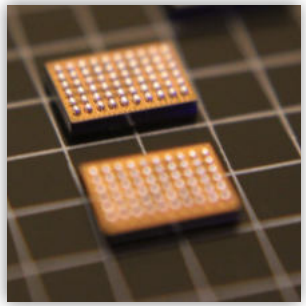
https://ef.link/start-analog

Software (FOSS)

+

5 Dev Boards

+



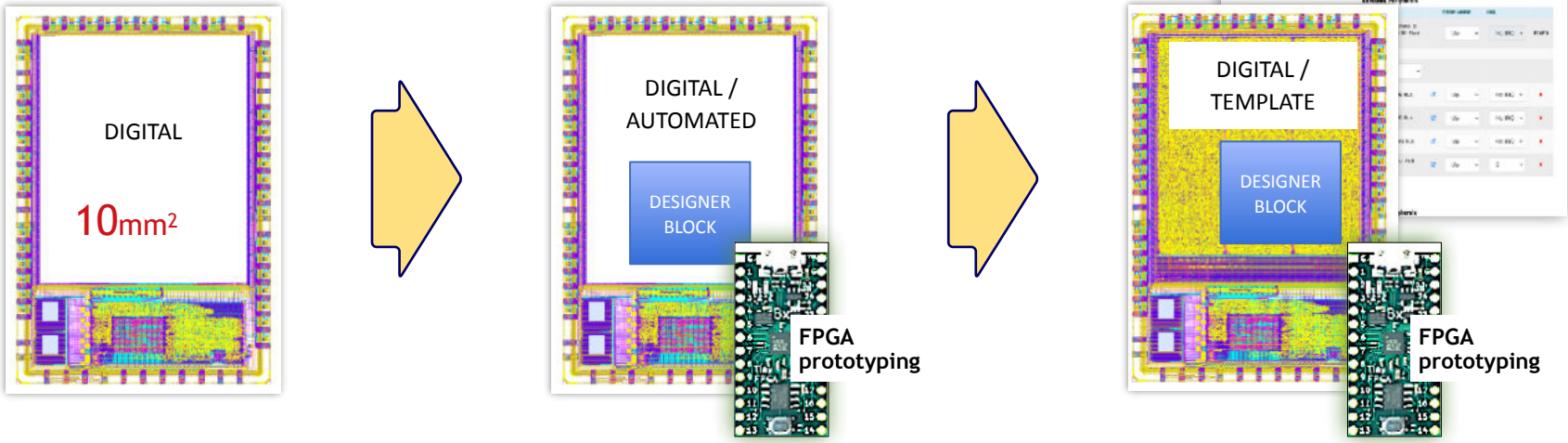
300 WCSP Parts

efabless.com

chipIgnite OPTIONS

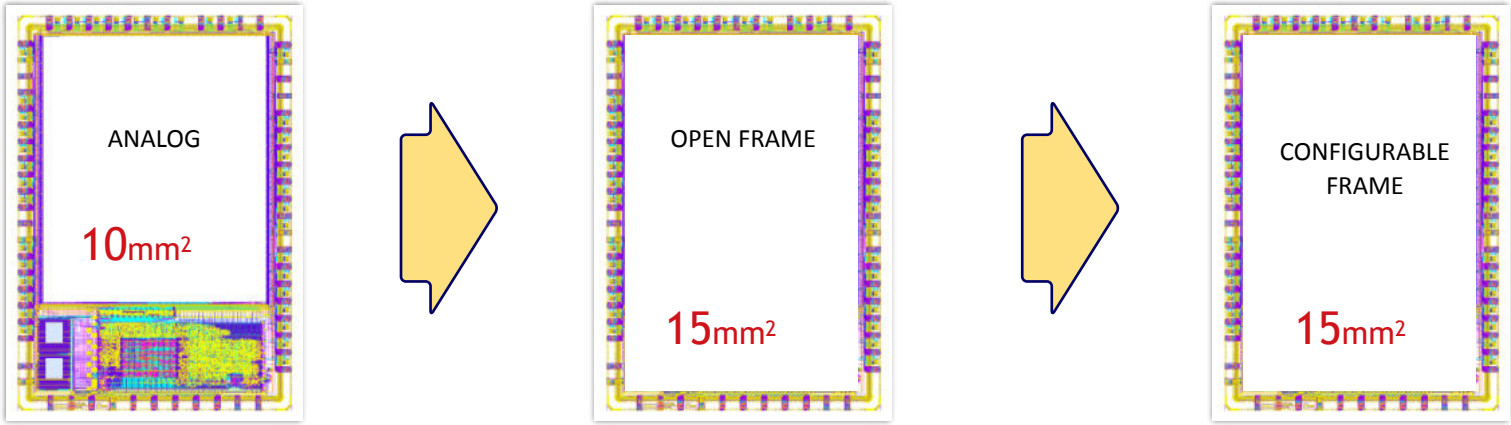
LOW COMPLEXITY

IP Development
Digital & low frequency analog
Enabling larger designer base



HIGH COMPLEXITY

IP Development
Complete Custom ASIC
Analog & Digital
Expert designer base



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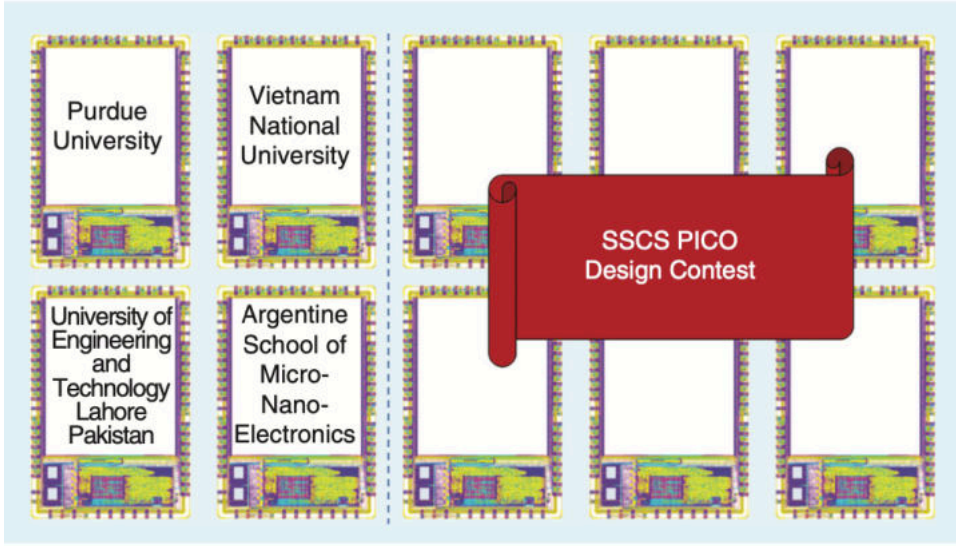
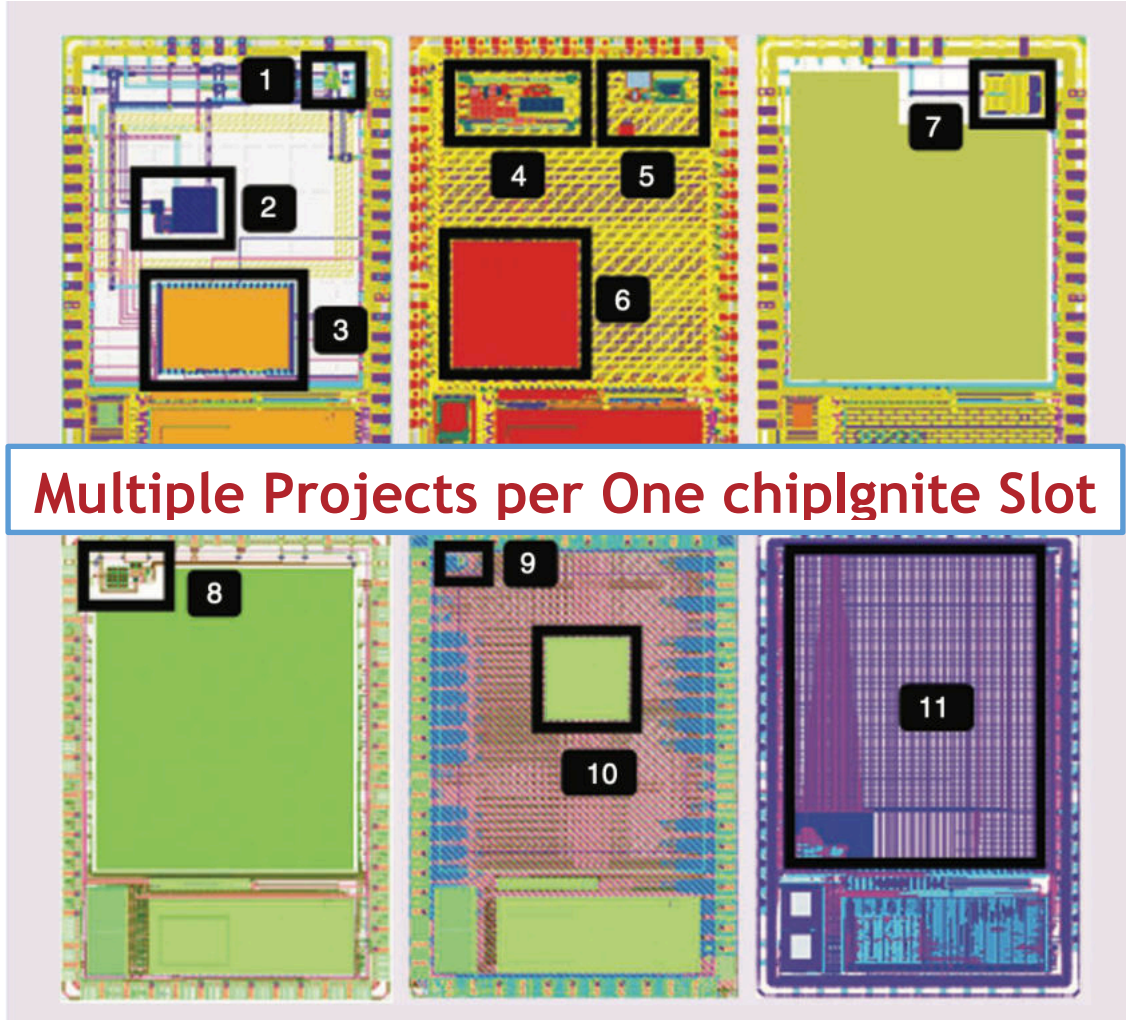
IEEE SOLID-STATE CIRCUITS SOCIETY™
IC Innovation

IEEE - PICO PROGRAM 2021

POWERED BY
chipIgnite
Rapid IC Creation



Link to Article SSCS Magazine Article - NOV 2021



Link to Article SSCS Magazine Article - JAN 2022

efabless.com

chipIgnite CUSTOMERS

POWERED BY chipIgnite Rapid IC Creation

IEEE SOLID-STATE CIRCUITS SOCIETY™ IC Innovation

1

Stanford **EE272** Design Course

Three more universities …

High Schools coming in June 2022

2

SSCS "**PICO**" Open Source Design Contest:

56+ submitted designs

10 will tape out at Efabless

https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program
https://efabless.com/projects/project_definition/SSCS-21

3

Open Source FPGA Foundation global program innovation among university students

2 **ChipIgnite** Slots per University

Turkey, Pakistan, India, Australia

4

Startups

Using chipIgnite as their proof-of-concept or low volume production

efabless.com

IEEE SOLID-STATE CIRCUITS SOCIETY™ IC Innovation

OPEN SOURCE CHIPATHON - 2022

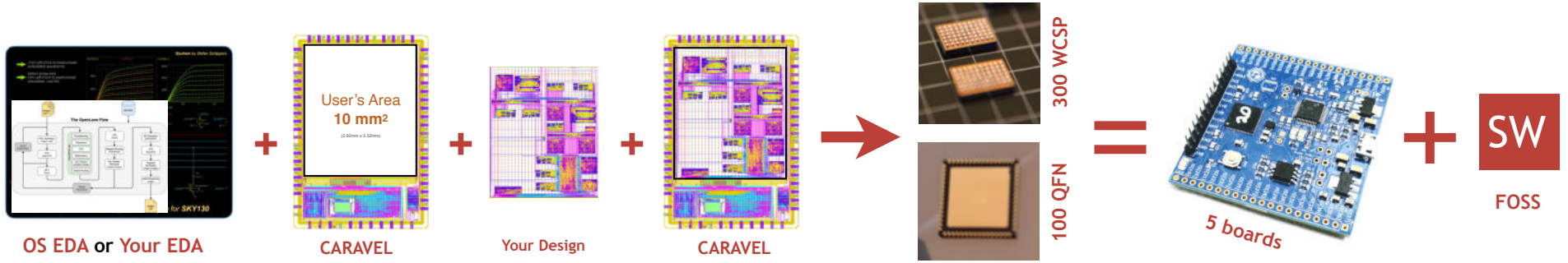
POWERED BY chipIgnite Rapid IC Creation

Low power 130nm CMOS 10 Bit SAR ADC	https://platform.efabless.com/projects/851
Analog Baseband Circuitry For 60GHz Receivers	https://platform.efabless.com/projects/855
SPATIAL SD ADC	https://platform.efabless.com/projects/872
ENCRYPTED LSB STEGANOGRAPHY WITH AES ACCELERATOR	https://platform.efabless.com/projects/873
CMOS Bandgap Voltage Reference Design	https://platform.efabless.com/projects/874
On Chip DC-DC Converter with Fast Transient Response	https://platform.efabless.com/projects/879
DC-DC Buck Converter for efficient CubeSat EPS	https://platform.efabless.com/projects/881
CMOS Power Oscillator Test Chip	https://platform.efabless.com/projects/882
Subthreshold SRAM	https://platform.efabless.com/projects/883
Self-Interference Cancellation Low Noise Amplifier	https://platform.efabless.com/projects/888
MATRIX MULTIPLIER FOR AI ON EDGE APPLICATIONS	https://platform.efabless.com/projects/889
ReRAM based DNN accelerator	https://platform.efabless.com/projects/904
Mix-Pix - A mixed signal circuit for smart imaging	https://platform.efabless.com/projects/916
60 GHz demonstrator chip	https://platform.efabless.com/projects/920
A compact batteryless low-startup boost converter	https://platform.efabless.com/projects/922
Sub-Sampling PLL targeting SerDes Applications	https://platform.efabless.com/projects/923
Radiation-Hardened-By-Construction Microcontroller	https://platform.efabless.com/projects/928
Mixed-Signal SoC for Nanopore-Based DNA Sequencing	https://platform.efabless.com/projects/933
Digitally Enhanced PLL	https://platform.efabless.com/projects/935
Novel boost converter for battery-powered IoT uses	https://platform.efabless.com/projects/939
System on Chip for the Next Pandemic	https://platform.efabless.com/projects/945
Electrochemical Water Quality Monitoring	https://platform.efabless.com/projects/951

efabless.com

WHAT IS?

chipIgnite
Rapid IC Creation



- Design using SkyWater SKY130 (130nm) rich process + std cells + IO cells
- Start from the Caravel Harness - **no cost** - book your slot for **$200**
- You *choose your licensing terms* for your design - by *default it's proprietary*
- The offered area (10mm2) is not just silicon area - *It is a framed house with plumbing and electricity - just bring your appliances*
- Cycle Time 95 days +/- depending on the package choice

Rapid Prototyping	**$9,750**	**100 QFN**	parts + 5 dev boards
Engineering Samples	**$9,750**	**300 WCSP**	parts + 5 dev boards
Low Volume Production	**$20,000**	1000 WCSP	parts + 5 dev boards

chipIgnite : GET STARTED

- chipIgnite Web Page
- Getting Started Video
- Project Template on Github
- Browse Previous Projects
- Join SkyWater PDK Slack Space - https://join.skywater.tools
- The OpenLane flow for digital PnR can be found at https://openlane.readthedocs.io
- The OpenROAD Project https://theopenroadproject.org/
- The documentation is at https://docs.skywater.tools
- Caravel documentation https://caravel-harness.readthedocs.io
- WOSET/ICCAD Workshop on EDA https://woset-workshop.github.io/WOSET2020.html

GET TO SILICON

https://efabless.com

CARRIER SOC HARNESS

caravel *noun*

Save Word

car·a·vel | \ ˈker-ə-ˌvel, ˈka-rə-, -vəl \

Definition of *caravel*

: any of several sailing ships

A small 15th and 16th century ship that has broad bows, high narrow poop, and usually three masts with lateen or both square and later sails.

Source: https://www.merriam-webster.com/dictionary/caravel