RISC-V Days Tokyo 2022 Spring

Creating a World where a 14-year-old Designs a Chip

Mohamed Kassem

Cofounder & CTO, EFABLESS.COM

mkk@efabless.com

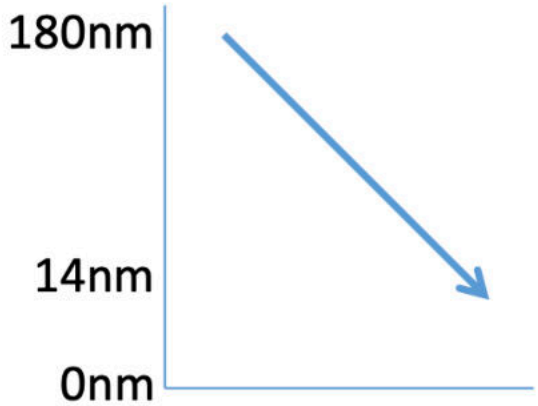
Why is it “hard” to design chips

Limited access to **knowledge**

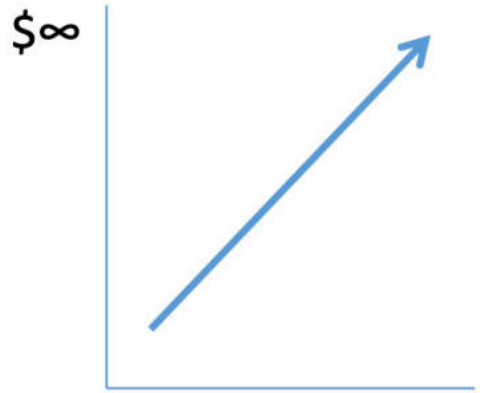
Limited access **technology**

Costly **manufacturing**

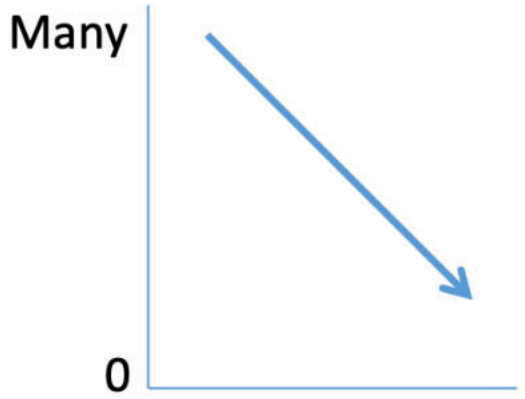
CHIP INDUSTRY TRENDS



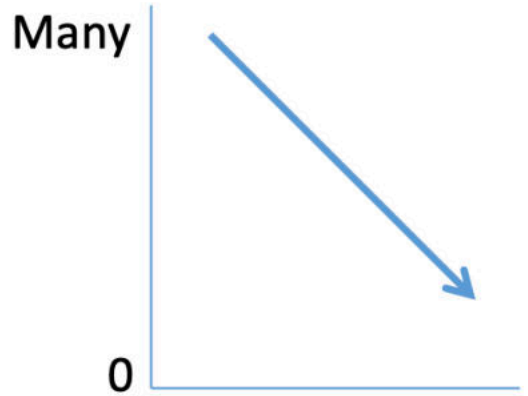
As Transistor Size Goes To Zero



Development Cost Goes to Infinity



Number of Customers Goes to Zero



Number of Designers Goes to Zero

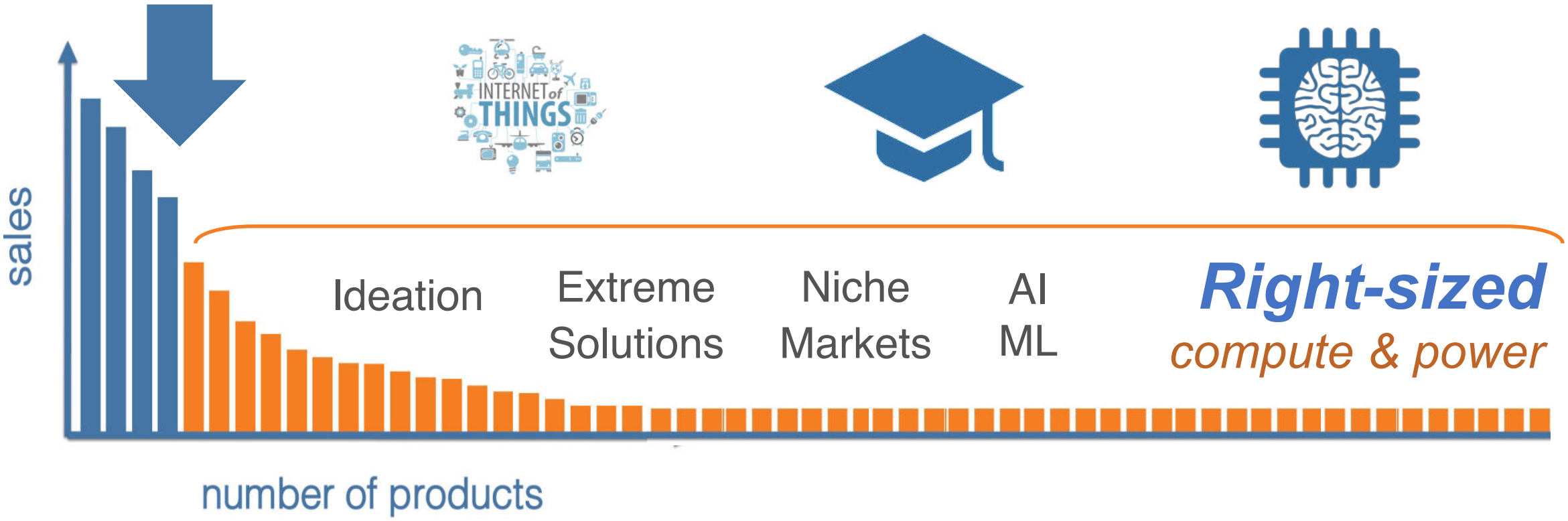
Source: Mike Noonen

WE NEED A 1000X PRODUCT DESIGNERS

Long-tail Innovation is required on a massive scale to meet demand

10,000's of Products

Markets Served By Traditional Methodology



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We need to

Simplify the process of **Chip creation** and open it **to Everyone**

How would we simplify chip design?

Think what **app stores** did

to software innovation.

***Simplified** (democratized)*

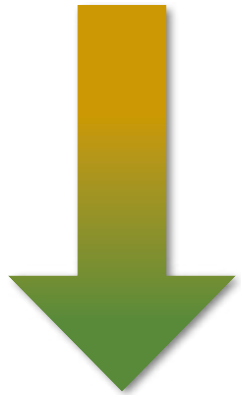
the **development tools**

the **business process**

the **connection to customers**

Think what **app stores** did to software innovation.

Thousands



At least

Millions

Including kids

***Simplified** (democratized)*

the **development tools**

the **business process**

the **connection to customers**

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Think that we apply the same approach to chip design

***Simplify** (democratize)*

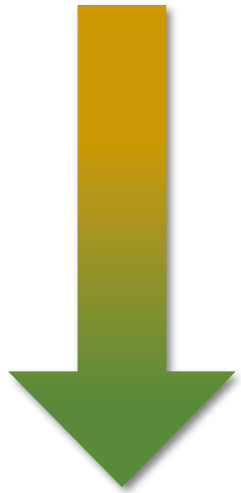
the **access** to chip design tools & PDK

the **business process**

the **connection to customers**

Think that we apply the same approach to chip design

Thousands



Simplify (democratize)

the **access** to chip **design tools** & PDK

the **business process**

the **connection to customers**

At least

Millions

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..... too complicated

1. Market Access — $$
2. Expertise — $$+Time
3. IP — $$+NDA
4. EDA Tools — $$+NDA
5. PDK — NDA
6. AFFORDABLE MFG/ASSY/TEST — $$

At least these **6** things must exist to create useful chips

YOU **CAN'T** BUILD A USEFUL **CHIP**

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….. still too complicated

1. Market Access — $$
2. Expertise — $$+Time
3. IP — $$+NDA
4. EDA Tools — $$+NDA
5. PDK — NDA
6. AFFORDABLE MFG/ASSY/TEST — $$

Partial solutions **don't work**

STILL **CAN'T** BUILD A USEFUL **CHIP**

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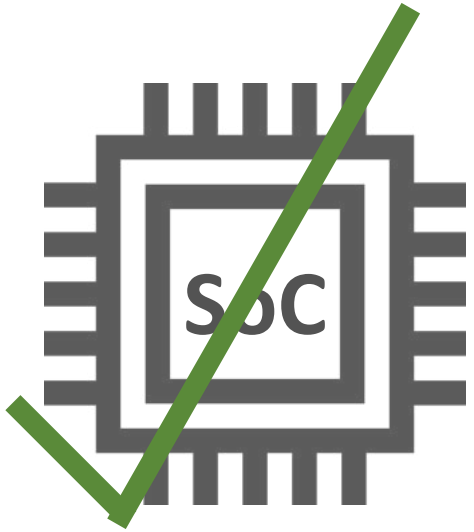
….. what we need …

1. **Market Access** — Open Online Marketplace for Chips Like the App Stores
2. **Expertise** — Open Community Collaboration Clusters of global teams
3. **IP** — No NDA or Access Fee Open Source or Obfuscated
4. **EDA Tools** — No Licensing Cost = Open Source Low Licensing Cost = Cloud-based
5. **PDK** — No NDA = Open Source or Obfuscated to protect IP
6. **AFFORDABLE** MFG/ASSY/TEST — No NDA = Open Source or Obfuscated to protect IP while enabling designers to use it

Must Solve for All Needs



CAN BUILD USEFUL **CHIPS**

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How do we simplify chip design? **#1**

Open access to technology PDK

No NDA, nothing to sign - it's Open Source

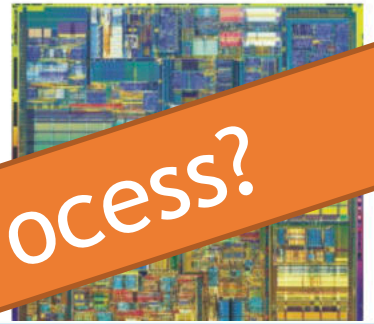
$ git clone https://github.com/google/skywater-pdk

—> *Technology information availability is **virtually limitless***

—> *Leading to **massive open collaboration***

—> *Skywater 130nm PDK*

Intel Chips



What do I do with a 130nm process?

13

2000

Initial clock speed:
1.5GHz

Transistors:
42 million

Manufacturing technology:
0.18 micron

2001
Intel® Xeon® processor

Initial clock speed:
1.7GHz

Transistors:
42 million

Manufacturing technology:
0.18 micron

15

2003
Intel® Pentium® M processor

Initial clock speed:
1.7GHz

Transistors:
55 million

Manufacturing technology:
90nm

16

2006
Intel® Core™2 Duo processor

Initial clock speed::
2.66GHz

Transistors:
291 million

Manufacturing technology:
65nm

410 million

Manufacturing technology:
45nm

47 million

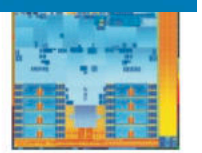
Manufacturing technology:
45nm

1.16 billion

Manufacturing technology:
32nm

1.4 billion

Manufacturing technology:
22nm



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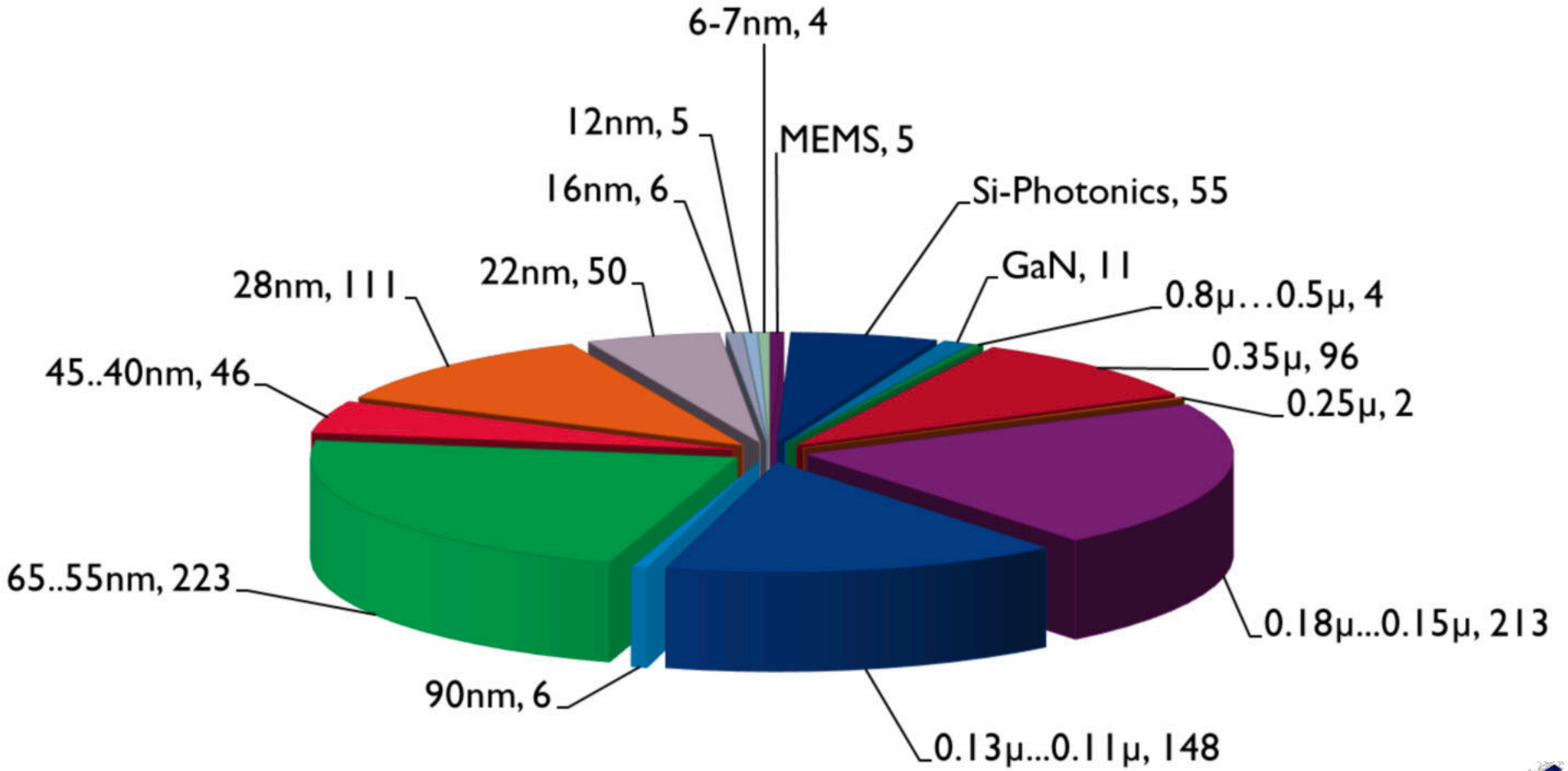
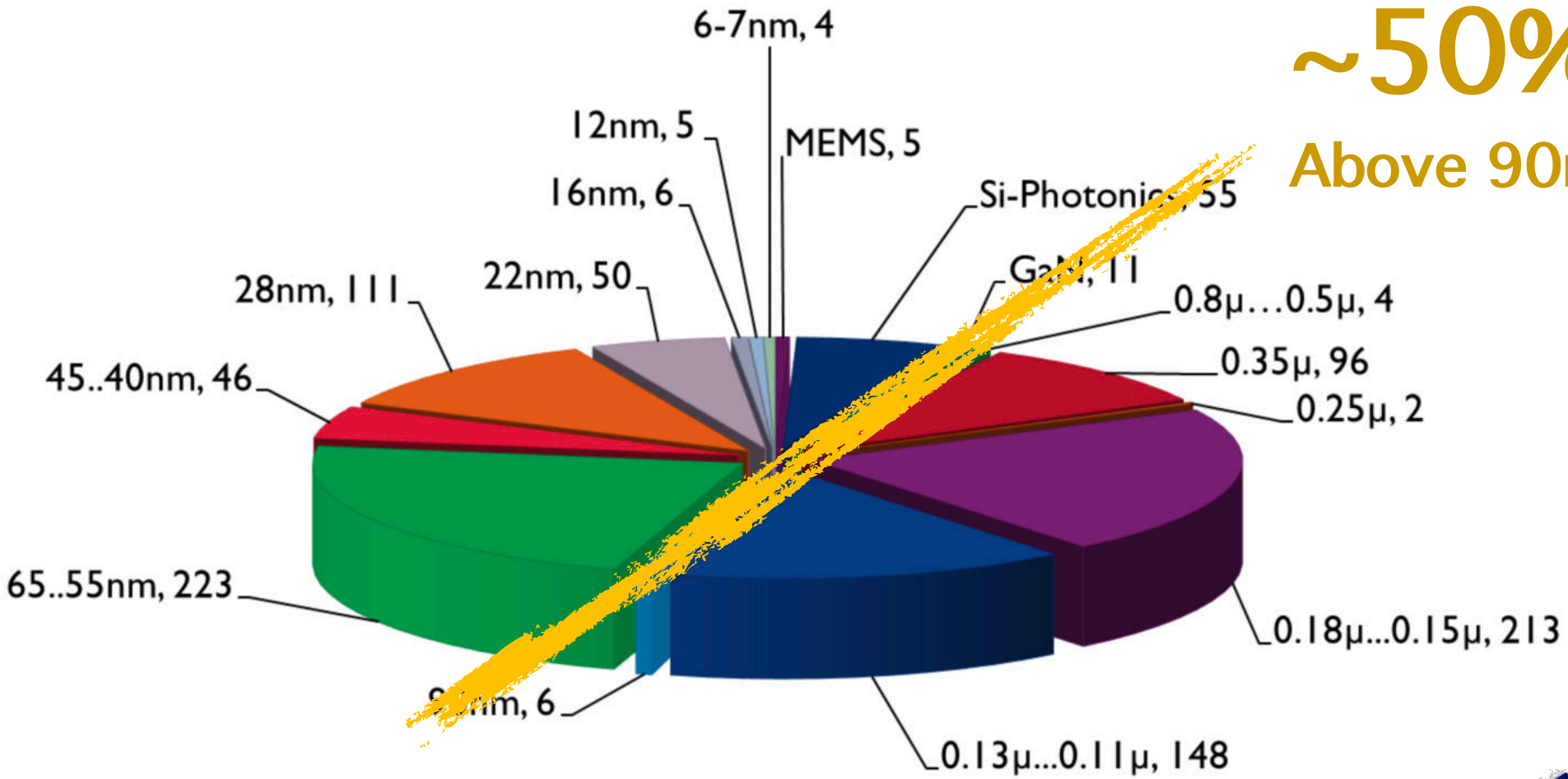
FABRICATION SERVICE (CIRCUITS 2021)



EUROPRACTICE has received funding from the European Unions H2020 Framework Programme for research, technological development and demonstration under grant agreement No 825121

FABRICATION SERVICE (CIRCUITS 2021)



~50%

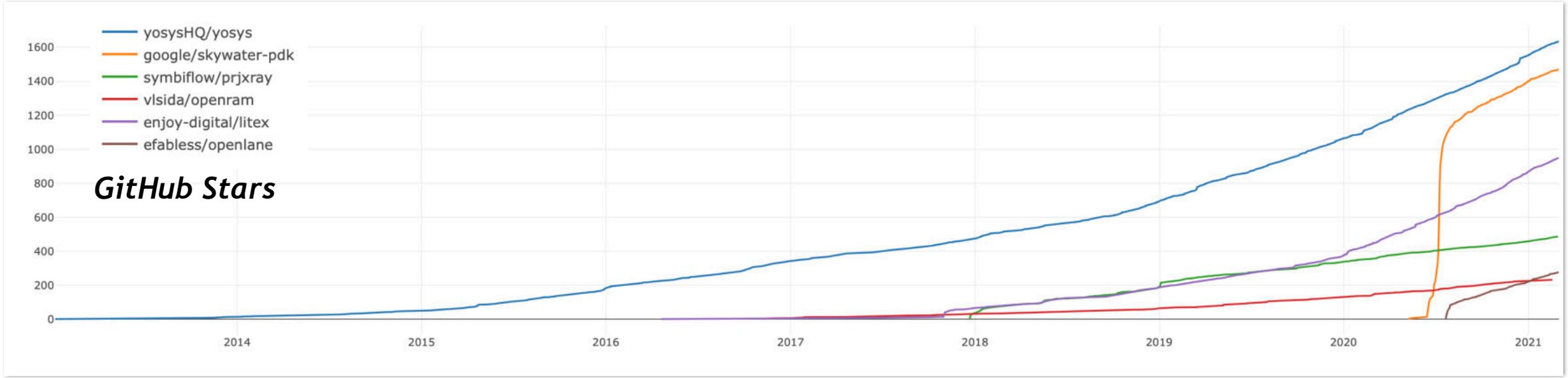
Above 90nm

EUROPRACTICE has received funding from the European Unions H2020 Framework Programme for research, technological development and demonstration under grant agreement No 825121

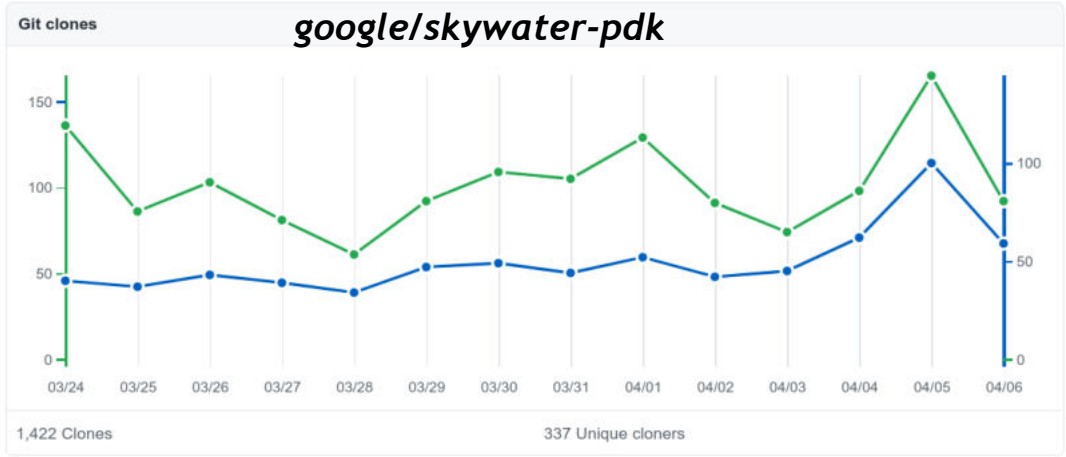
A LOT.....

See efabless.com/projects

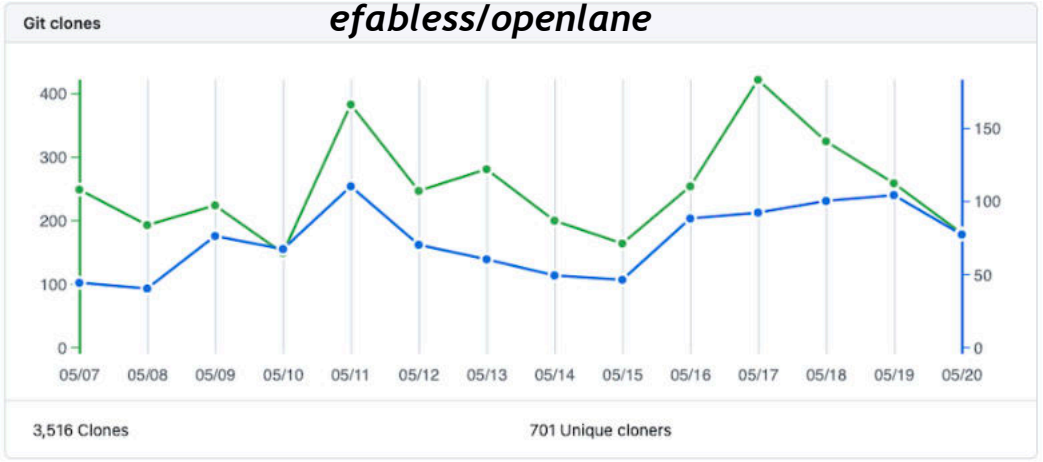
SKY130 OPEN SOUCRE PDK WENT VIRAL



google/skywater-pdk



efabless/openlane



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LIVE SLACK COMMUNITY

3K+

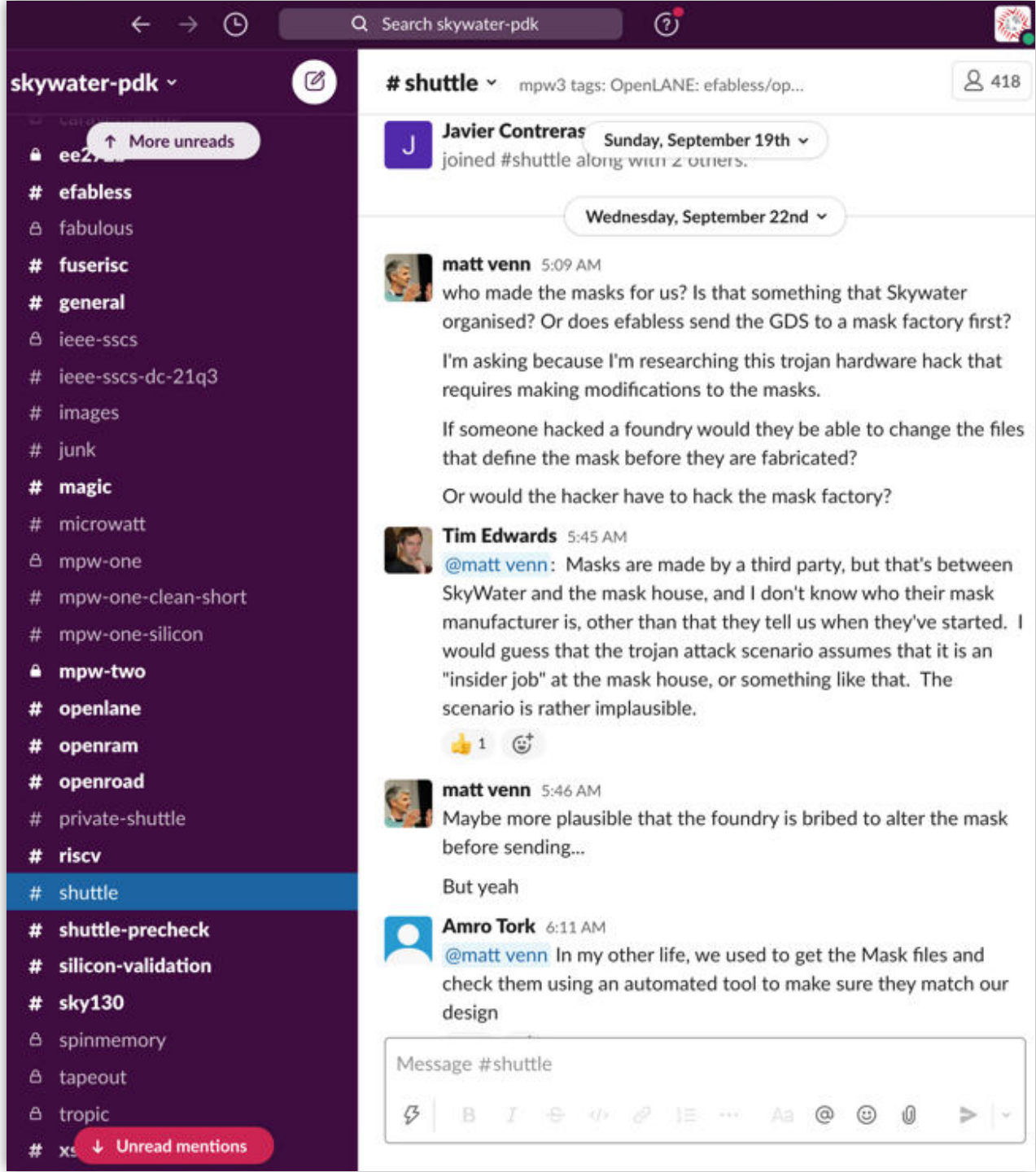
COMMUNITY MEMBERS

100+

CHANNELS & TOPICS

Join SkyWater-PDK Community

https://join.skywater.tools



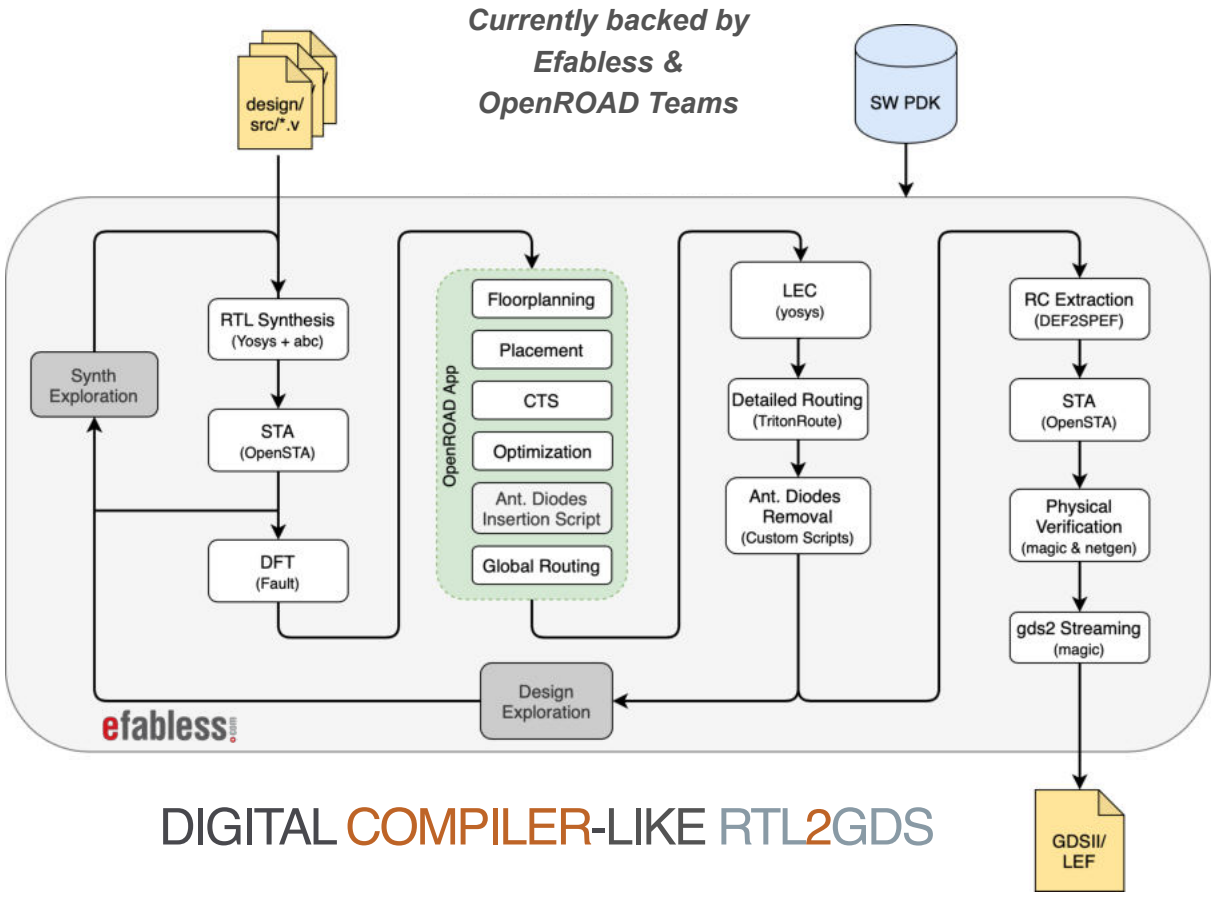
How do we simplify chip design? **#2**

Codify and abstract knowledge

Automate code-to-chip like a ***GNU software compiler -*** *with trade-offs in area and performance.*

It opens the door for software developers to generate hardware

That's at least a 1000X more potential designers!



DIGITAL COMPILER-LIKE RTL2GDS

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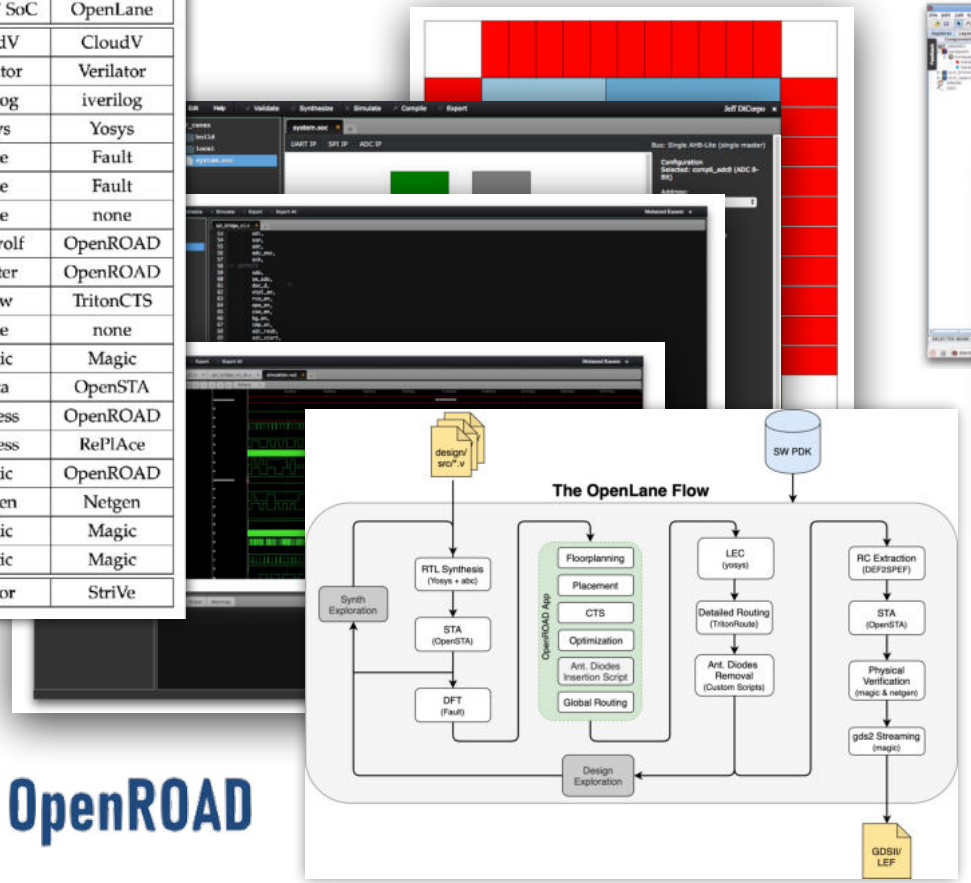
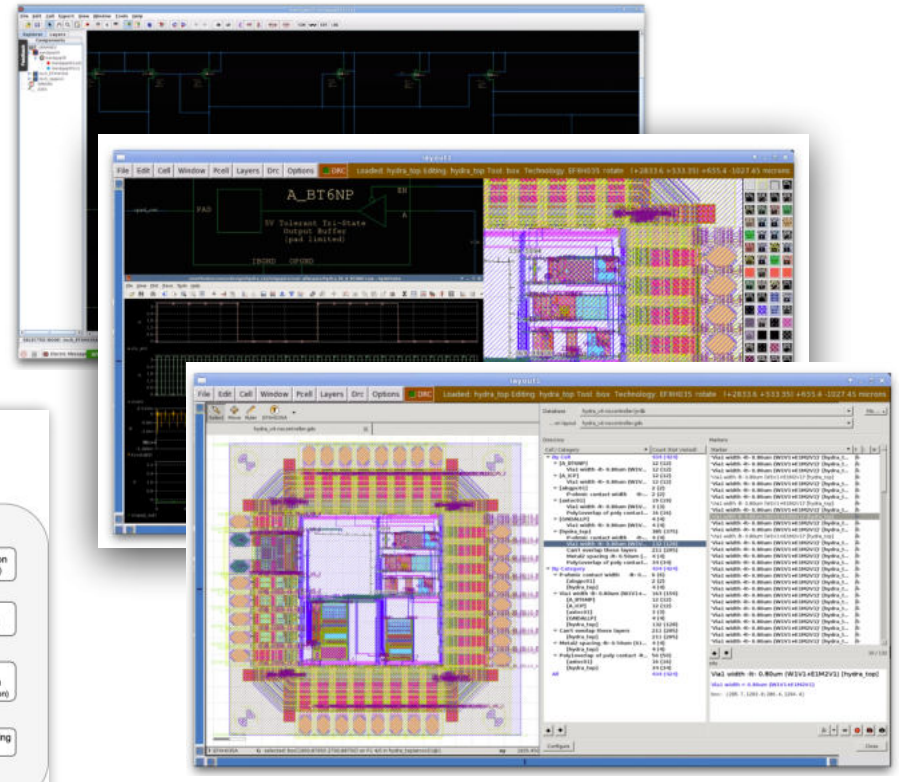
OPEN SOURCE DESIGN FLOWS & TOOLS

DESIGN STEP	Qflow	CloudV SoC	OpenLane
System Design	N/A	CloudV	CloudV
RTL Lint	Verilator	Verilator	Verilator
RTL Simulation	iverilog	iverilog	iverilog
Logic Synthesis	Yosys	Yosys	Yosys
DFT Scan Insertion	none	none	Fault
DFT ATPG	none	none	Fault
Formal Verification	none	none	none
Placement	graywolf	graywolf	OpenROAD
Routing	qrouter	qrouter	OpenROAD
CTS	Qflow	Qflow	TritonCTS
Dynamic EMIR	none	none	none
Extraction	Magic	Magic	Magic
Timing Analysis	Vesta	Vesta	OpenSTA
Floorplanning	Magic	efabless	OpenROAD
Top-Level Placement	Magic	efabless	RePlAce
Top-Level Routing	Magic	Magic	OpenROAD
LVS	Netgen	Netgen	Netgen
DRC	Magic	Magic	Magic
GDS	Magic	Magic	Magic
SoC	Raven	Raptor	StriVe





- SoC Editor
- RTL Simulation
- Synthesis
- GL Simulation

OpenROAD

- Schematic Capture
- SPICE Simulation

- Mixed-Mode Simulation
- Parasitic Extraction
- Physical Verification

Silicon Compiler **Coriolis** **OpenLane**

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ANALOG TRANSISTOR-LEVEL

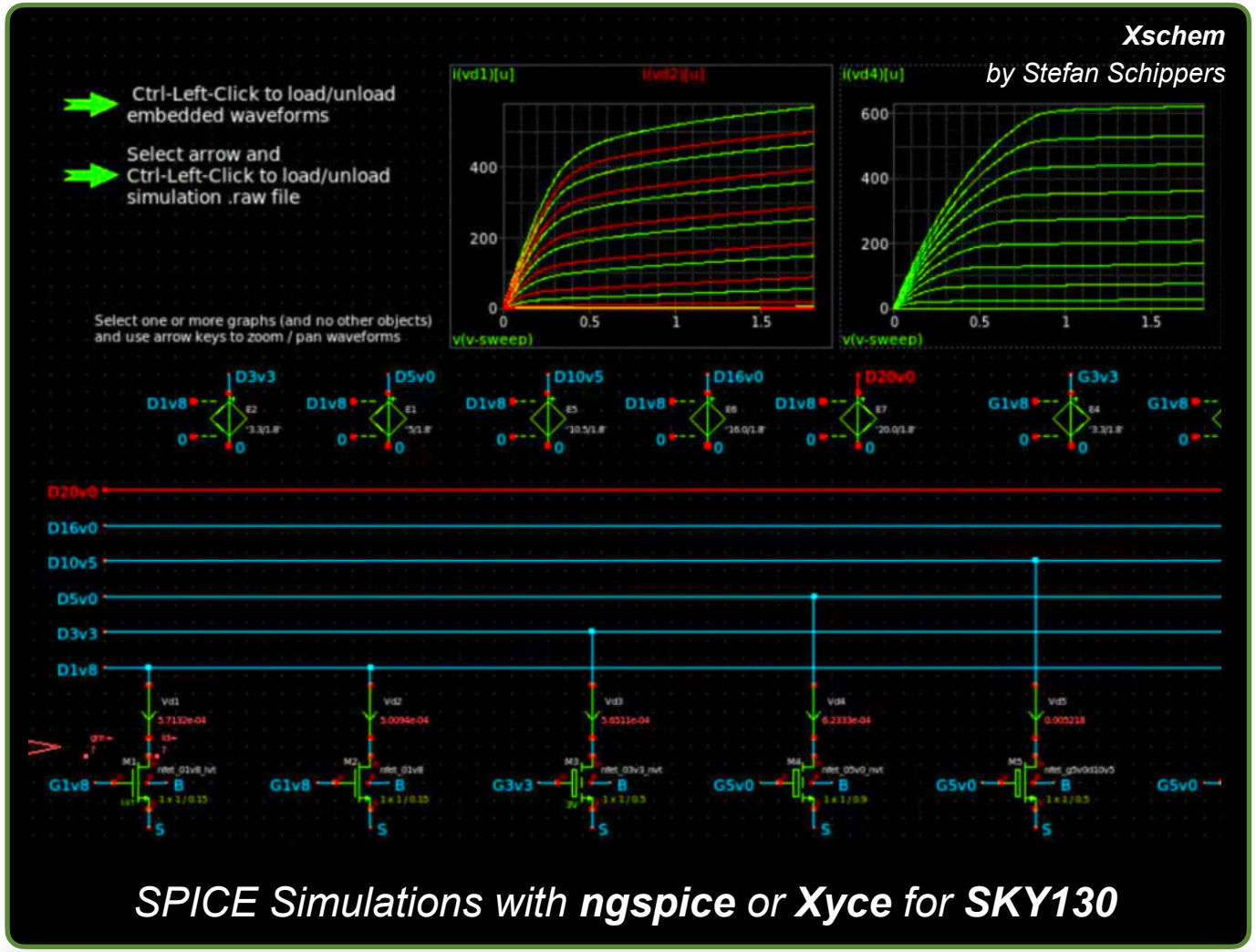
Analog transistor-level design, schematic and layout

Schematics: Xschem

Simulators: ngspice, Xyce

Support: Process Corners and statistical simulations

Packed with out-of-the-box examples - just click, copy and run yours



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Why does it matter to have tools open-sourced?

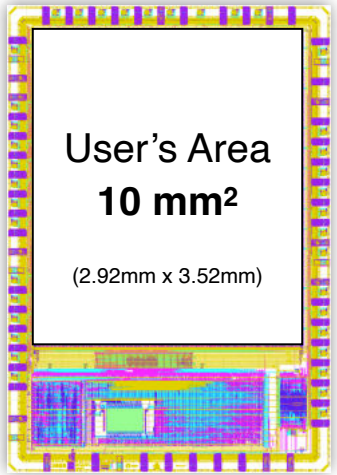
***Limitless availability** which fosters **spontaneous idea realization** and open **collaborative** development by community*

How do we simplify chip design? **#3**

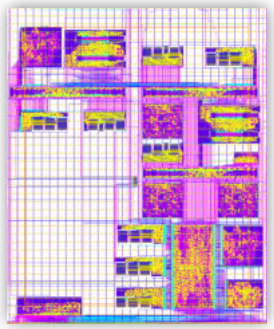
Start from the 15th floor to reach 20

*Build on existing foundational work by others - **CARAVEL***

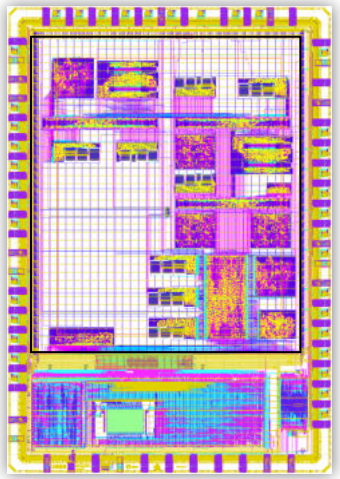
*You only need to know your design … or **your code***



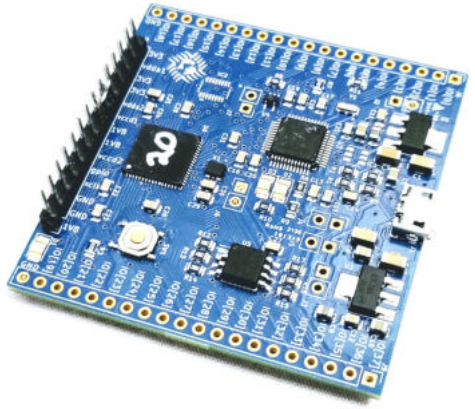
CARAVEL



My Design



CARAVEL + My Design



Plug & Play Dev Board

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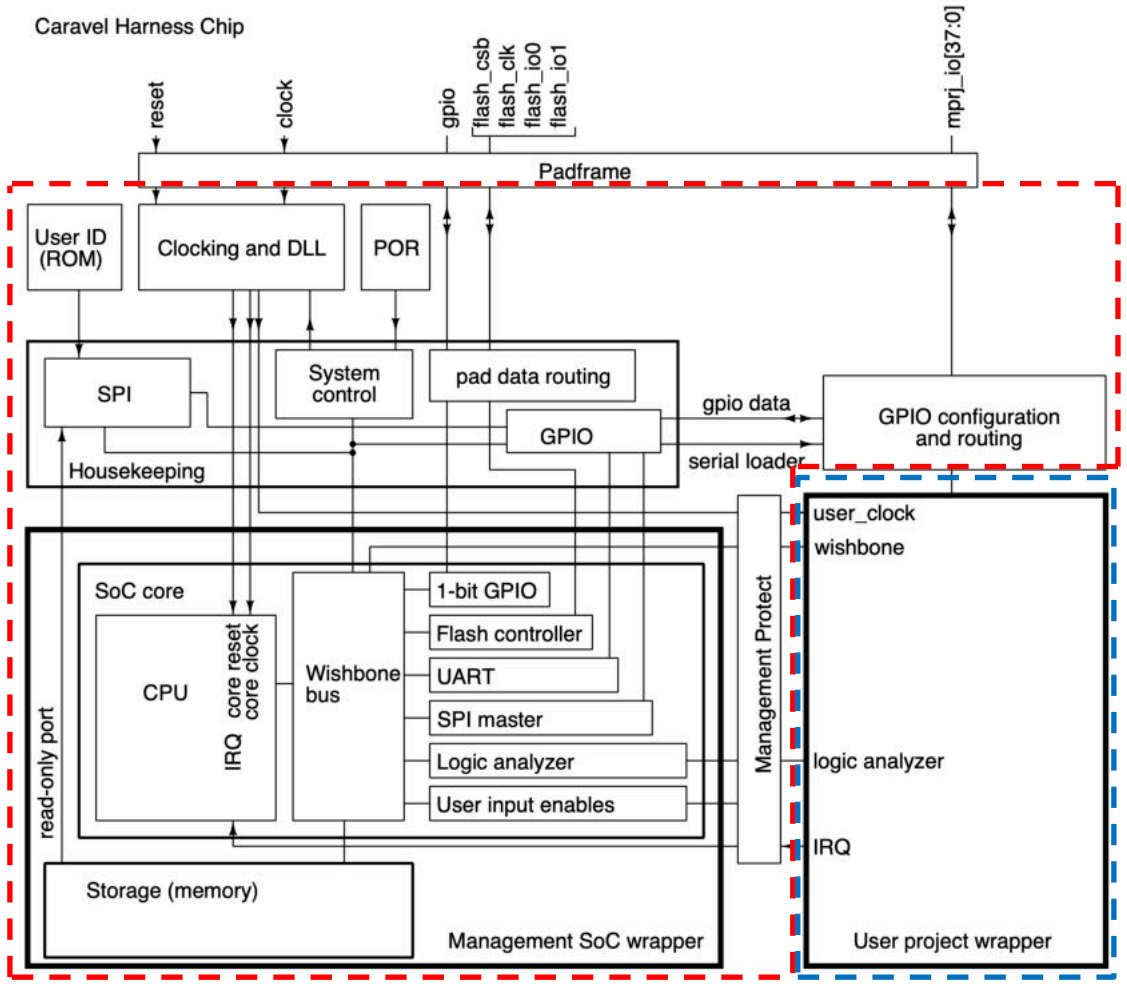
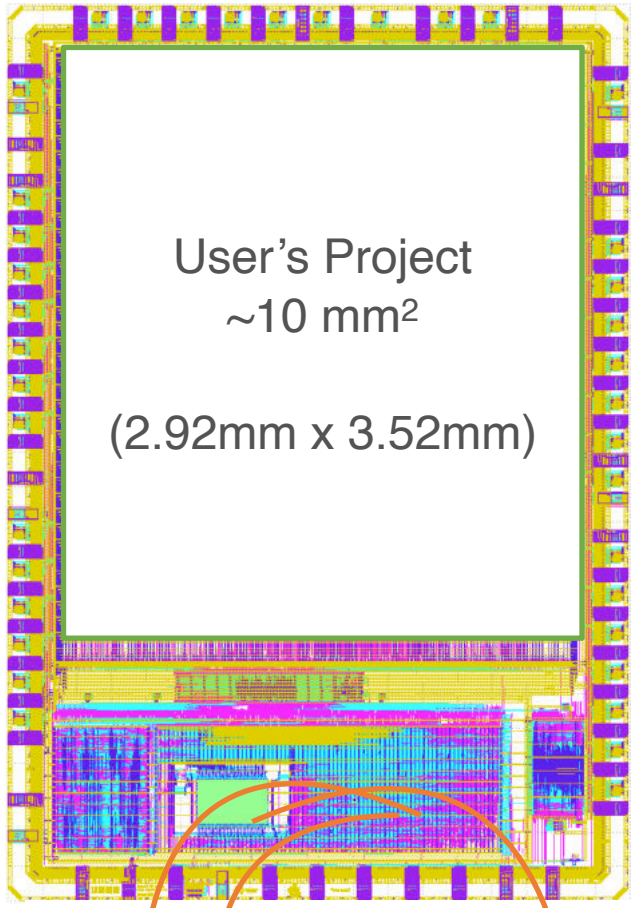
CARAVEL PLATFORM



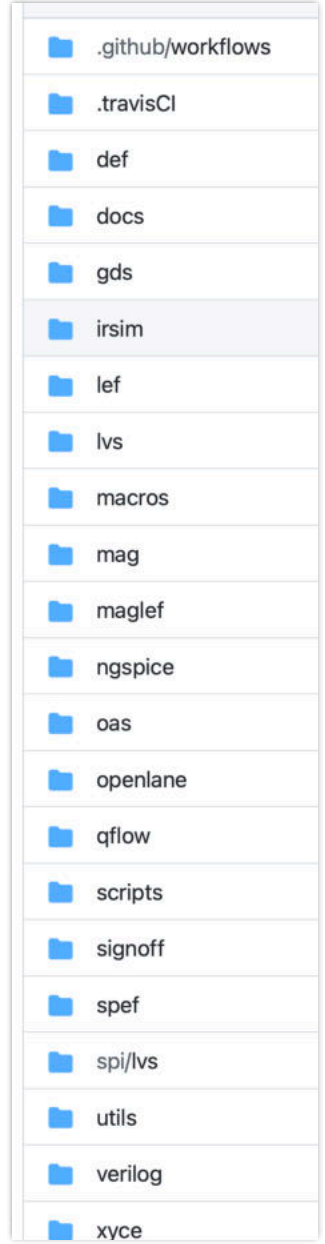
https://github.com/efabless/caravel

CARAVEL SoC Platform



PicoRV32 OpenRAM
OpenROAD OpenLane

Uniform Open Source File Structure to ease reuse & modifications



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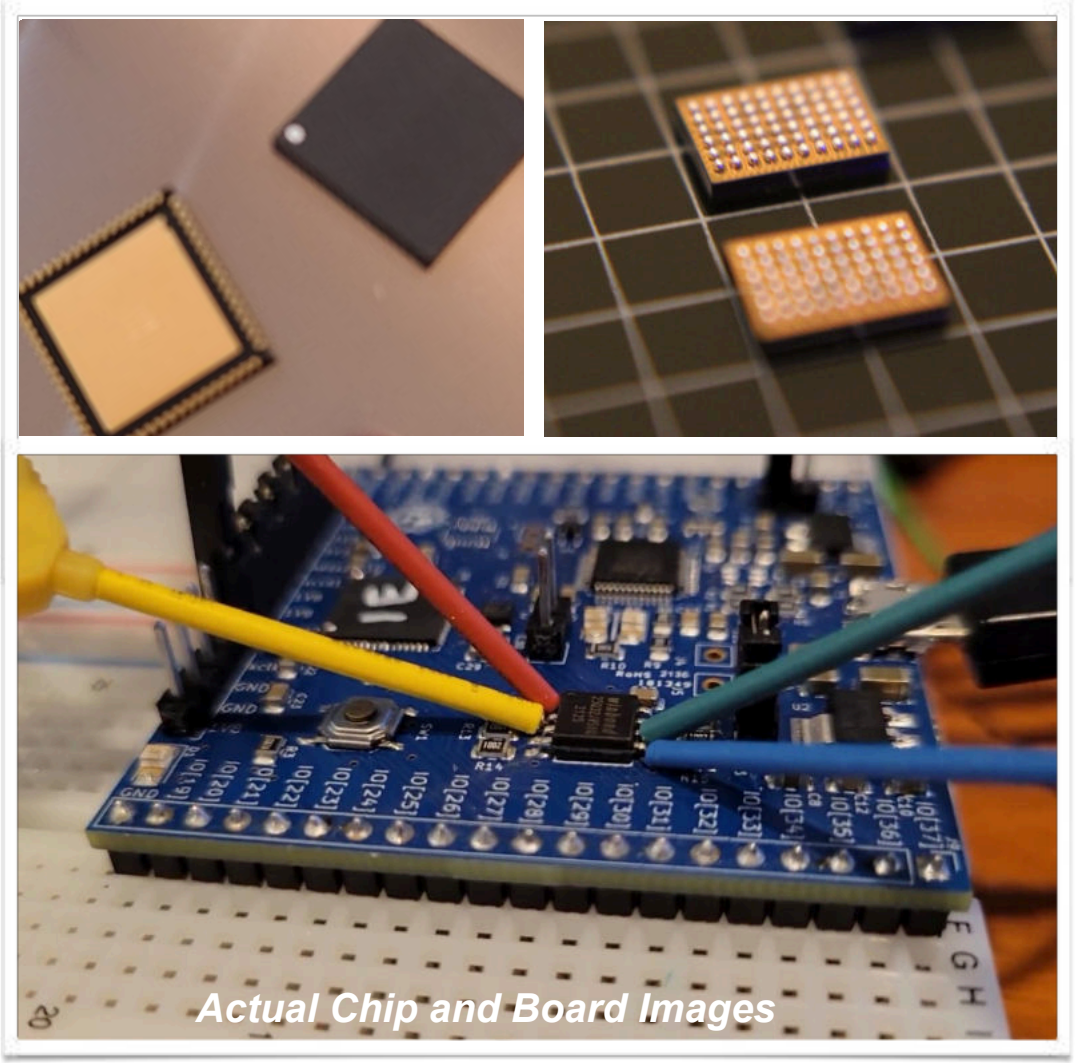
SILICON TESTING & VALIDATION



Designers receive **packaged chips** and **assembled 5 evaluation boards** with for each project

On-chip **open source** test framework with firmware to support the following:

- On-chip logic Analyzer
- Drivers for common peripherals
- Flash memory programming software utility
- Example firmware routines for common functions
- Instructions for customizing firmware for each project

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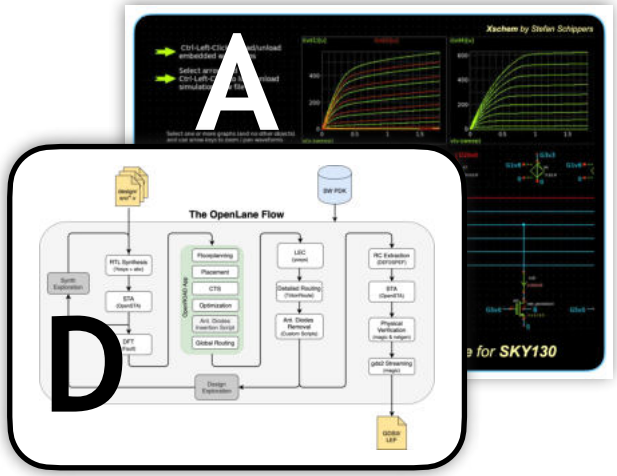
OS EDA Digital & Analog



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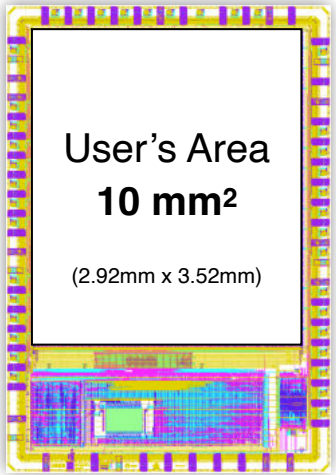
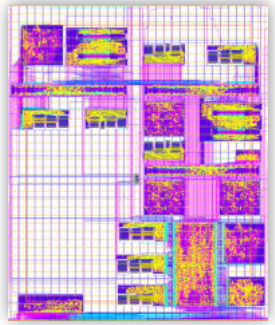
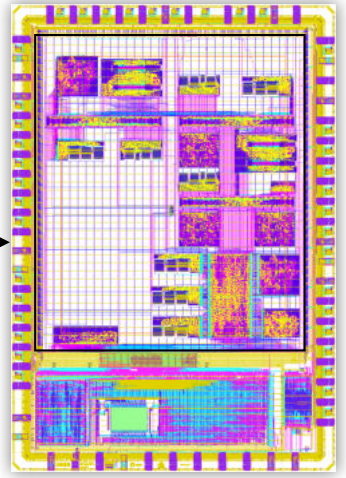


CARAVEL

+

User Design





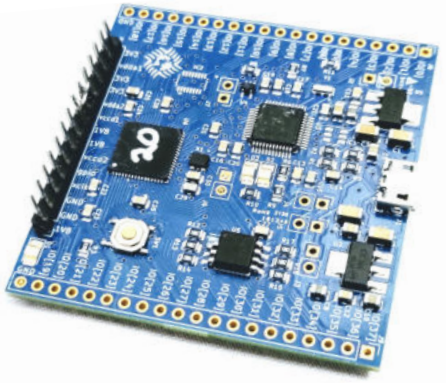
CARAVEL + User Design

MANUFACTURING

Start Here
https://ef.link/start-digital
https://ef.link/start-analog

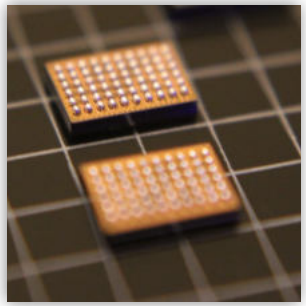
Software (FOSS)

+



5 Dev Boards

+



300 WCSP Parts

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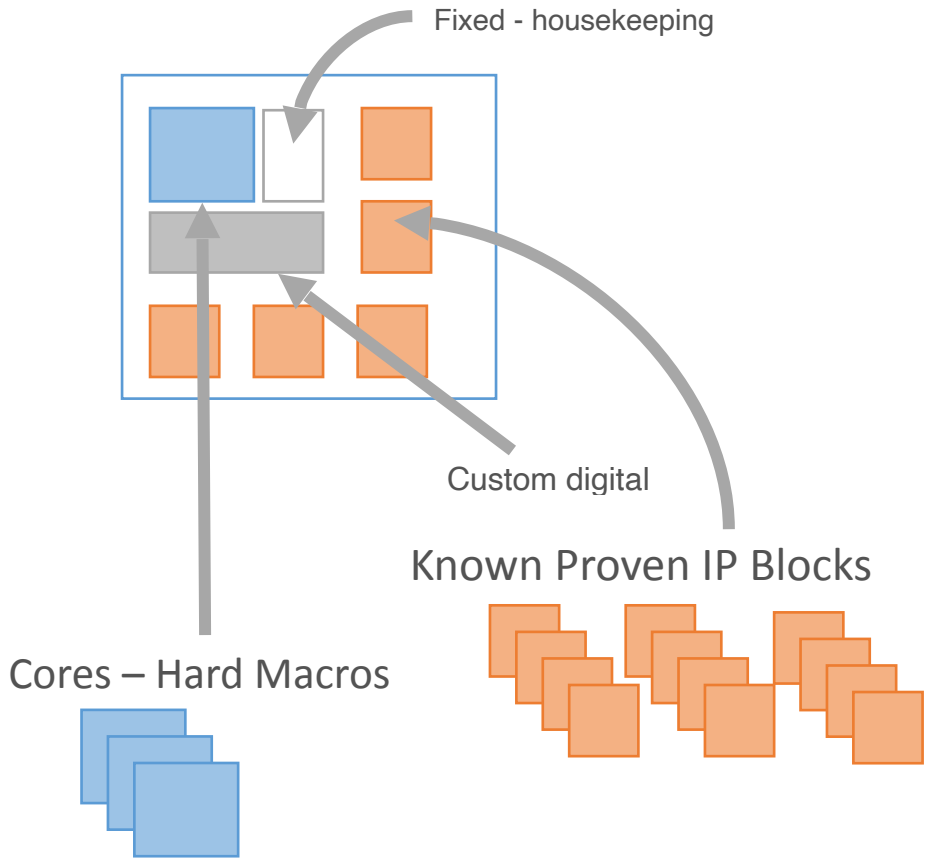
How do we simplify chip design? **#4**

Build an **open** library of “IP blocks”

Make them like **LEGO**

- Silicon proven / verified functions
- Highly leveraged known proven IP blocks
- Scope of customization is constrained
- Quality processes enable extending the known proven IP blocks by community



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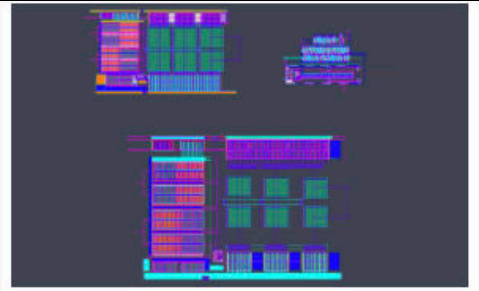
Select Open Source Designs

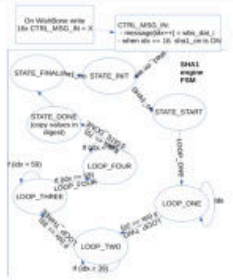


caravel_fulgor_opamp public

Diego Hernando | http://www.fundacionfulgor.org.ar/sitio/index.php

Operational amplifier (opamp) based on the Miller topology designed in Skywater SKY130 CMOS process.

MPW-1 SKY130 2.2k

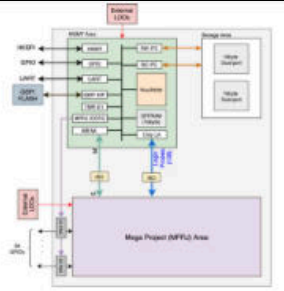


SHA1 engine public

Konrad Rzeszutek Wilk

The SHA1 engine, while not the most secure nowadays is still used by git commits and TPM PCR...

MPW-2 SKY130A 731

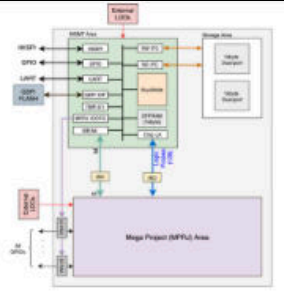


Caravel-SOFA-HD public

Xifan Tang | https://sites.google.com/site/pegaillardon/home

SOFA-HD (Skywater Opensource FPGAs)

MPW-1 SKY130 1.6k

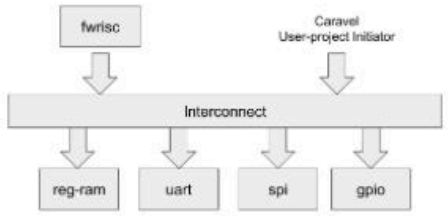


Caravel public

Sylvain Munaut | https://github.com/PyFive-RISC-V

Peripherals tests for future SoC targeting Micro/Circuit Python

MPW-1 SKY130 1.8k

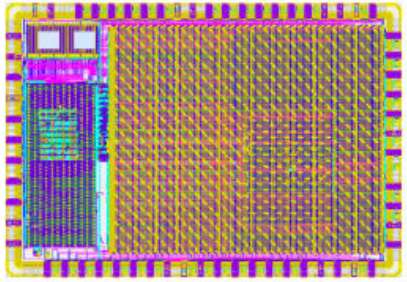


FWPayload public

Matthew Ballance | http://github.com/mballance

A simple RISC-V core+peripherals subsystem for the Google-sponsored Open MPW shuttles for SKY130.

MPW-1 SKY130 962

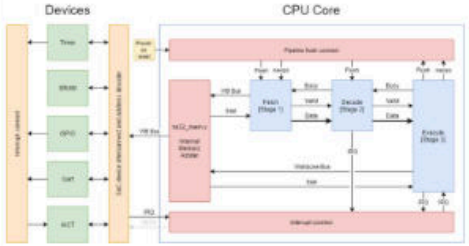


Caravel_Astria_Testchip public

Astria Nur Irfansyah | http://www.its.ac.id

Test circuits consisting of synthesizable comparators for a stochastic ADC, to be submitted for...

MPW-1 SKY130 1.2k

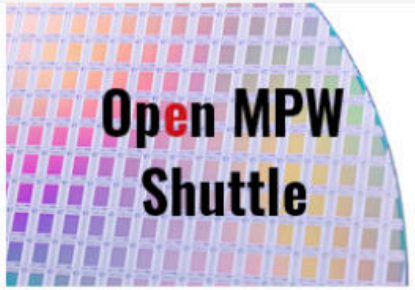


HS32Core public

Kevin Mack Baragona | https://github.com/hsc-latte

Open Source Hardware Processor

MPW-1 SKY130 1.4k



10_bit_potentiometric_DAC public

Sameer S Durgoji | https://www.vlsisystemdesign.com/

Design of a 10 Bit Potentiometric Digital to Analog Converter with 3.3V analog voltage, 1.8V...

MPW-2 SKY130A 1.1k