SiFive Automotive, AI & Use Case

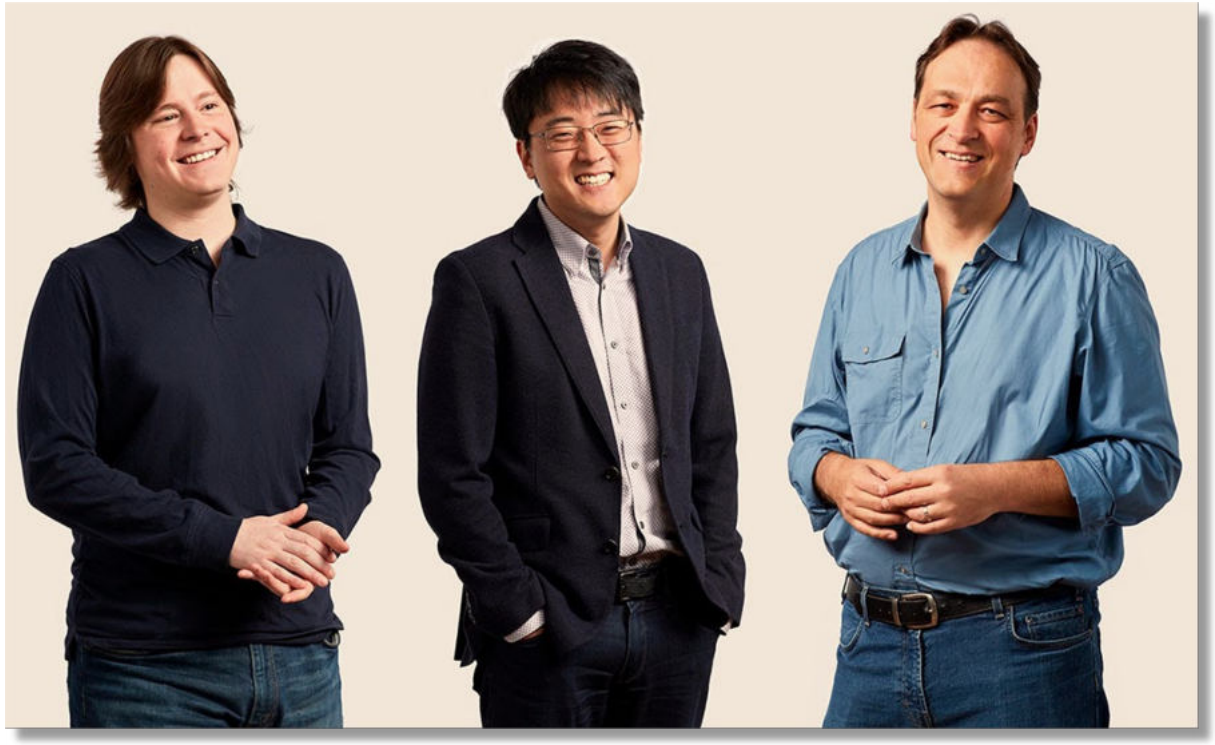
RISC-V Days Tokyo 2022 Autumn

Sam Rogan, Yoshihito Kondo, SiFive Japan 株式会社

Nov, 18th 2022

SiFive: The RISC-V Founder and Brand Standard

We Invented RISC-V



SiFive's founders are the same UC Berkeley professor and PhDs who invented and have been leading the commercialization of the RISC-V Instruction Set Architecture (ISA) since 2010

Recognized as the Most Respected Private Semiconductor Company
2018, 2019, 2020

GSA 2018 Awards

GSA 2019 AWARDS Winner

GSA 2020 Most Respected Private Semiconductor Company

SiFive

300+	100+	8 of 10	500+	$2.5B+
Design Wins	Companies	Top semiconductor companies work with us	Employees	Valuation

The Rise of RISC-V

Over 60 billion RISC-V cores projected to ship by 2025

Based on the already sizeable adoption of RISC-V, we forecast that the market will consume a total of ***62.4 billion RISC-V cores by 2025***

SoCs shipping with RISC-V between 2020 and 2027 projects ***73.6% CAGR***

Source: Semico Research

2,800 RISC-V International members across 70 countries

RISC-V is Inevitable

The ecosystem of the **Future** is already being deployed

- The only major global compute platform on an open standard
- Used by all top semiconductor companies
- Supported by 3200+ members in RISC-V International
- Platform of choice in China & India
- Selected by US Govt
- Taught in all Top Universities
- Publicly embraced by Intel
- The strongest, most robust ecosystem is built on open standards with multiple participants

Legacy ‘efficiency processors’ are failing the industry

- Latest market requirements are not being met by current suppliers
- No innovation for the last 5 years
- SiFive’s latest innovation brings significant upgrade opportunities
- Vector compute brings performance boost and power efficiency
- SiFive Performance portfolio enables greater design flexibility

Market requirements for wearables

Smartwatch, sport watch, fitness tracker, Feature phones, smartphones

Performance efficiency is critical

- Feature-rich OS demand aggressive design innovation
- Advanced features put stress on power envelope
- Physical dimensions require optimized area

SiFive solutions

- Best compute density enables greater flexibility
- Future-proof for next generation premium wearables
- Vector computing for AI/ML, media and sensor processing
- Path to Android Wear OS with RVA22/Platform-A

Need for more performance & efficiency

- Requirement for dynamic scalable processor architecture
- Phone apps and UI drive constant innovation
- Battery life remains a key requirement

SiFive solutions

- Mixing high-performance and high-efficiency cores
- Vector computing for AI/ML and video workloads
- RISC-V standardized RVA22 to enable Android OS
- System-level virtualization support
- Advanced power management features

Market requirements for smart home appliances

Home assistant, smart TV, STB, smart speaker, thermostat, door bell, security camera

High processing power and edge AI required

- Audio processing & voice activation/recognition
- Edge AI vision for object detection & filtering
- 4K+ video encoding/decoding
- Network connectivity

SiFive solutions

- Broad portfolio to address full range of devices
- Vector compute for AI/ML, sound & media processing
- Auto-vectorizing compiler simplifies product development
- Vector cryptography for TLS/SSL acceleration
- Strong Linux community with standard software & RVA22

Market requirements for network appliances

Router, switch, WiFi AP, 5G base station

Need for performance & data throughput

- High throughput & massive parallel processing needs
- Hardware isolation for better software security

SiFive solutions

- Linux enabled high performance efficient processors
- Coherent multi-core and multi-clusters capability
- Flexible multi-level cache with cache stashing
- Vector crypto for TLS/SSL acceleration
- System-level virtualization support & WorldGuard

SiFive cores to power NASA's next spaceflight computer

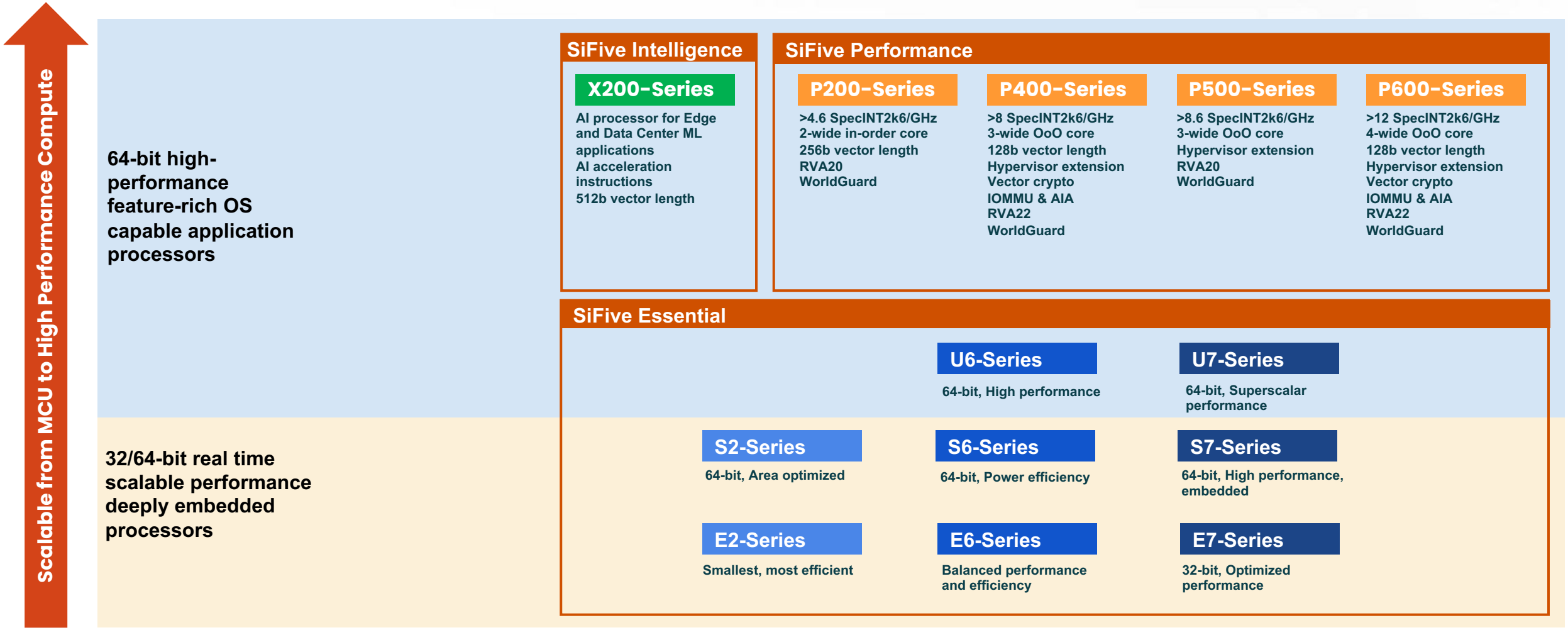
- High Performance **Spaceflight Computing Processor** will utilize an 8-core, **SiFive® Intelligence™ X280** RISC-V vector core, as well as four additional SiFive RISC-V cores, to deliver 100x the computational capability of today's space computers.
- X280 is a multi-core capable RISC-V processor with vector extensions and SiFive Intelligence Extensions and is optimized for AI/ML compute at the edge.
- Ideal for applications requiring high-throughput, single-thread performance while under significant power constraints.
- 100x increase in computational capability vs. today's space computers
- Leading power efficiency, fault tolerance, and compute flexibility
- In scientific and space workloads, X280 provides several orders of magnitude improvement over competition
- Open and collaborative RISC-V ecosystem allows broad academic and scientific software development community to contribute and develop scientific applications and algorithms

Google uses SiFive RISC-V cores in AI compute nodes

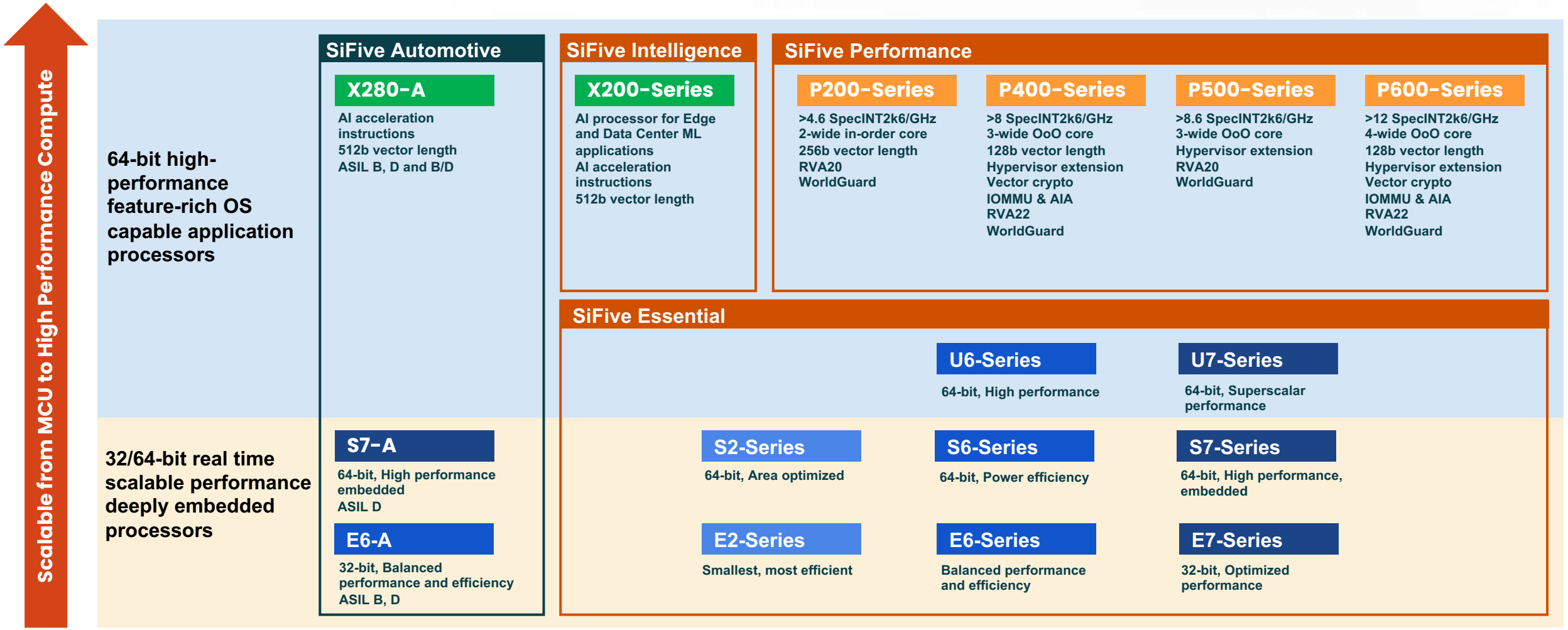
- At the AI Hardware Summit in Santa Clara, September 14th, Krste Asanovic, SiFive Co-Founder and Chief Architect, took to the stage with Cliff Young, Google TPU Architect and MLPerf Co-Founder, to reveal how the latest **SiFive Intelligence™ X280** processor with the new SiFive Vector Coprocessor Interface Extension (**VCIX**) is being used as the AI Compute Host to provide flexible programming combined with the Google MXU (systolic matrix multiplier) accelerator in the **datacenter**.

- Please find more detailed article in SiFive blog below.
  https://www.sifive.com/blog/sifive-intelligence-x280-as-ai-compute-host-google

SiFive broad IP portfolio



SiFive broad IP portfolio



Enhancing the SiFive Performance Portfolio

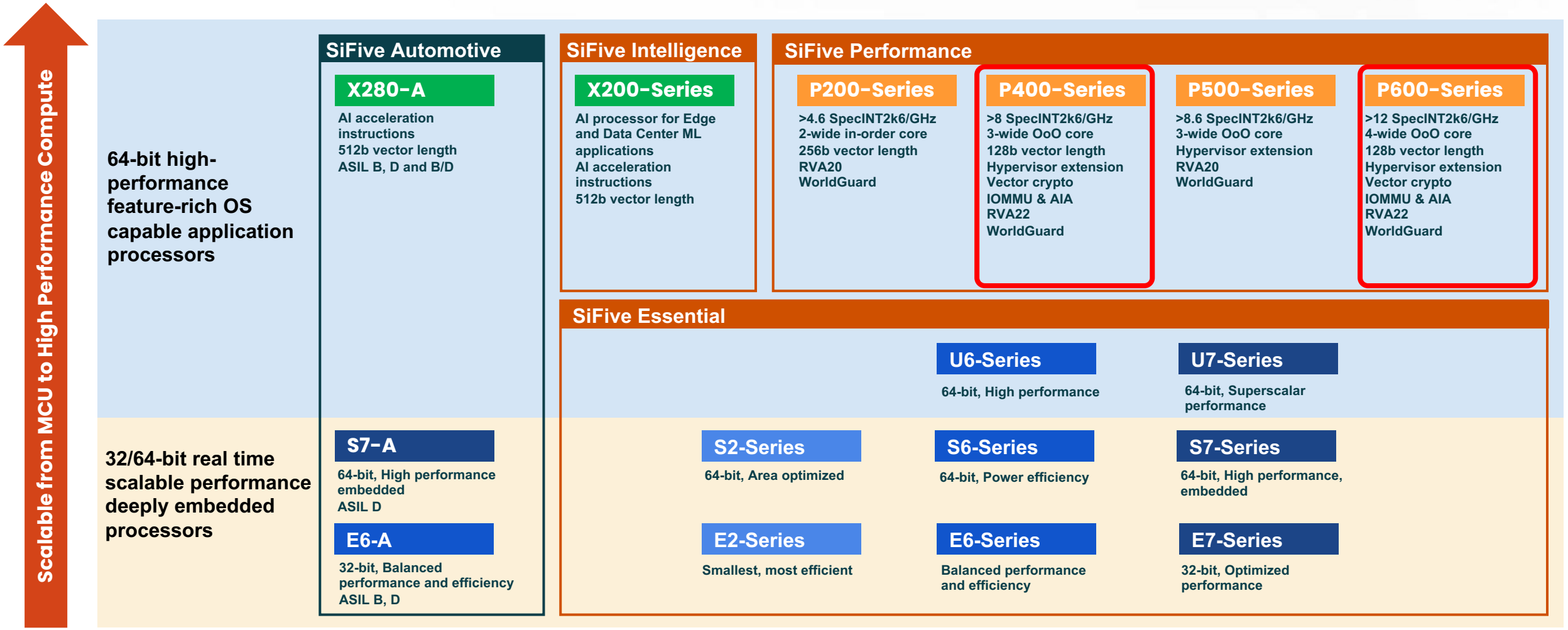
Extended family of area & power efficient processors

SiFive Performance™ Family

Market **leading RISC-V** Application **Processors**

- Performance density leadership
- First with latest RISC-V features, standards, and technology
- High performance with optimized power efficiency
- SiFive momentum with NASA, Google, and Intel Horse Creek

SiFive broad IP portfolio



SiFive

SiFive Performance™ P470

Boosted
Performance

Significant upgrade to legacy efficiency cores

Small
Area

Optimized area for power constrained applications

Efficient
Power

Highly-tuned for aggressively low power consumption

Optimized
Pipeline

Out-of-Order pipeline enables optimal performance efficiency

RISC-V
Compliant

Compliant with RVA22 profile, with support for Vector and Vector Crypto extensions

SiFive Performance™ P670

Highest
Performance

Best-in-class performance

Balanced
PPA

Optimized performance within constrained area and power envelope

Vector
Extensions

Acceleration for media, crypto and data processing

Feature
Rich

Virtualization, IOMMU, AIA, Debug & Trace, Security

RISC-V
Compliant

Compliant with RVA22 profile, with support for Vector and Vector Crypto extensions

Upgrade to the SiFive Performance Family

Performance density leadership

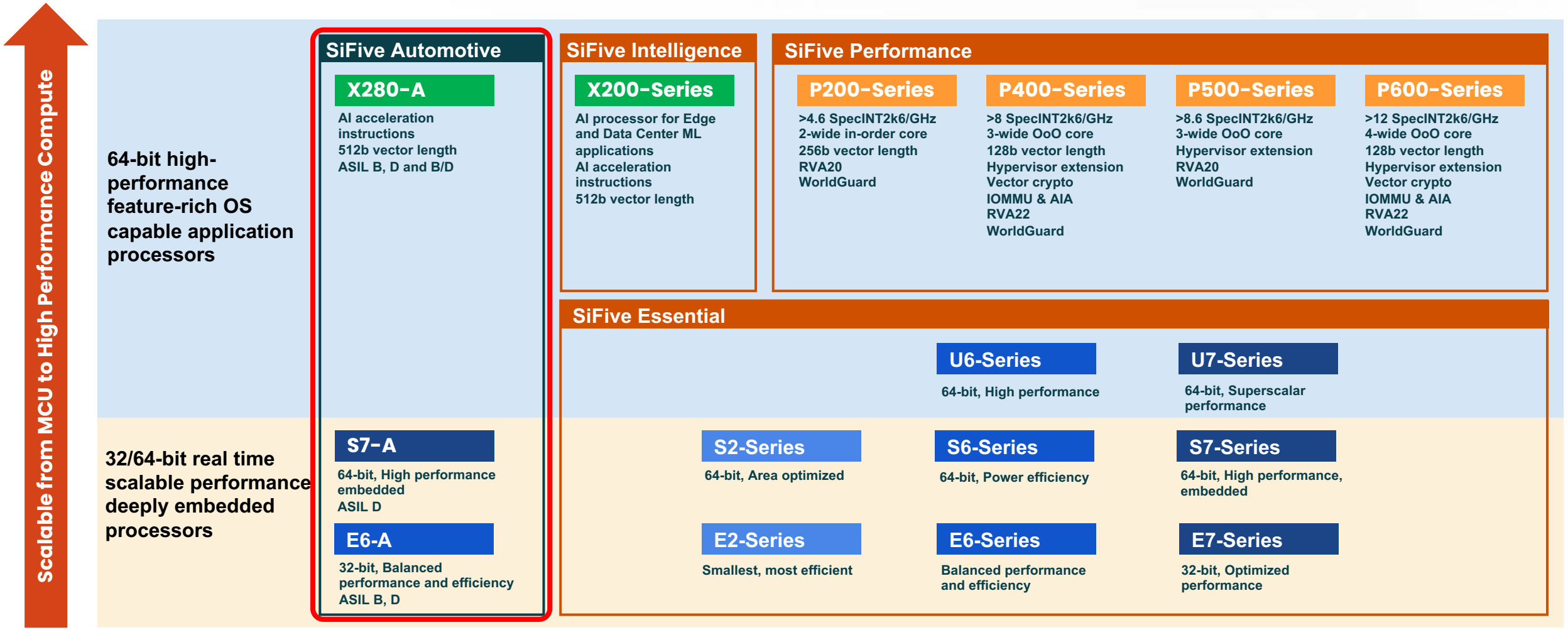
High performance with optimized power efficiency

First with latest RISC-V features, standards, and technology

The P400-Series and P600-Series are available to Lead Partners in Q4 2022

SiFive Automotive Solutions

SiFive broad IP portfolio



Automotive market for MCU & SoC

Automotive industry is moving towards a Software Defined Car

More ADAS capabilities being added to cars

- Increasing investments in all levels of vehicle autonomy
- 2020 to 2030 CAGR: 19% (SoC), 9% (MCU)*

Migration to domain/zonal architecture

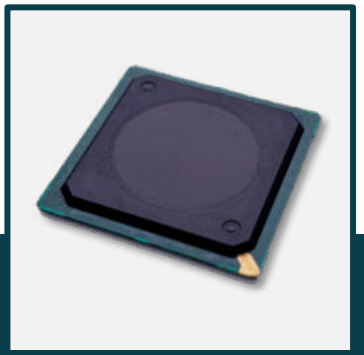
- Aggregation of multiple functions into single modules
- Transition to high-performance Central Compute
- Unified software development for greater flexibility

Electrification

- 2020 to 2030 CAGR: 20% (BMS)*

*Source: SiFive & Industry sources

RISC-V automotive industry benefits



Silicon Vendors

Optimized PPA

Flexible IP and business model

Long term support

Best-in-class Functional Safety

Tier-1s

Enhanced multi-sourcing

Custom development options

FuSa and security compliance

OEMs

Supply security

SW portability (single ISA)

Vertical integration of supply chain

Differentiated and cost-reduced ADAS solutions

Automotive RISC-V growth momentum

Renesas partners with SiFive to develop next generation high-end **RISC-V** Automotive Solutions

Apr 21'

IAR Systems extends support for Functional Safety Offering

Oct 21'

Kneron introduces **RISC-V** based AI edge chip for Auto

Nov 21'

European Processor project shifts from ARM to **RISC-V**

Dec 21'

Intel/Mobileye EyeQ Ultra based on **RISC-V**

Jan 22'

Green Hills support **RISC-V** RTOS targeting ISO-26262 ASIL applications

Feb 22'

NSITEXE selects Imperas for **RISC-V** Processor lock-step Verification

May 22'

SiFive ISO 26262 enablement

Safety Element out of Context (SEooC)

- SiFive CPU IP is considered as a hardware element treated as a SEooC (ISO 26262) and a compliant item (IEC 61508).

ASIL compliance

- ASIL B: Single Core + STL or partial redundancy architectures
- ASIL D: DCLS, Split-Lock

Safety Package

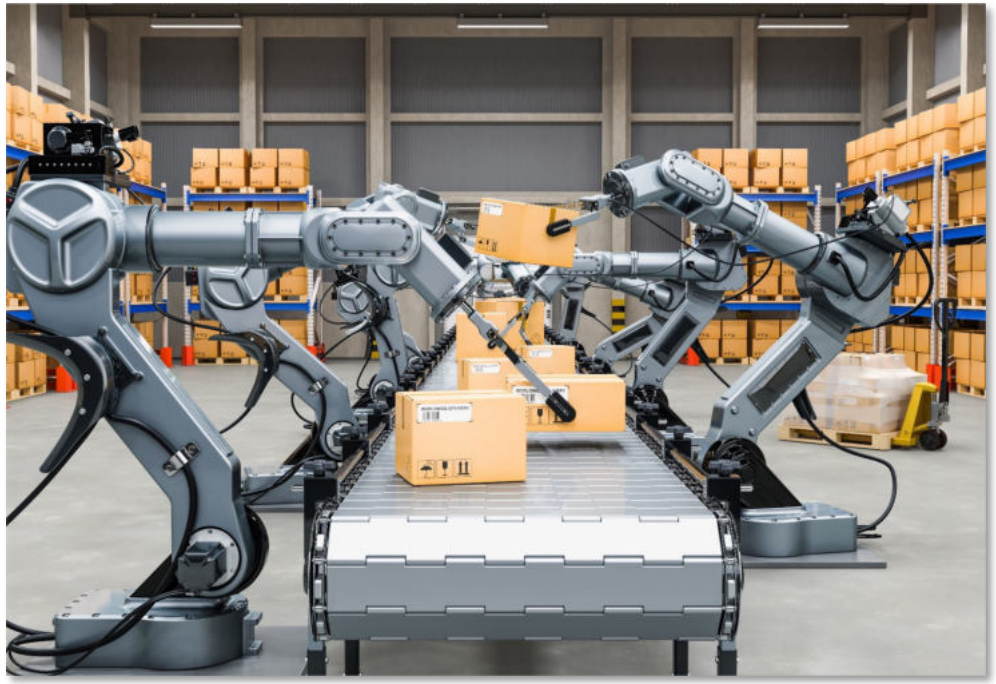
- Safety manual (safety architecture, safety mechanisms….)
- Safety report (FMEA, FMEDA, DFA…), DIA

SiFive Automotive RISC-V Ecosystem

Compilers, RTOS, Virtualization, STL, Safety consultancy…

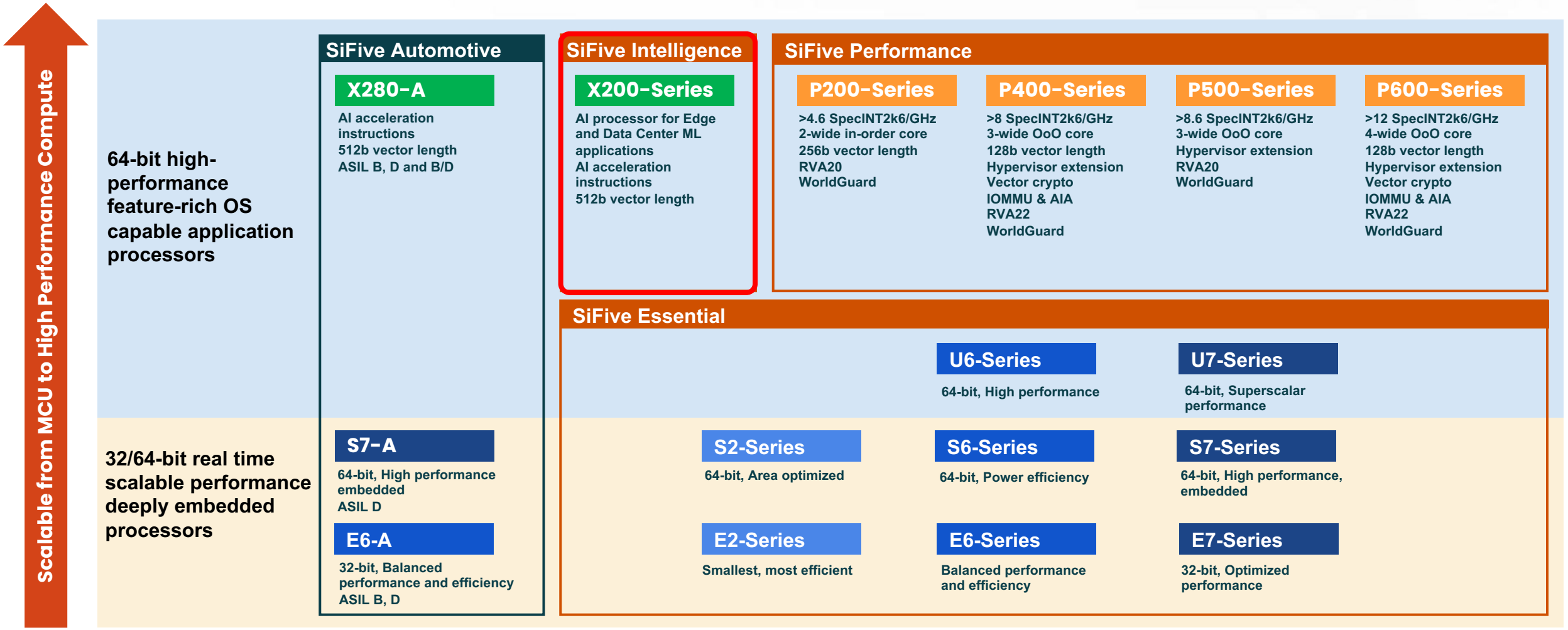
Expanding SiFive Markets with Functional Safety

Medical



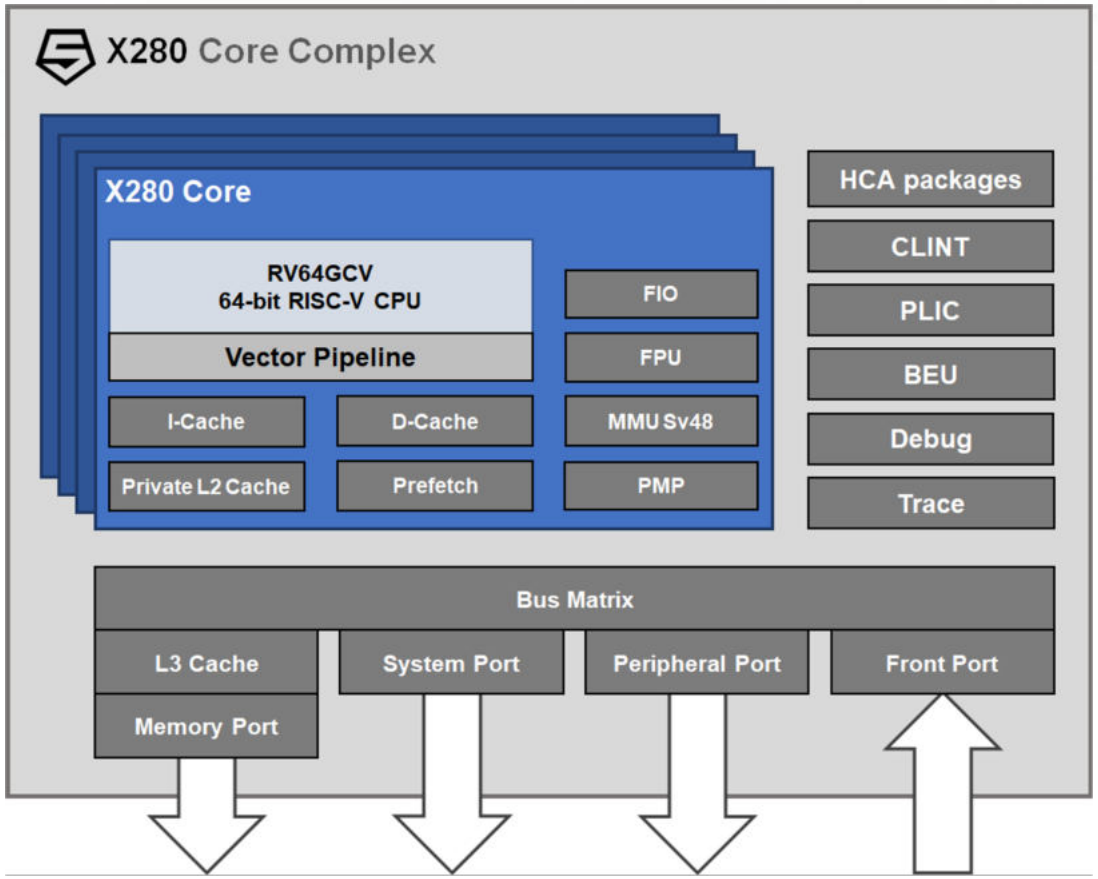
Industrial & Automation

SiFive broad IP portfolio

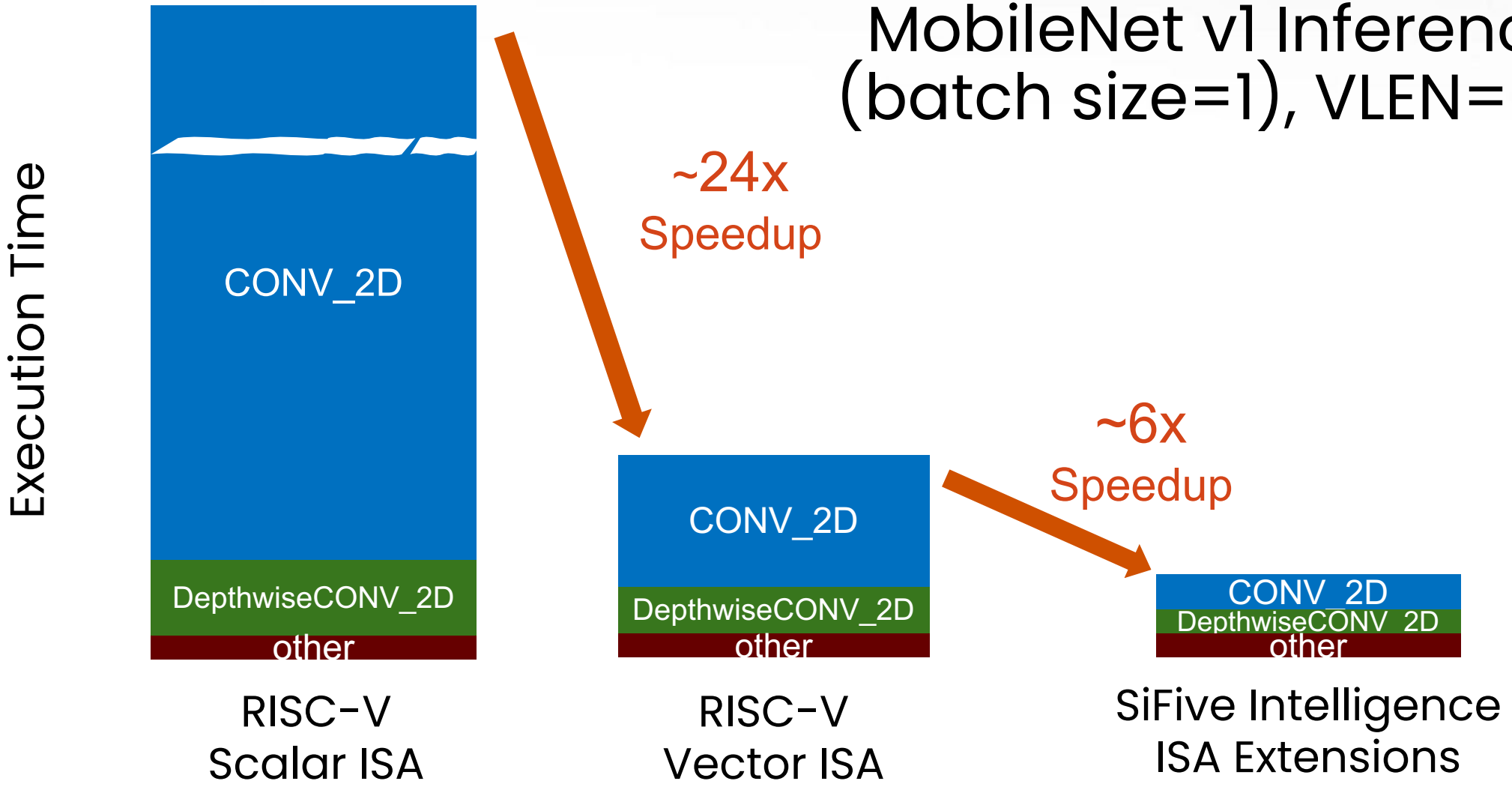


SiFive Intelligence X280

- RISC-V 64-bit scalar unit
  - 8-stage dual-issue in-order pipeline
- RISC-V vector unit with complete RVV v1.0 support
  - 32 x 512-bit vector registers
  - Up to 4096-bit vector operations (LMUL=8)
- SiFive Intelligence Extensions for AI/ML
  - Custom instructions accelerate critical AI/ML kernels
- Full Linux-capable applications processor (RVA22 profile)
  - Supports 48-bit virtual memory MMU (Sv48)
- Coherent multi-core configurations with up to 16 cores
- High-performance multi-level memory subsystem
  - Private L1 and L2 plus shared L3 for efficient data access
  - Stride prefetcher
- Performance
  - 5.7 CoreMarks/MHz 3.3 Dhrystone/MHz
  - 4.5 SpecINT2k6/GHz 3.4 SpecFP2k6/GHz (HiPerf config)



SiFive Intelligence: Accelerate end-to-end models

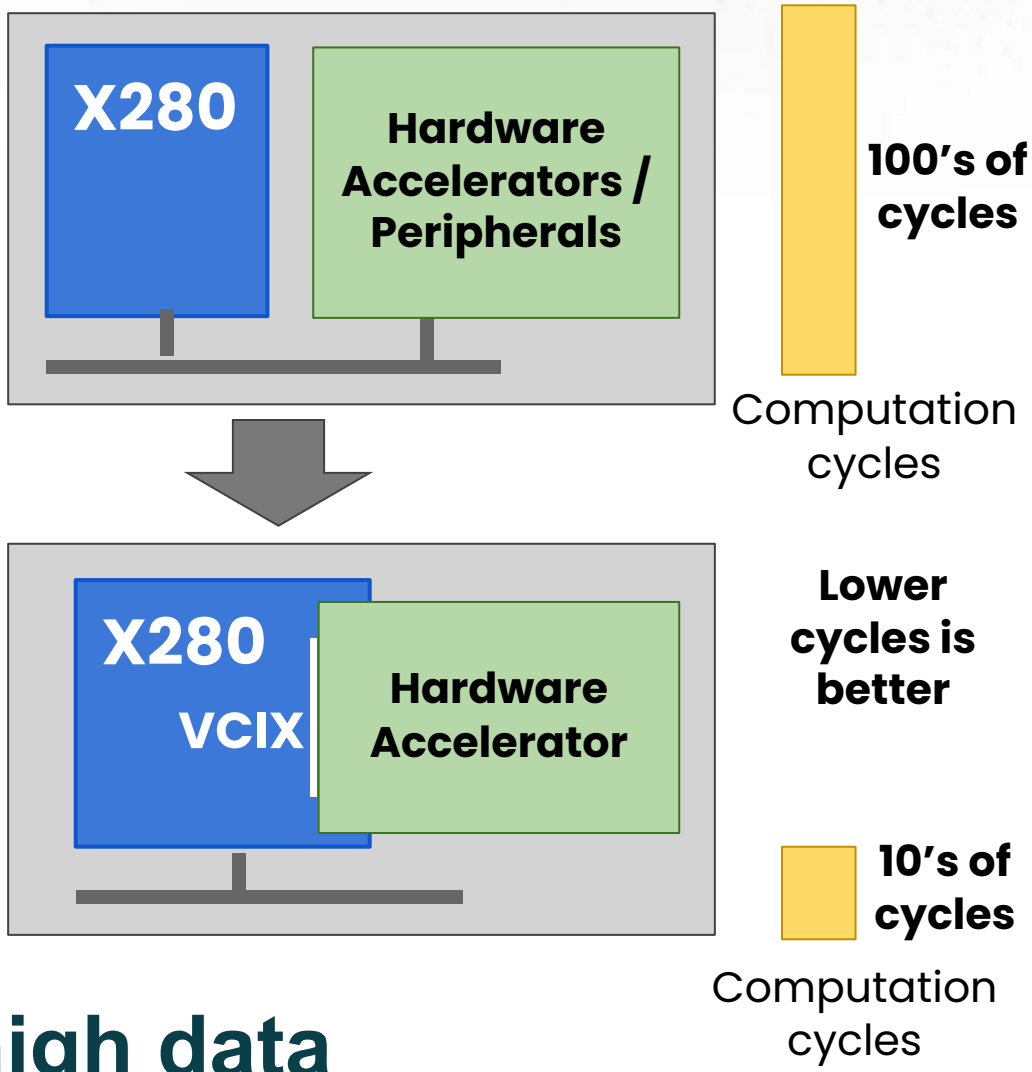


SiFive Intelligence X280 Market Applications

Consumer	Mobile	Edge	Data Center (Servers)
~0.1 - 2 TOPS	1 - 5 TOPS	1 - 20 TOPS	>100 TOPS
Imaging Processing (DSP & AI) Speech Recognition (DSP & AI)		**High-Performance Inferencing and Signal Processing**	**DL Training and Inference** High Performance Computing (HPC) Audio/Video Streaming /Compression Automotive

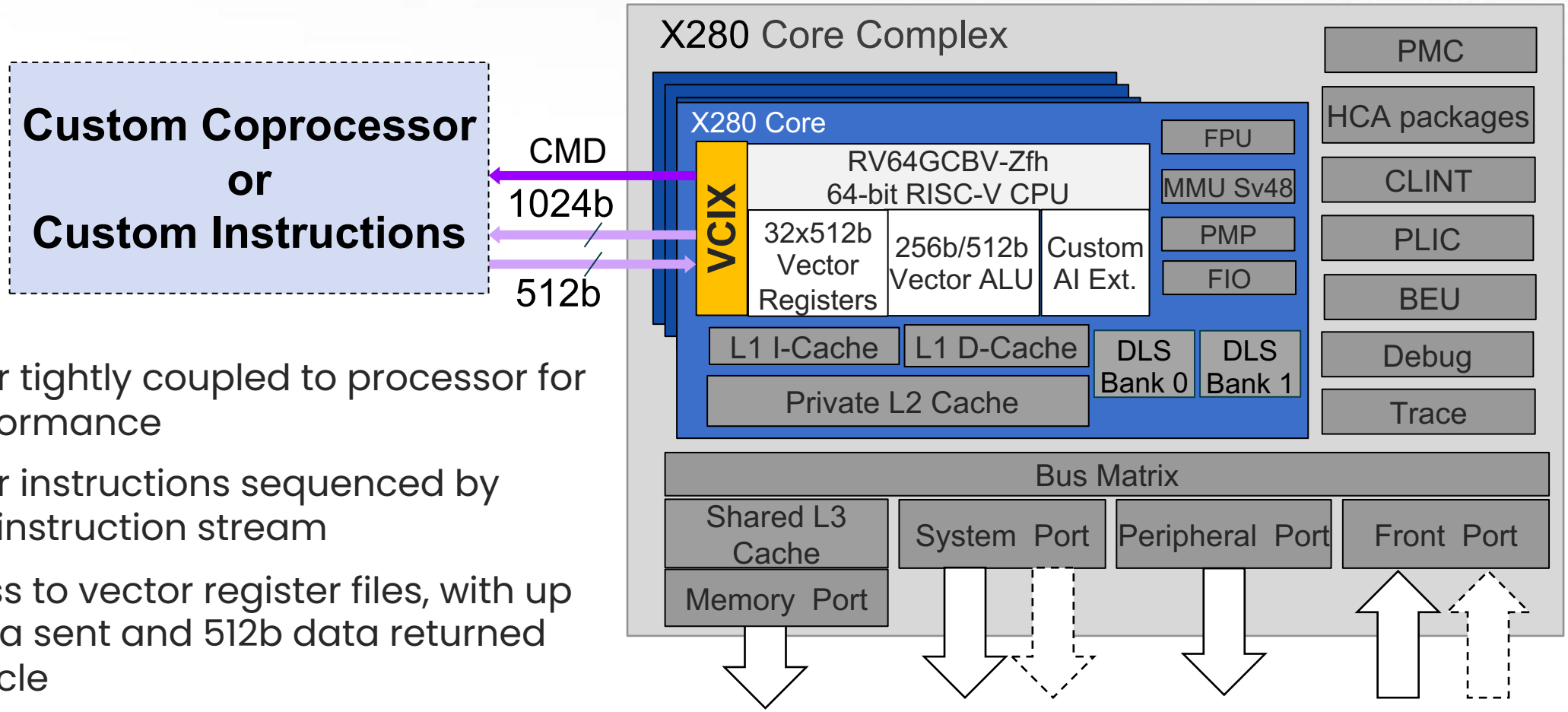
Vector Coprocessor Interface eXtension (VCIX)

- Strong demand for X280 coupled to hardware accelerators
- X280 “companion core” provides software and hardware “shell” for accelerator
- X280‘s benefit increased by bringing acceleration functionality into X280 core
- Easily add your **own vector instructions** and/or acceleration hardware to X280 vector processor
- Increase performance with custom instructions
  - FFT Butterfly, Matrix operations, Color Conversion, etc



Increased performance, high data bandwidth, low latency, simpler software

Vector Custom Coprocesor Interface (VCIX)



- Coprocessor tightly coupled to processor for highest performance
- Coprocessor instructions sequenced by processor's instruction stream
- Direct access to vector register files, with up to 1024b data sent and 512b data returned per clock cycle

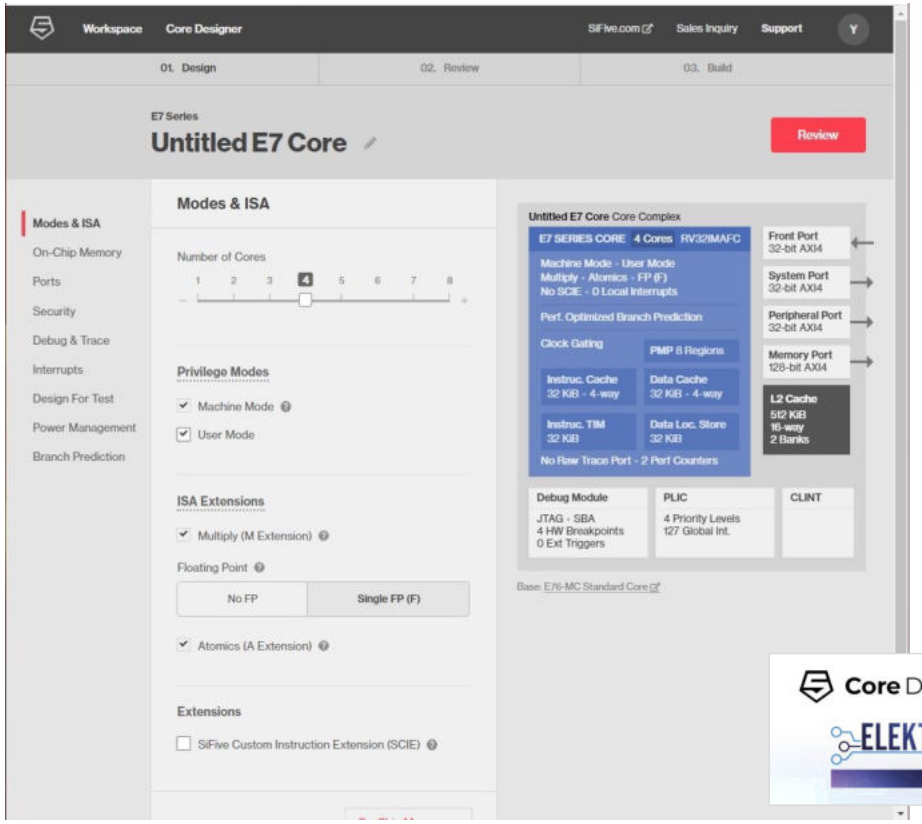
Bring Your Own Coprocessor (BYOC) into SiFive's Vector Machine while leveraging the entire RISC-V toolchain and software ecosystem!

DEMO: SiFive Core Designer

[Core designer demo]

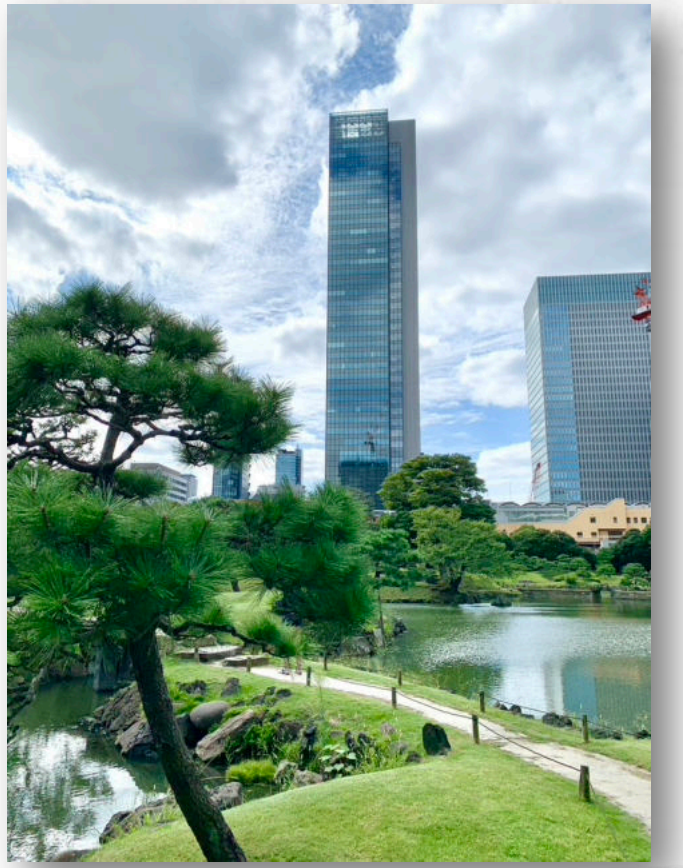
SiFive Core Designer

Optimize SiFive RISC-V Core IP for Your Application



- SiFive Core Designer enables configuration of SiFive RISC-V Core IP through an easy to use Web Portal
- **Variants** are generated with click of a button and are available from the Workspace
- **Variants** contain
  - RTL matching the configuration, including a testbench and other collateral needed to realize the design
  - Documentation specific to the design
  - Customized bare-metal BSP for easy

Contact us



We’d love to hear from you!

Get In Touch

Info-Japan@sifive.com

〒105-5117 東京都港区浜松町2-4-1

世界貿易センタービルディング南館 17F

Tel:03-4567-2840(代) Fax:03-4567-2601

SiFive

Thank you

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