Lowering Barriers to Chip Design
using OpenFASoC

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Our Research Group

- Open positions include Analog, Digital and Systems!

Lead Faculty

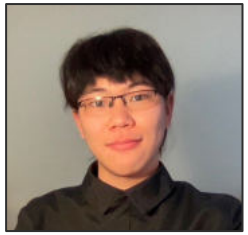
Mehdi Saligane

PostDoc

Dr. Chanho Kye

PhD Students

Ming-Hung Chen



Anhang Li

Ke-Haur Taur
(AMD)

MS and Undergrads

- Woobean Lee
- Ali Bilal
- Lucca Reinher
- Jianwei Zhang
- Sai Charan
- Ryan Wans
- Sihan Xie

Visiting Students

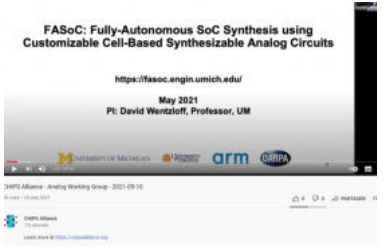
- Pranav Lulu (India)
- Ashbir Aviat (Japan)

Background

- DARPA IDEA Program (OpenROAD and FASoC)
- Multi-University and Industry effort
- Member of CHIPS Alliance

https://fasoc.engin.umich.edu/

CHIPS Alliance Workshop - October 12, 2021

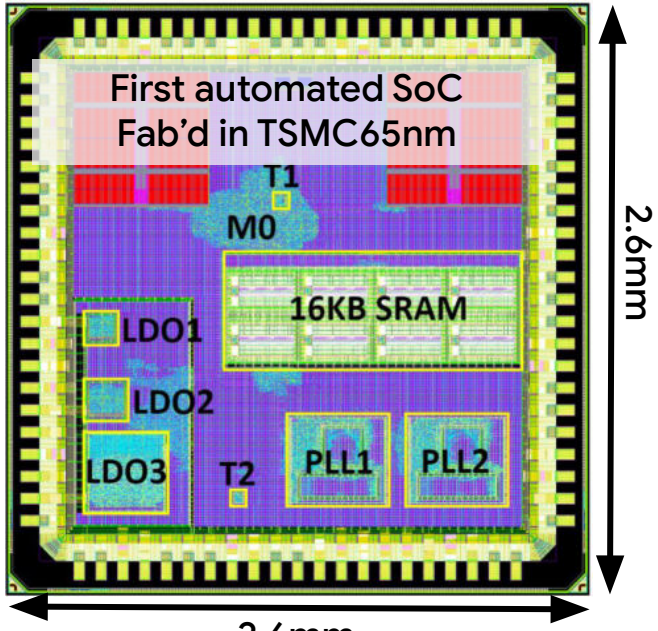


CHIPS Alliance - Analog Working Group - 2021-05-10

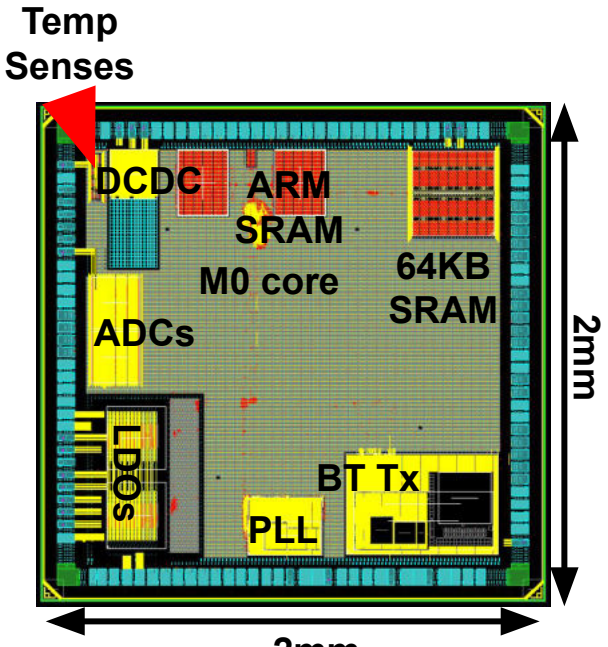
- *T. Ajayi et al, "Fully-Autonomous SoC Synthesis Using Customizable Cell-Based Analog and Mixed-Signal Circuits Generation", IFIP/IEEE VLSI SOC*
- *T. Ansell and M. Saligane, "The Missing Pieces of Open Design Enablement: A Recent History of Google Efforts : Invited Paper," 2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD), San Diego, CA, USA, 2020, pp. 1-8.*
- *Q. Zhang et al., "An Open-Source and Autonomous Temperature Sensor Generator Verified With 64 Instances in SkyWater 130 nm for Comprehensive Design Space Exploration," in IEEE Solid-State Circuits Letters, vol. 5, pp. 174-177, 2022..*

FASoC SoCs in TSMC 65 and GF12LP

- Multiple tape-outs in TSMC 65, GF12LP, SkyWater 130nm

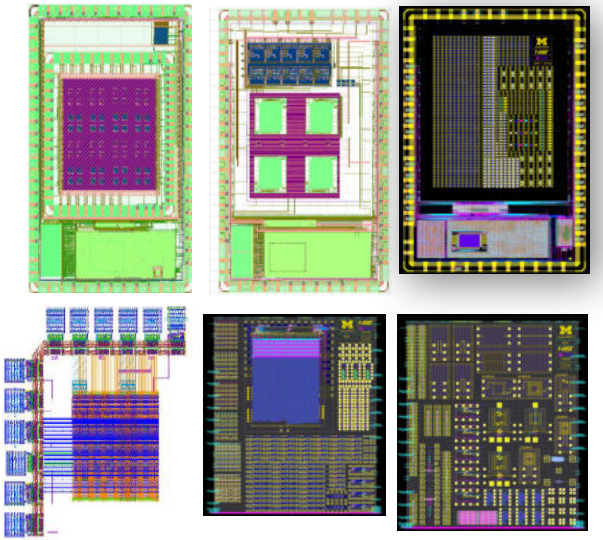


TSMC65LP SoC (2019-08)



GF12LP SoC (2020-10)

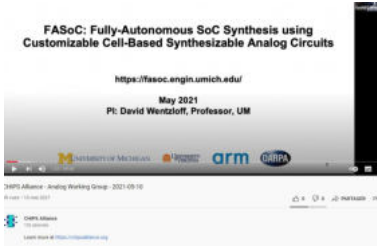
- GF12LP - 12nm FinFET
- GF 8HP - 130nm BiCMOS
- SKY130 - 130nm Bulk



(Open)FASOC Now

- Endorsed framework by CHIPS Alliance
- Analog Work Group
- Now Funded by Google, NIST and others

[CHIPS Alliance Workshop - October 12, 2021]



[CHIPS Alliance - Analog Working Group - 2021-05-10]

https://openfasoc.readthedocs.io/

- *T. Ajayi et al, "Fully-Autonomous SoC Synthesis Using Customizable Cell-Based Analog and Mixed-Signal Circuits Generation", IFIP/IEEE VLSI SOC*
- *T. Ansell and M. Saligane, "The Missing Pieces of Open Design Enablement: A Recent History of Google Efforts : Invited Paper," 2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD), San Diego, CA, USA, 2020, pp. 1-8.*
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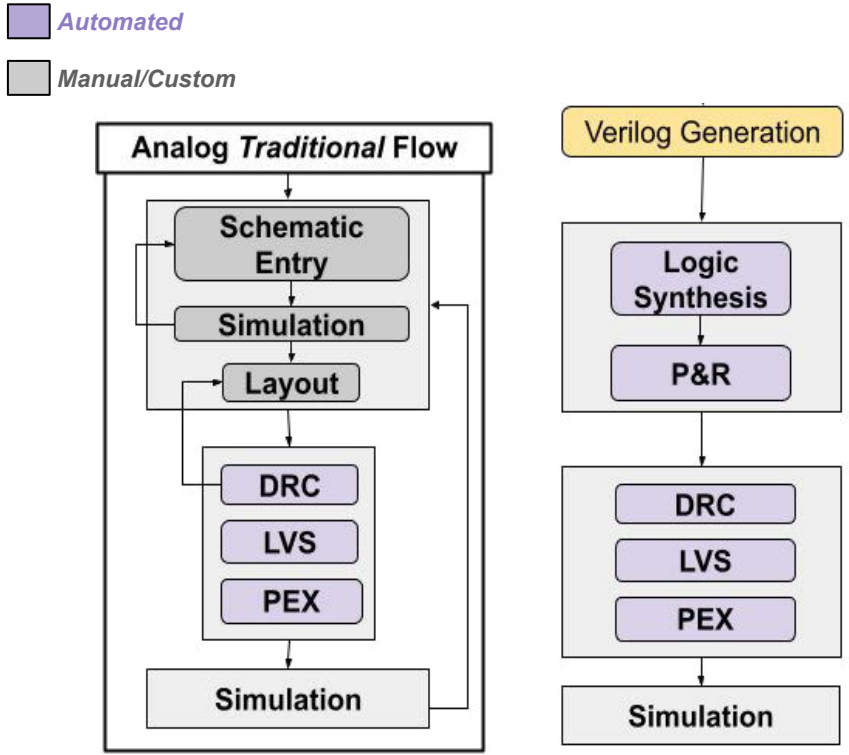
How it works:
Traditional vs Automated Chip Design

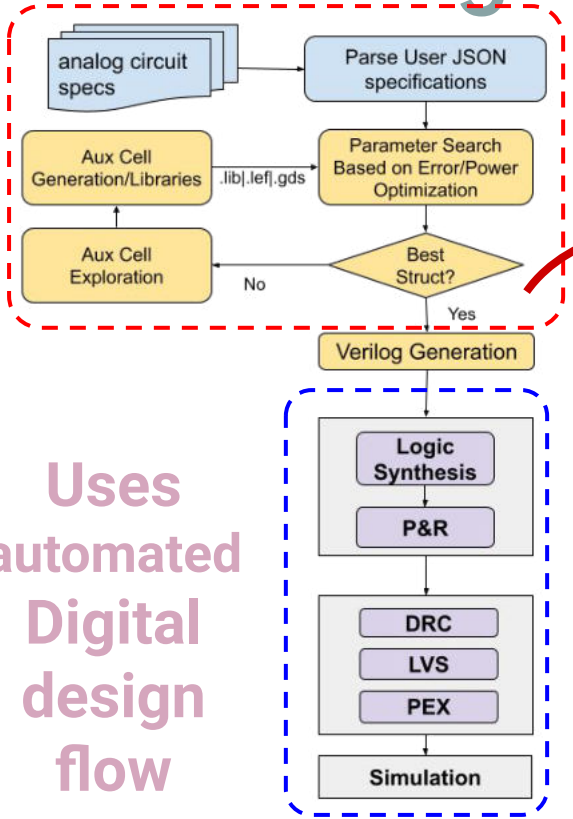
Analog vs. Digital design flow



- **Analog** design flow
  *Significant number of **manual** and custom steps.*
- **Digital** design (*grid-based*) flow
  *Almost **entirely automated**.*

Generated Analog *into* Digital design flow

FASoC Generator

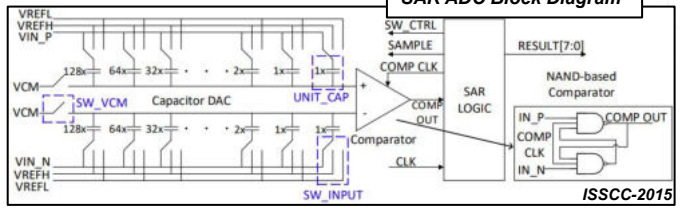


Automated

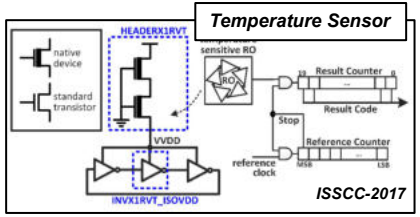
Manual/Custom

Uses automated Digital design flow

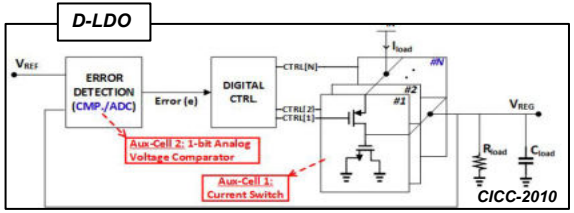
SAR ADC Block Diagram



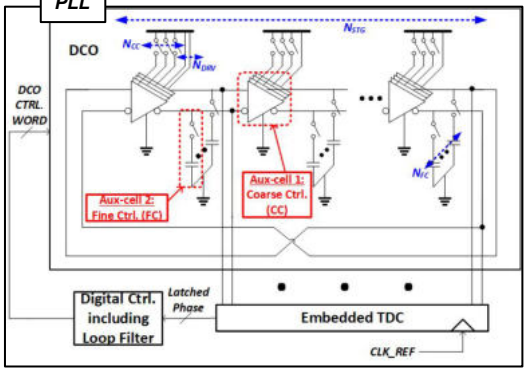
Temperature Sensor



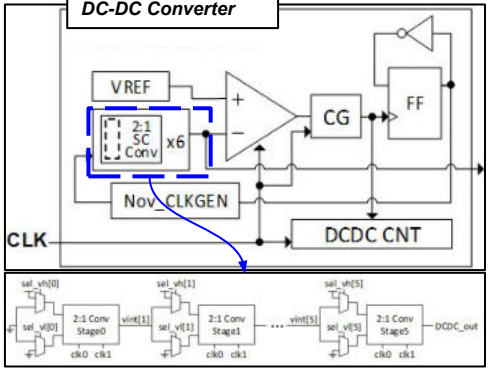
D-LDO



PLL

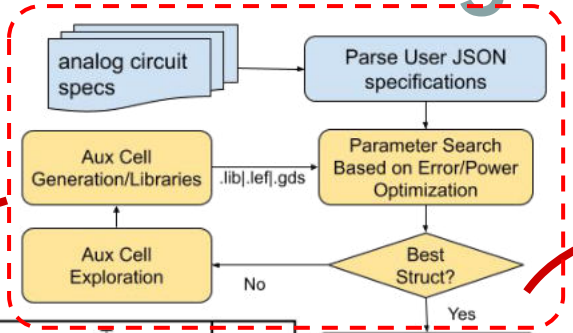


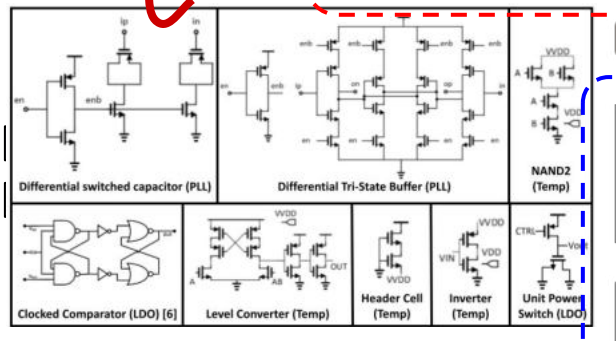
DC-DC Converter



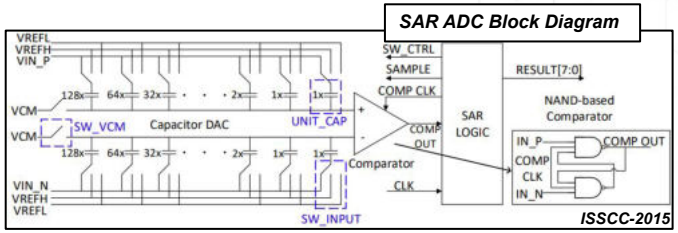
Generated Analog *into* Digital design flow

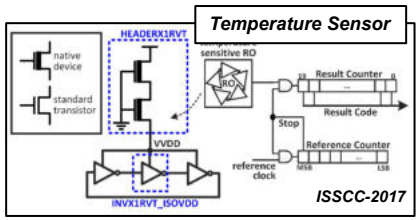
FASoC Generator

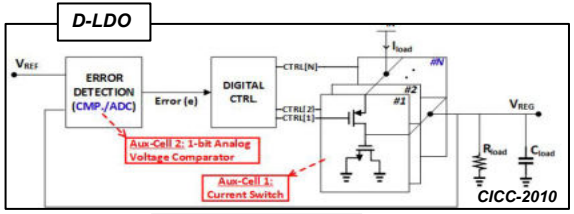


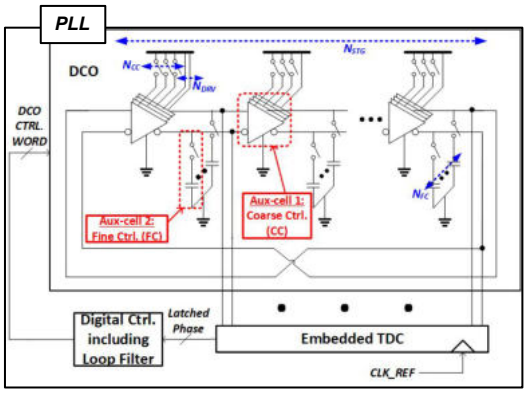


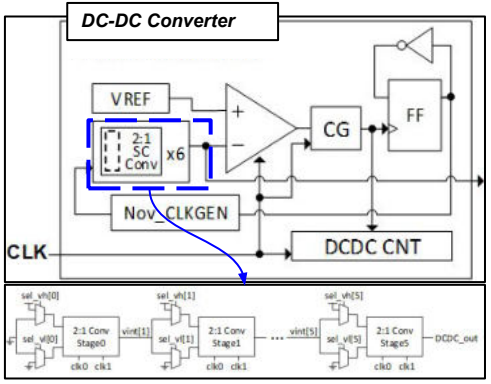
FASoC Aux Cells





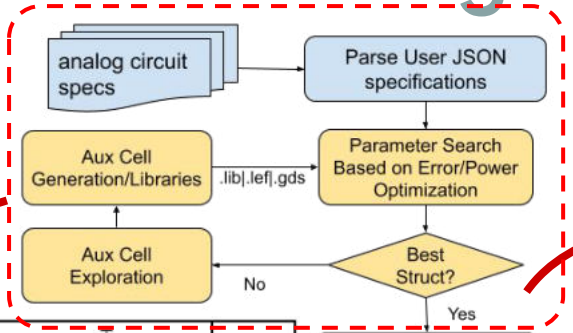


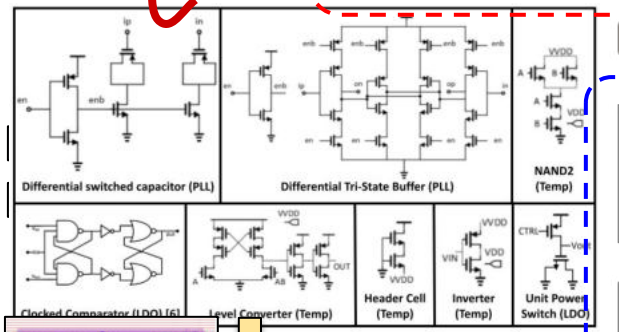




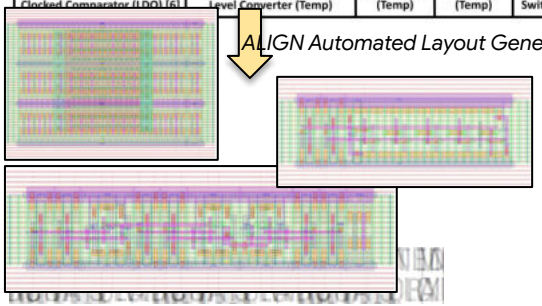
Generated Analog *into* Digital design flow

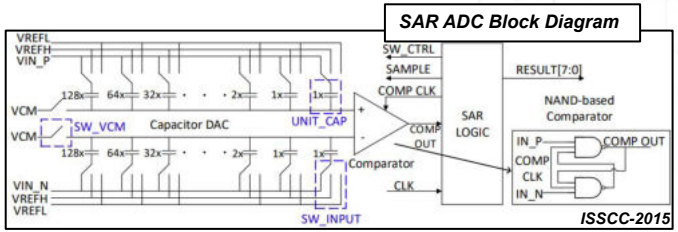
FASoC Generator

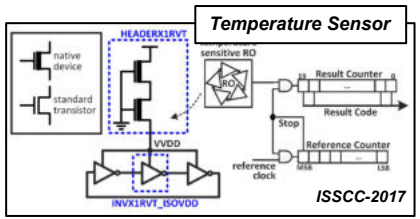


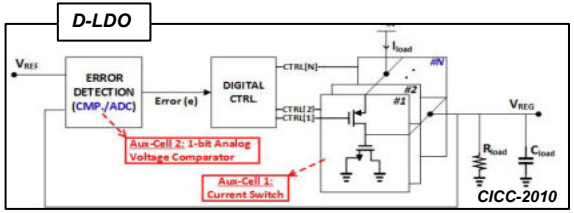


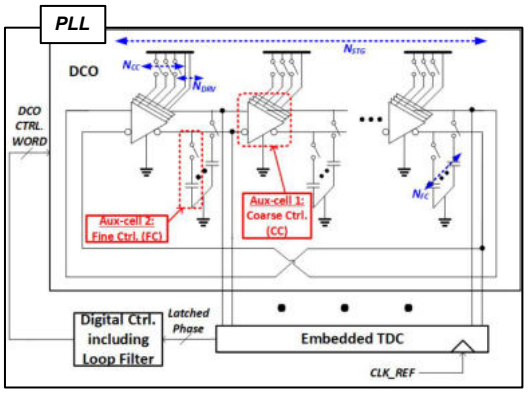
ALIGN Automated Layout Generator

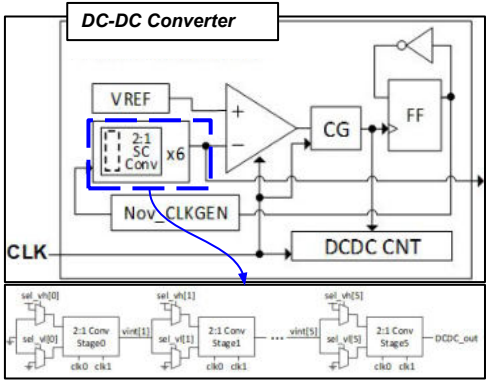




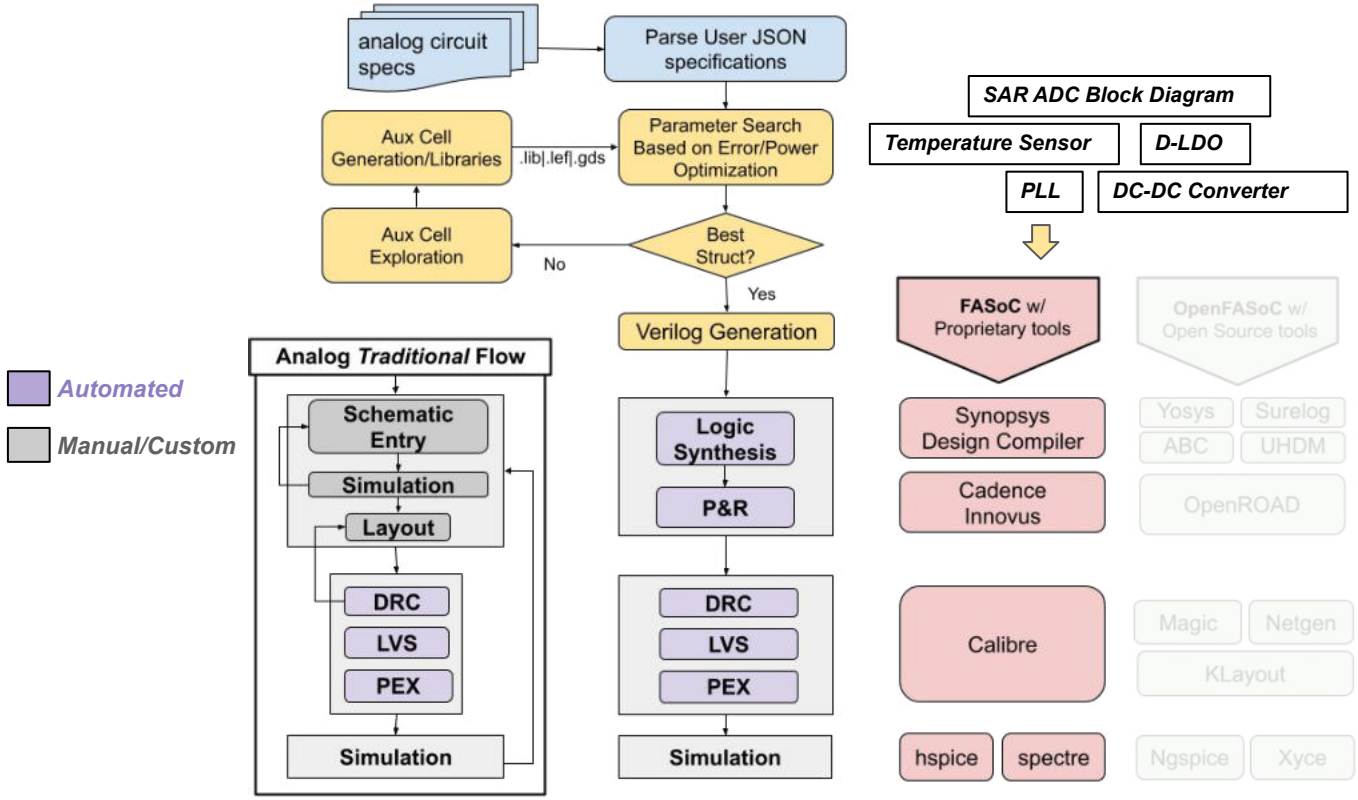




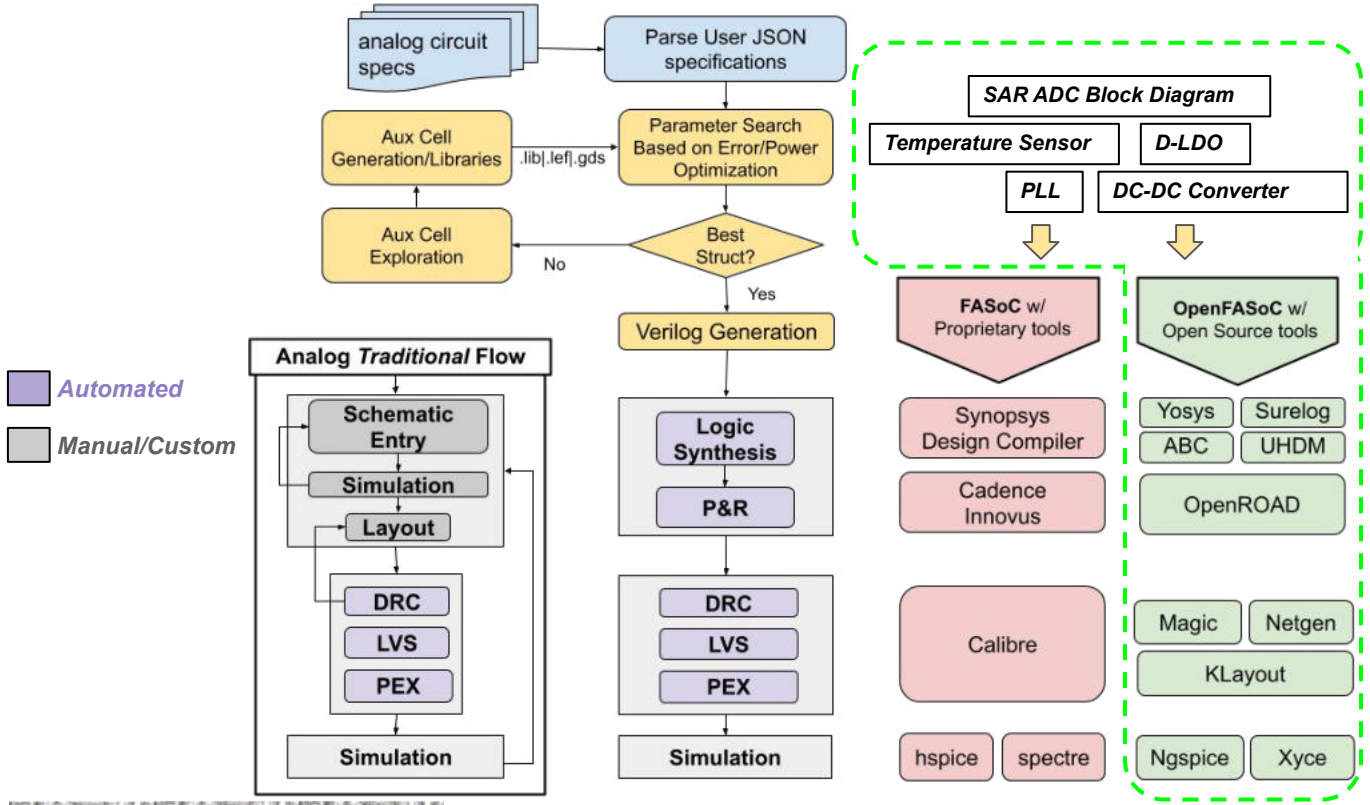




Initially only **proprietary** design flow



Now proprietary *or* **open source** design flow



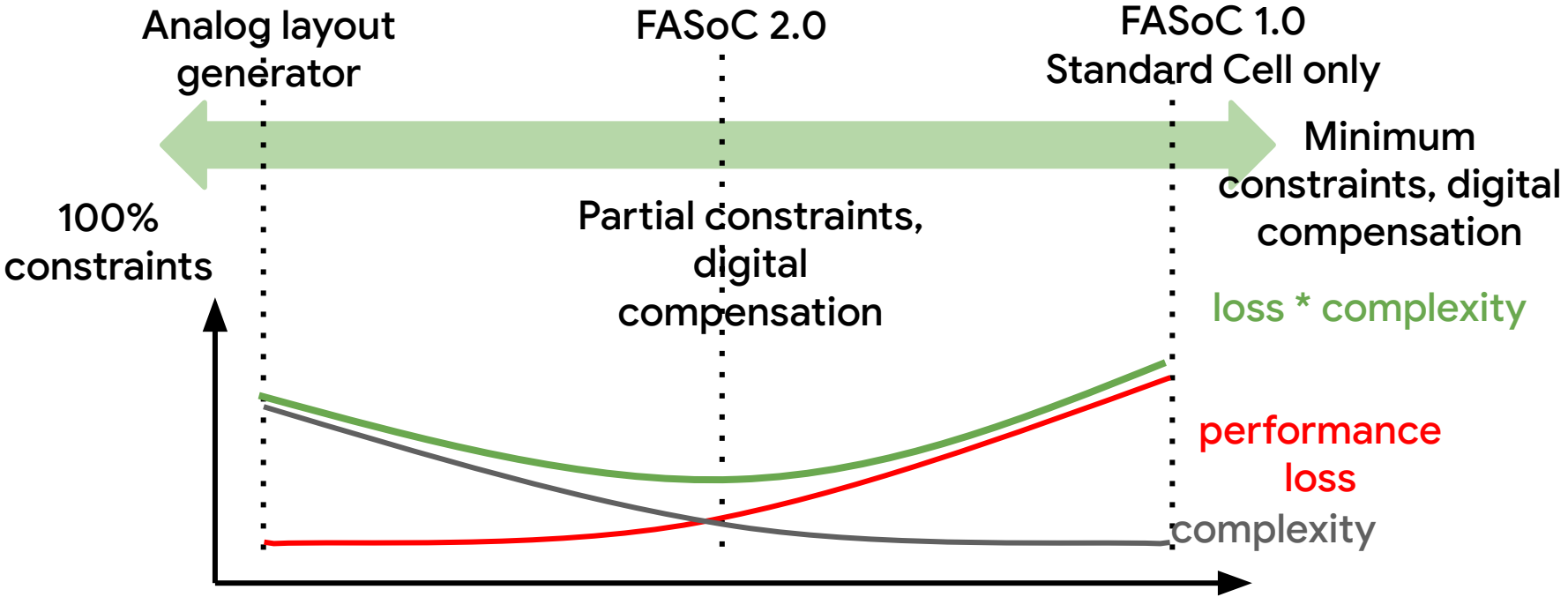
OpenFASoC!

Automated **portable** analog

Trade-offs and Examples

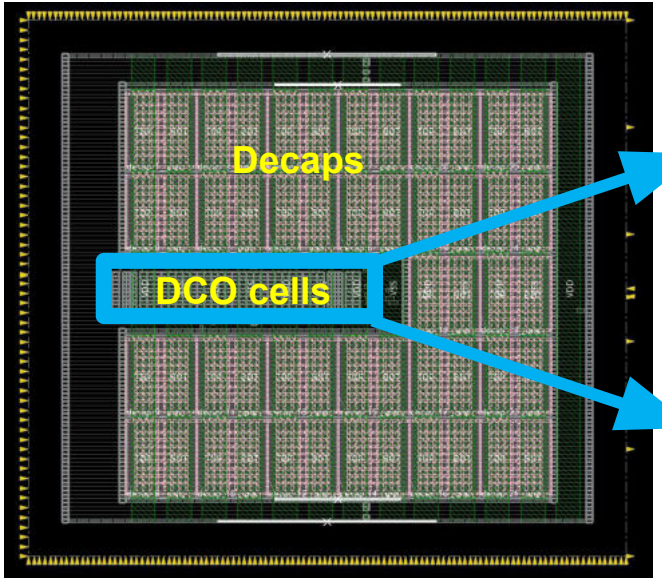
Performance / Complexity Tradeoff

- FASoC augments digital flow with APR tool placement/routing constraints and minimizes the (performance loss * complexity)



ADPLL (DCO) - Structured Placement Example

- Patterned placement information generated by python code ⇒ reduce delay mismatch between stages, added Decaps
- Scalable with design parameters



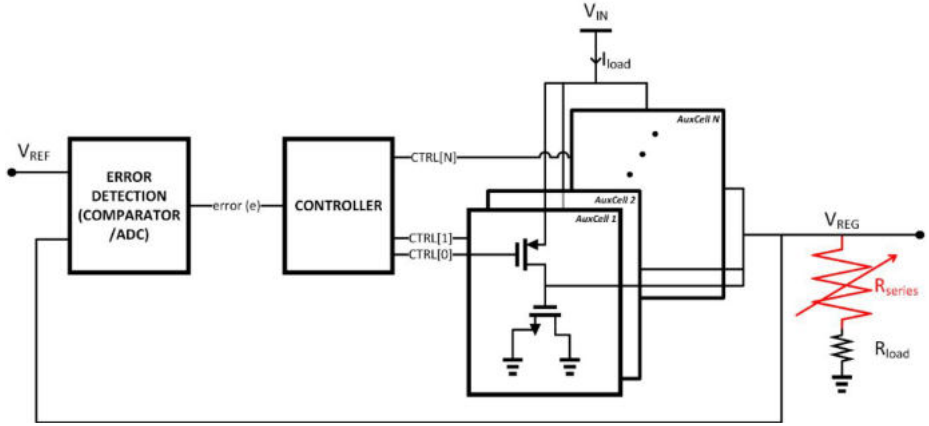
DCO placements with Decap

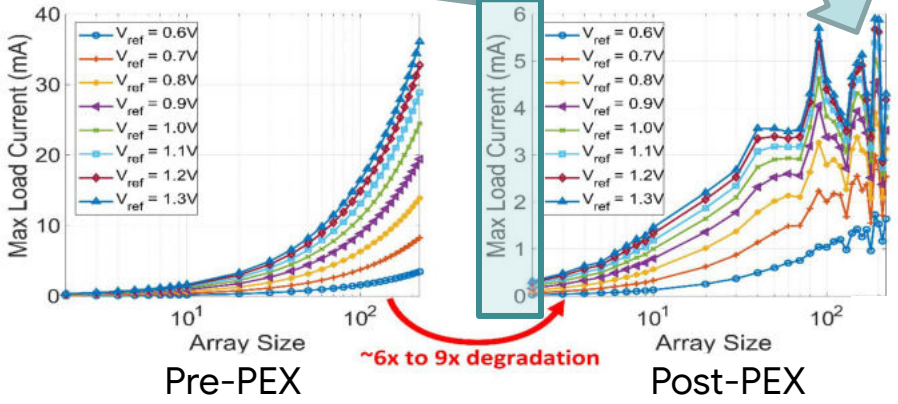
DCO cells

D-LDO Power Routing Example

Performance loss caused by PnR

- Large Series Resistance caused by wiring congestion for increased array size
- Unpredictable wiring due to random placement of power cells

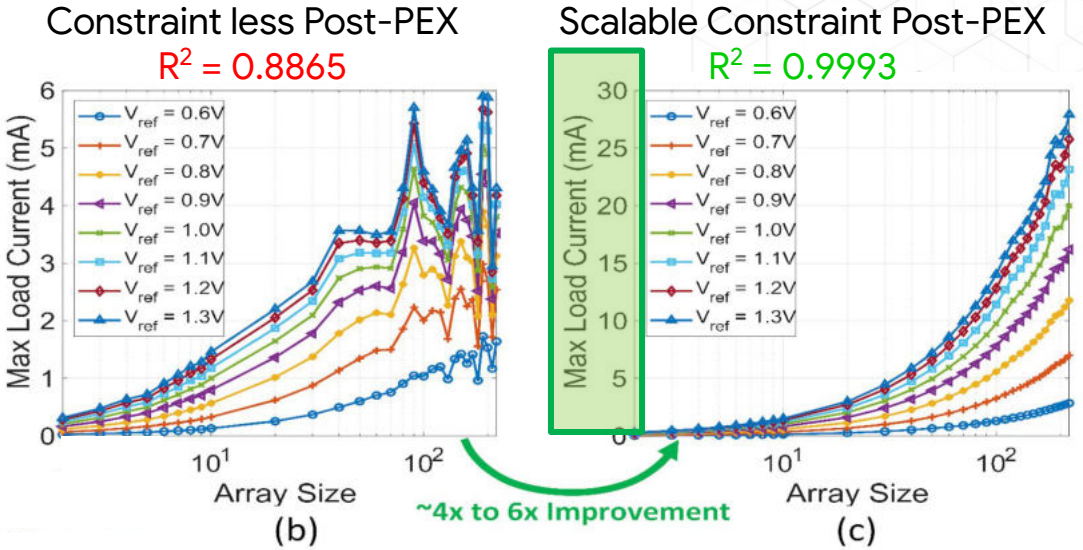


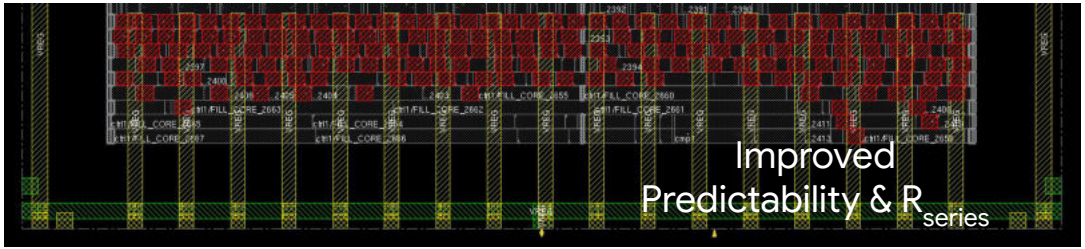


D-LDO Power Routing Example

Constraints to improve performance

- Technology agnostic fencing to constraint placements
- Use power stripes to improve series R problem
- Automatic analysis of technology database file for determining the stripe metal layers
- Taped out in BiCMOS and bulk 130nm, TSMC 65LP and GF12LP

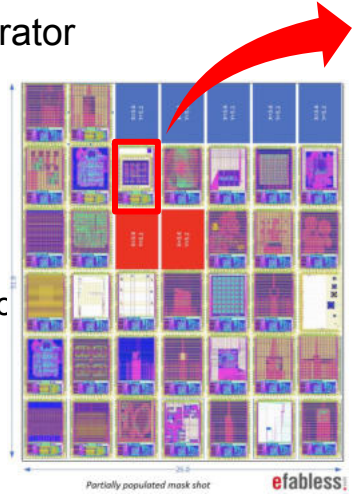


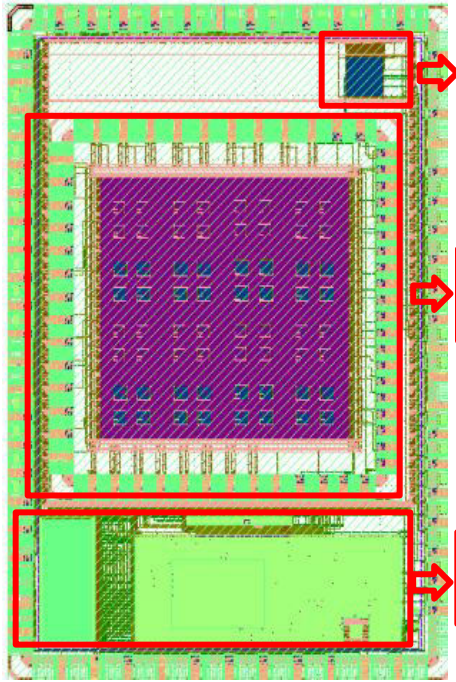


Open Source IC contributions (tapeouts)

OpenFASOC on MPW-I: 64 sensors + D-LDO

- Actively contributing to the open source community
- 1st open FASoC flow built on top of OpenROAD tools
  - Focused on the Temp. Sensor Generator
- FASoC testchip in SKY130:
  - Includes Caravel SoC
  - 64 Temp. Sensor Mesh
  - LDO ported (~ a week)
    - Updated strongArm latch
    - 5v native NMOS switch





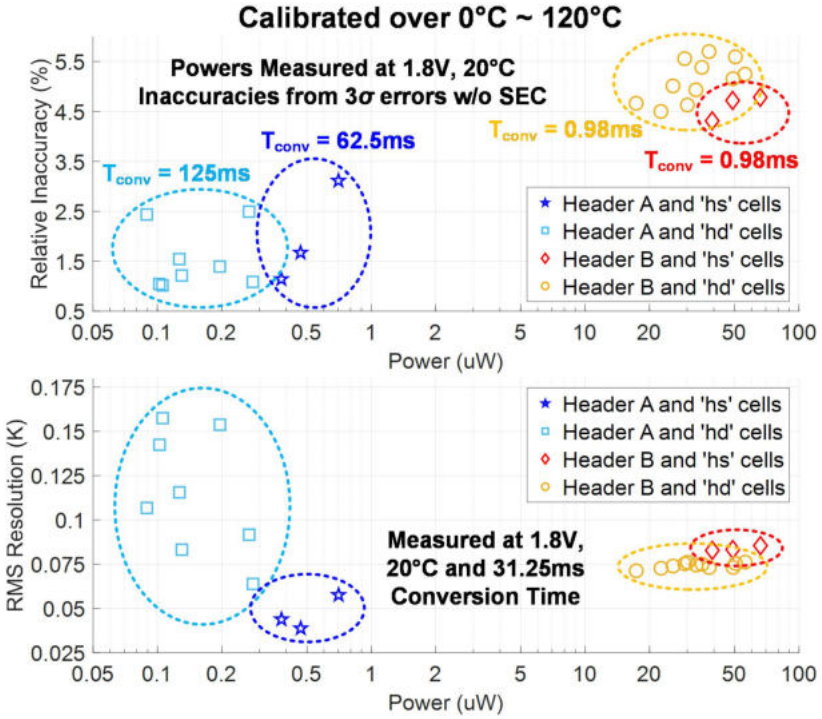
Test-chip in MPW-I

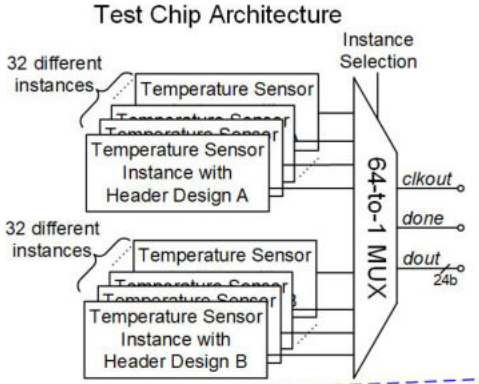
Open MPW Shuttle Program

efabless Sponsored by Google

MPW-I Measurement Results

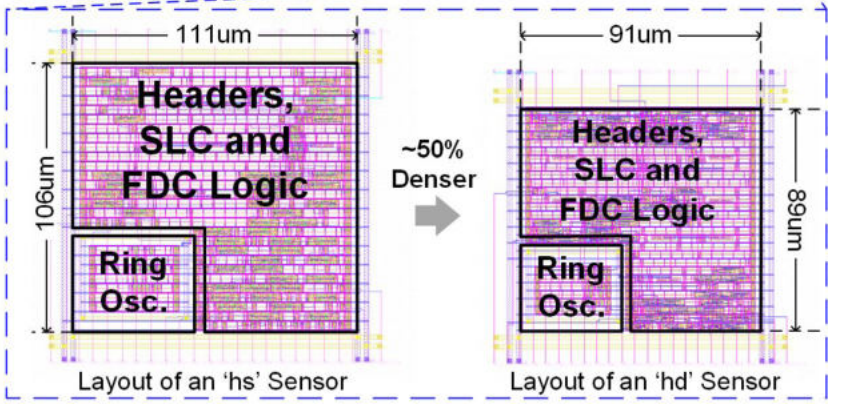
- 64 sensors array used for low-cost design space exploration





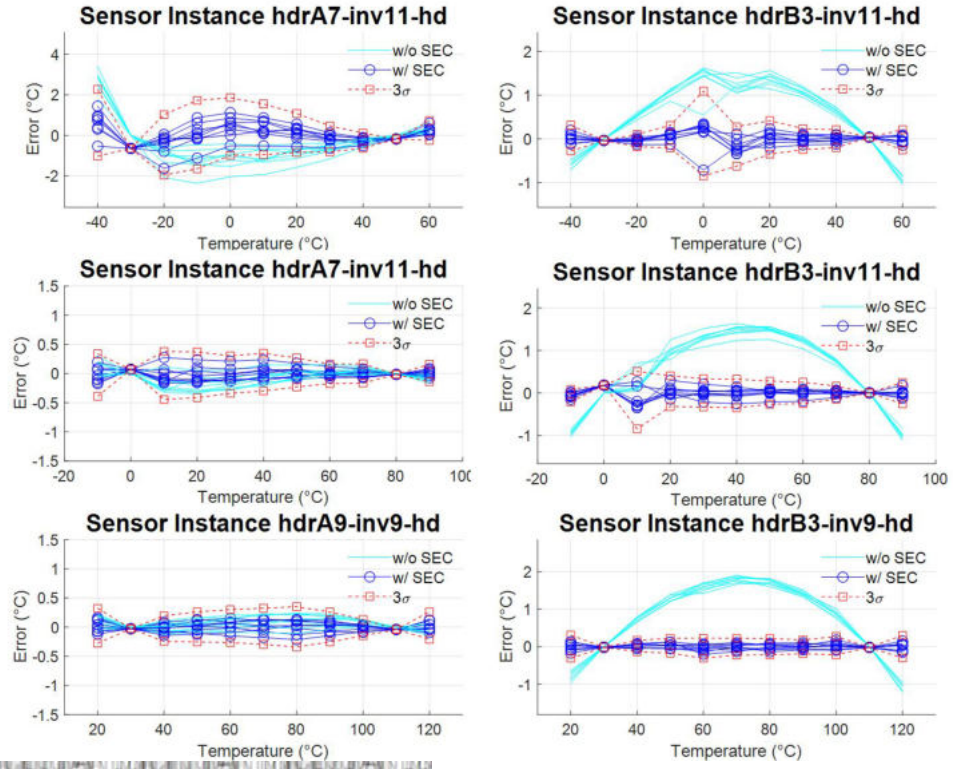
Design Space Explorations

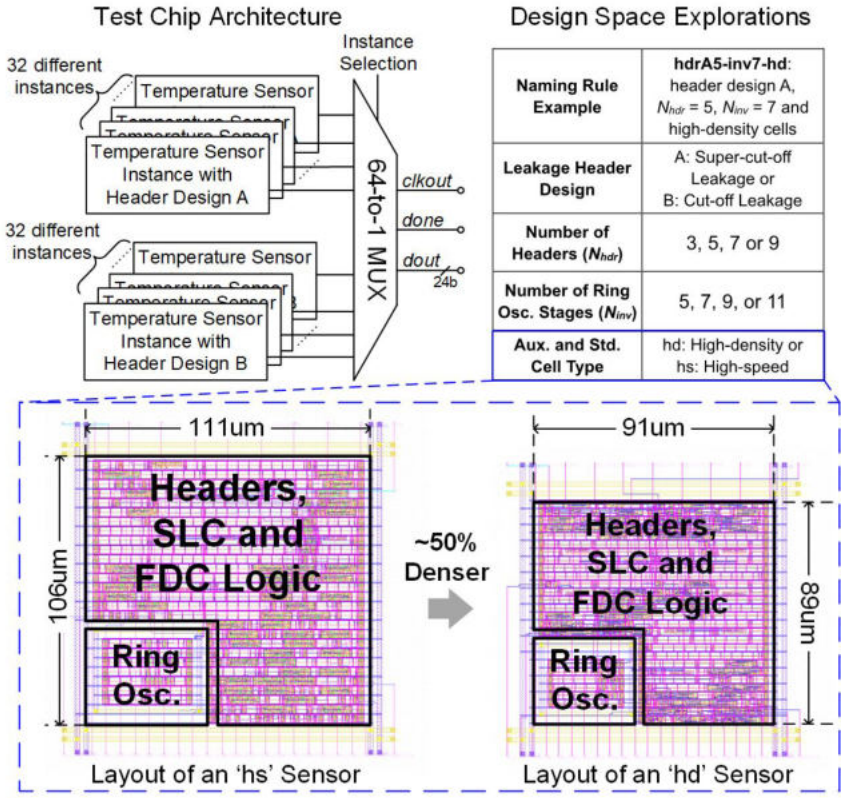
Naming Rule Example	**hdrA5-inv7-hd**: header design A, N_{hdr} = 5, N_{inv} = 7 and high-density cells
Leakage Header Design	A: Super-cut-off Leakage or B: Cut-off Leakage
Number of Headers (N_{hdr})	3, 5, 7 or 9
Number of Ring Osc. Stages (N_{inv})	5, 7, 9, or 11
Aux. and Std. Cell Type	hd: High-density or hs: High-speed



MPW-I Measurement Results

- Below 1 °C inaccuracy and SOTA results

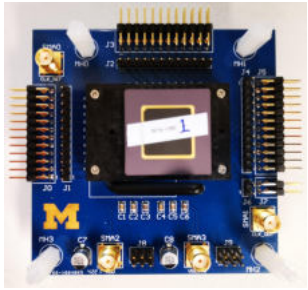


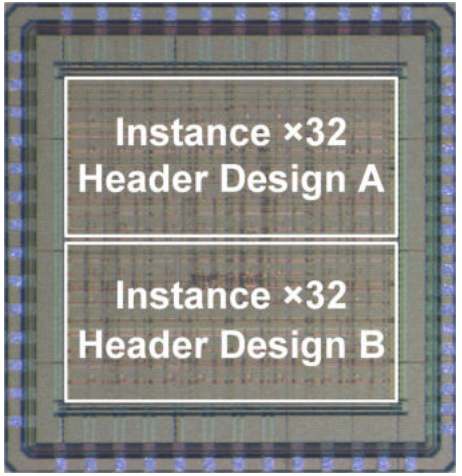


MPW-I Measurement Results

- Results Summary and Comparison Table
- Published at the Solid-State Circuits Letters!

	This Work			JSSC '20 [5]	JSSC '19 [6]	CICC '18 [7]	ISSCC '17 [4]
	B3-hd-11	**A9-hd-7**	**A7-hd-9**				
Technology	**SkyWater 130nm (Open-source PDK)**			55nm	65nm	180nm	180nm
Generator-based Design	**Yes**			No	No	No	No
Supply Voltage (V)	**1.8V**			0.8 ~ 1.3	0.5	0.8 ~ 1.4	1.2
Area (μm^2)	**8095**			1770	630000	65000	8865
Temperature Range (°C)	**-40 ~ 80**	**-20 ~ 100**	**0 ~ 120**	-40 ~ 125	0 ~ 100	-20 ~ 80	-20 ~ 100
Conversion Time (ms)	**0.98**	**125**	**125**	1.31	300	840	8
Inaccuracy (°C)	**-0.97/1.08 3σ**	**-0.59/0.61 3σ**	**-0.67/0.74 3σ**	-0.7/0.7 3σ	-1.53/1.61 Min./Max.	-0.7/+1.3 Min./Max.	-0.22/0.19 3σ
Relative Inaccuracy	**1.71%**	**1.00%**	**1.18%**	0.85%	3.14%	2.00%	0.35%
Power (μW)	**17.33**	**0.25**	**0.13**	9.3	0.000763	0.0013	0.075
Energy/Conv. (nJ)	**16.92**	**31.38**	**16.25**	12.2	0.23	11	0.6
Resolution (mK)	**78**	**21**	**24**	16	300	110	73
Resolution-FoM ($pJ \cdot K^2$)	**101.9**	**13.4**	**9.7**	3.1	20.7	140	3.2

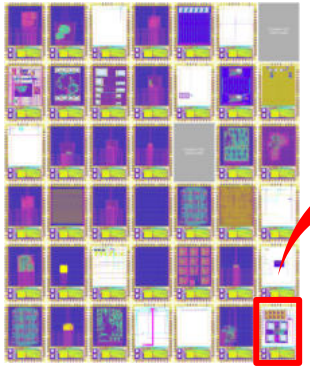


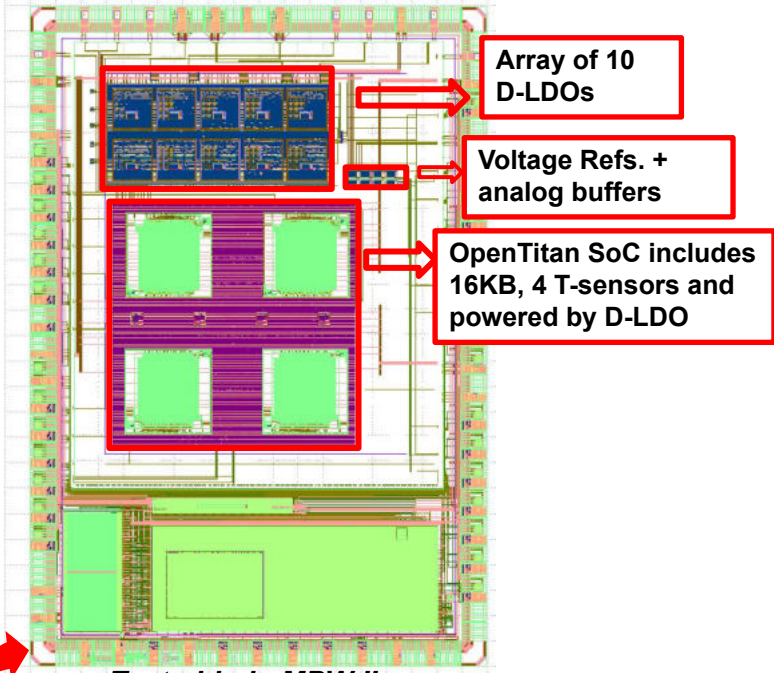


OpenFASOC on MPW-II: 1st Open Source AMS SoC

- Included initial support for voltage domains in OpenROAD
- Implementation of the OpenTitan SoC using an ECO flow to fix hold timing with degrading the F_{MAX}
- Temperature Sensor generator is using an end-to-end Open Source flow
- Updates to the D-LDO generator:
  - Embedded voltage references
  - Decap cells using MIM cap.
  - Multiple implementations and I_{LOAD}

- https://efabless.com/projects/239
- https://github.com/msaligane/caravan_openfasoc.git





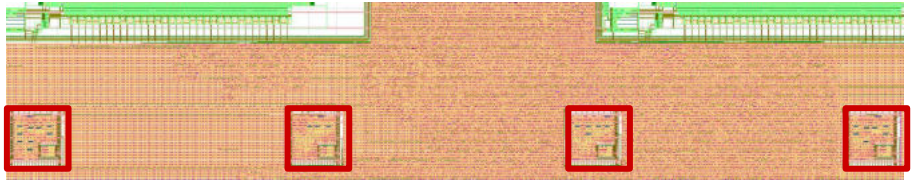
Test-chip in MPW-II

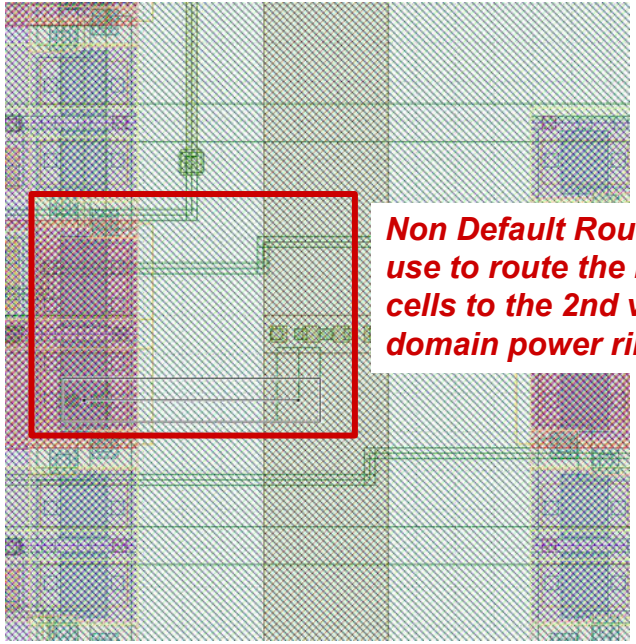
Open MPW Shuttle Program

efabless
Sponsored by Google

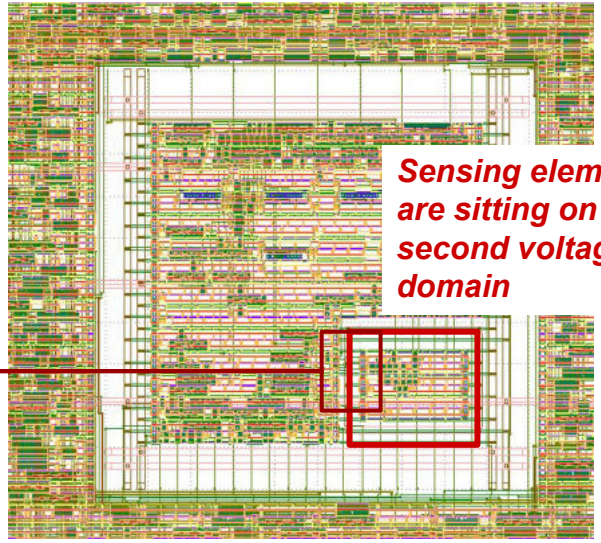
OpenFASOC on MPW-II: Integrated Temperature Sensors

Sensors are embedded inside the OpenTitan SoC and connected through tilelink

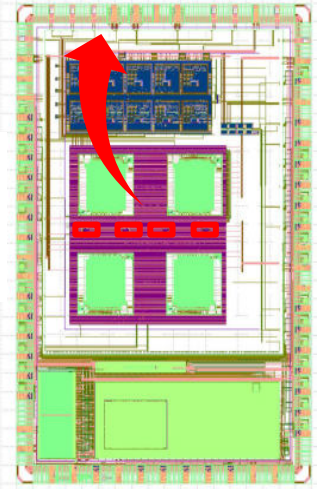




Non Default Routing is use to route the header cells to the 2nd voltage domain power ring

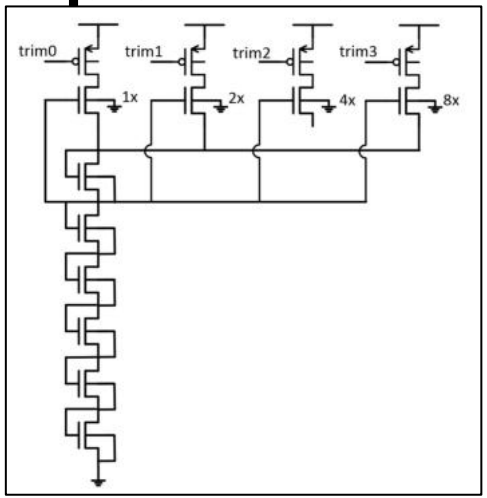


Sensing elements are sitting on a second voltage domain

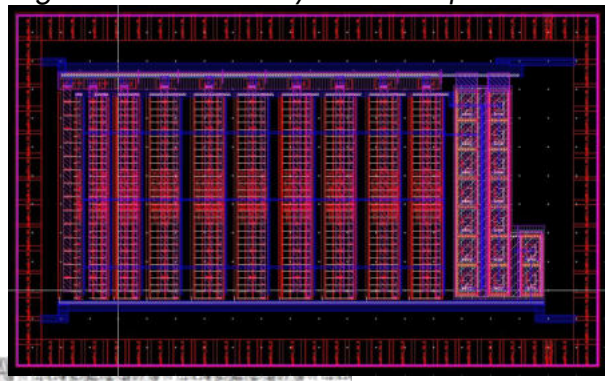


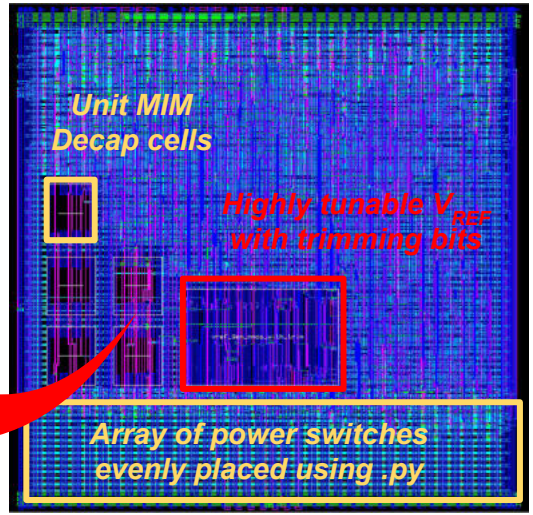
The temperature sensor generator uses a fully open source flow

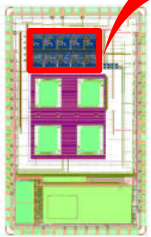
OpenFASOC on MPW-II: D-LDO generator

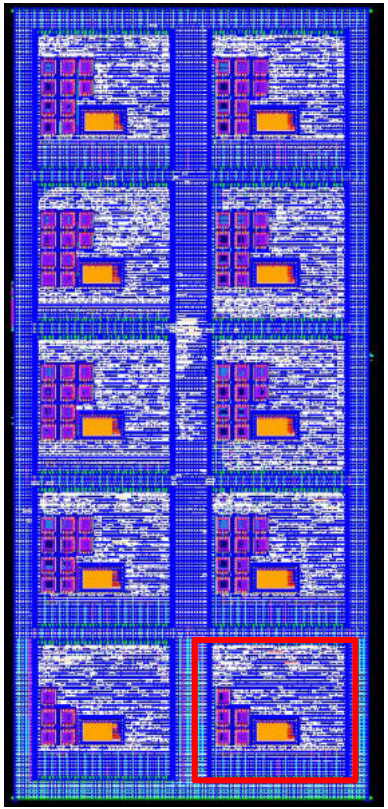


Voltage Reference with symmetrical placement





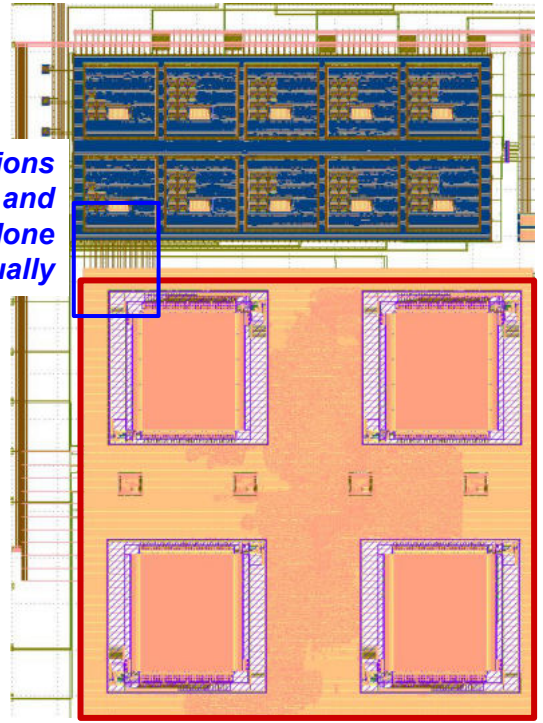




Array of D-LDOs

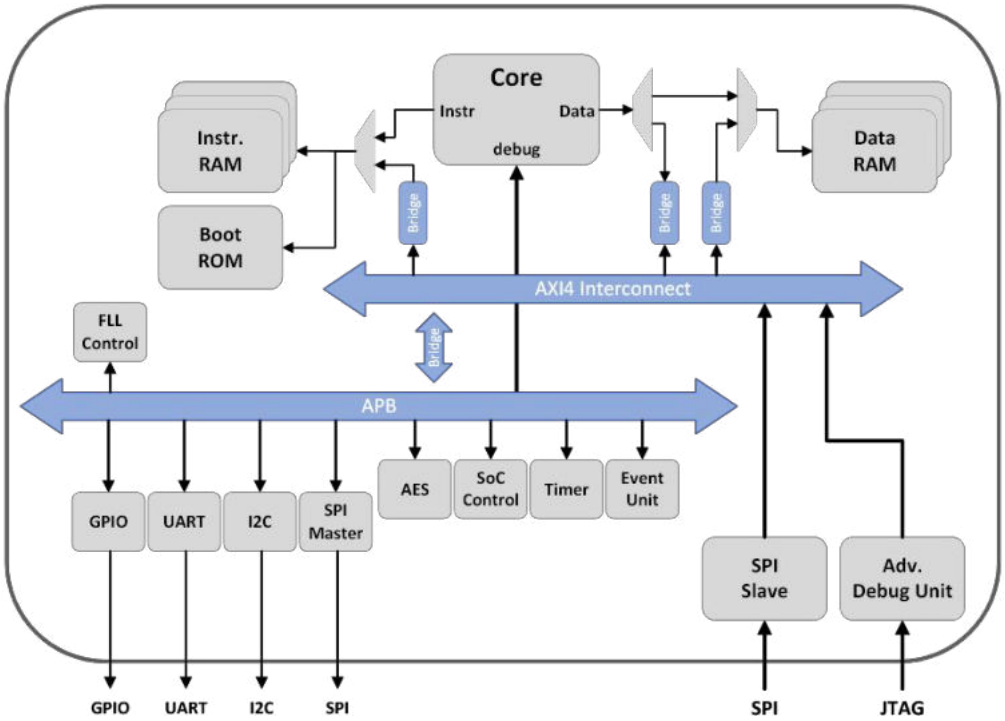
OpenFASOC on MPW-II: OpenTitan SoC

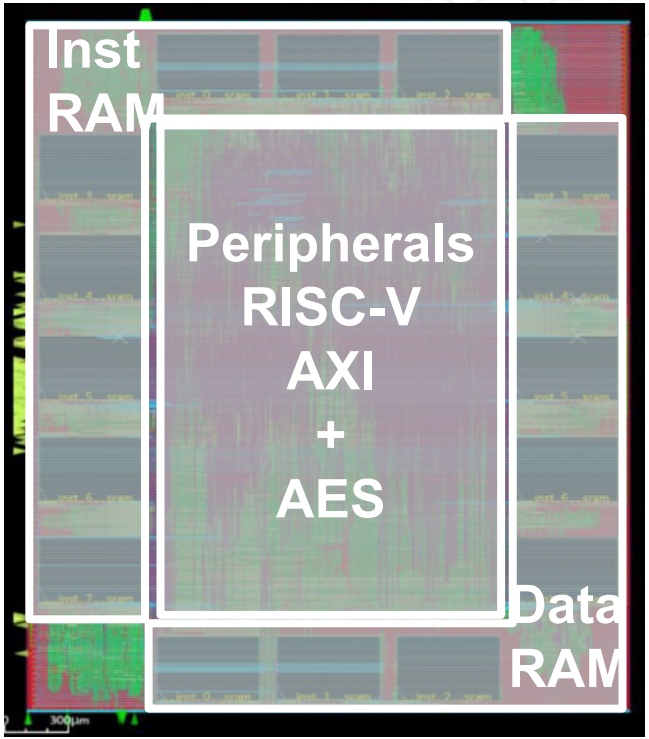
- 1st SoC using AMS components
- The Opentitan SoC contains
  - UART, SPI interfaces
  - 16KB of SRAM (OpenRAM)
  - D-LDO is used to power-up all the blocks
  - All Peripherals are connected through Tilelink
- Timing has been carefully checked and an ECO flow has been used to avoid altering the F_{MAX} while fixing hold violations



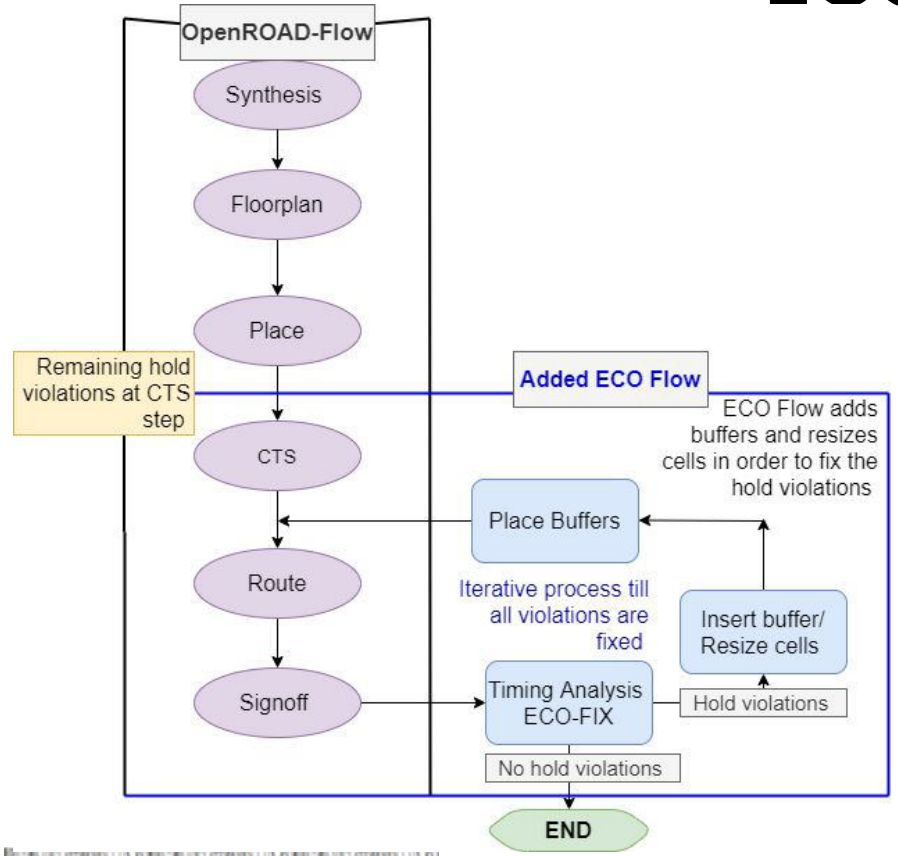
OpenTitan AMS SoC - Die Photo

Open Source RoT (PULP) on MPW-6





OpenFASOC on MPW-II: OpenTitan SoC - ECO flow



- Custom automated ECO flow to close timing
- Modular flow using both proprietary and open source tool based flows

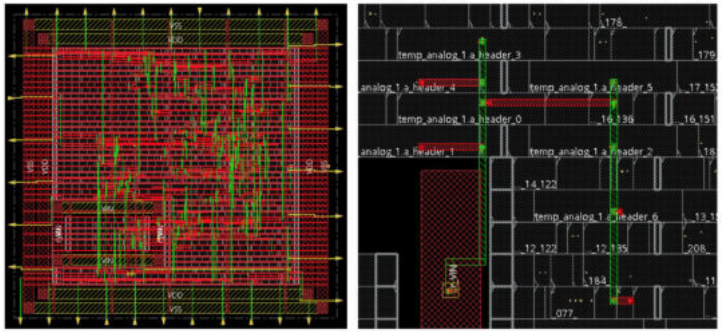
	OpenROAD flow	OpenROAD + ECO
Clock (ns)	48	48
Fmax (MHz)	20.8	20.8
Setup Time (ns)	11.01	9.44
Hold Time (ns)	-1.72	0.01
No of violations	1493	0
No of iterations for ECO	0	5

Hold fixing table with and without ECO

OpenFASOC on MPWs: OpenROAD tooling

- The OpenROAD's team is actively improving their tools and adding new design features
- Closely working with UCSD and ARM to enable an AMS flow (power gating, UPF flow)

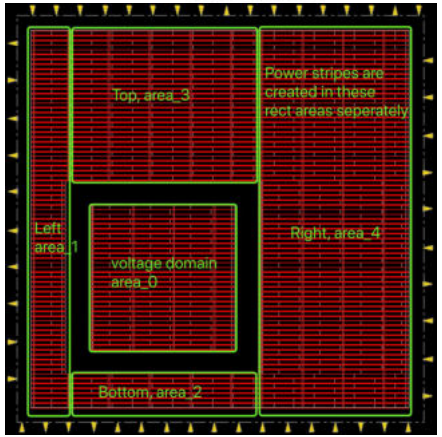
Custom nets python scripts are used for special routing



Layout view Custom net

Example of code updates to create new PD features

File name	Func/Proc
OpenROAD/src/init_fp/src/InitFloorplan.cc (Floorplan)	updateVoltageDomain()
OpenROAD/src/pdngen/src/PdnGen.tcl (Floorplan)	generate_stripes{}
OpenROAD/src/replace/src/replace.tcl (Placement)	global_placement{}



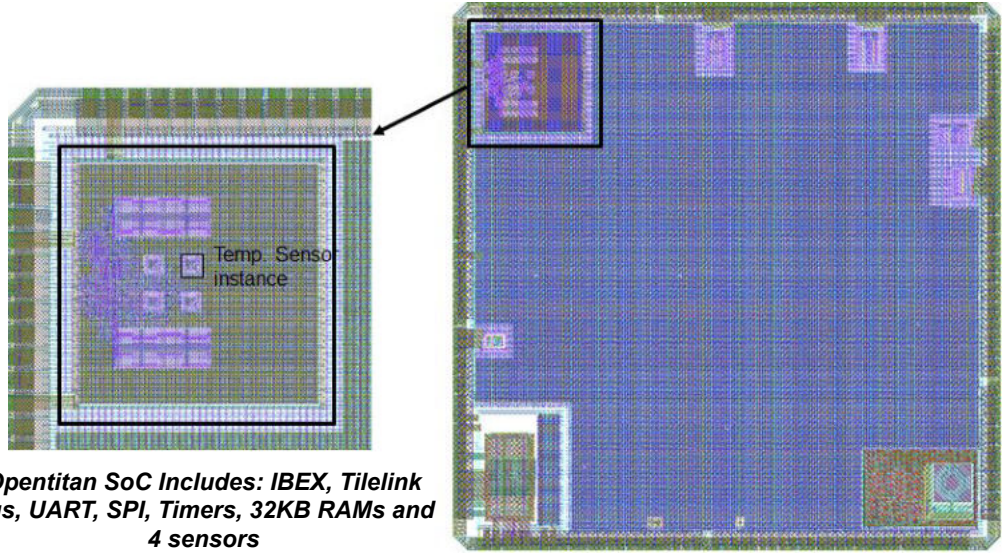
Example of `create_voltage_domain` usage

Tape Outs in GF12LP - OpenTitan SoC

- 1st tapeout in GF12LP using OS tools (OpenROAD)
- PD and timing optimization using OpenROAD
- Used a modular flow to smoothly fill-in the gaps using proprietary tools

- Signoff using PT
  - @ TT|25C|0.8v|funcmax
    - 350MHz

- Temperature sensors
  - T_{RANGE}: -20 to 100°C
  - Error: +/- 0.2°C (post-PEX)



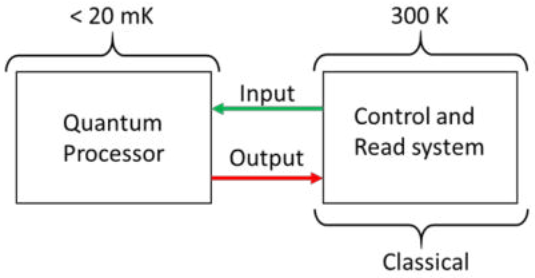
Opentitan SoC Includes: IBEX, Tilelink bus, UART, SPI, Timers, 32KB RAMs and 4 sensors

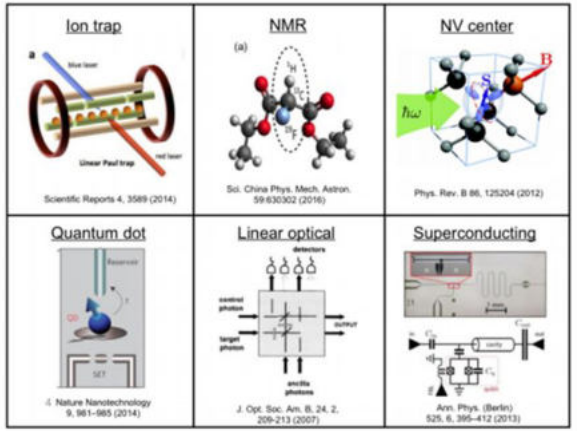
Die Photo of FASoC's 2021 testchip in GF12LP Including RAMs, LDOs, BLE, CDC and an OpenROAD based implementation of the Opentitan SoC

Taped-out Teststructures using OpenFASOC

Control Electronics for Quantum Computers

Quantum computer: < 20 mK





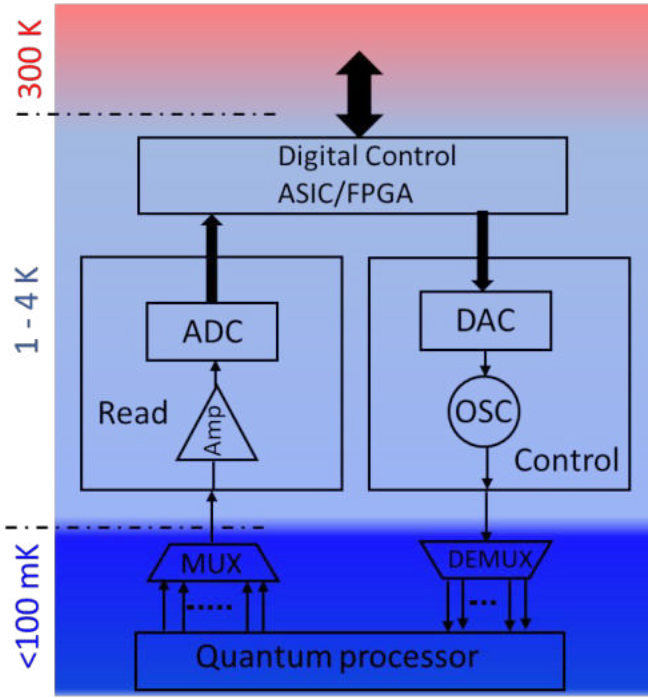
Mix of AC and DC signal required to control and read the Qubits

Digital

- Inverters, ring oscillators

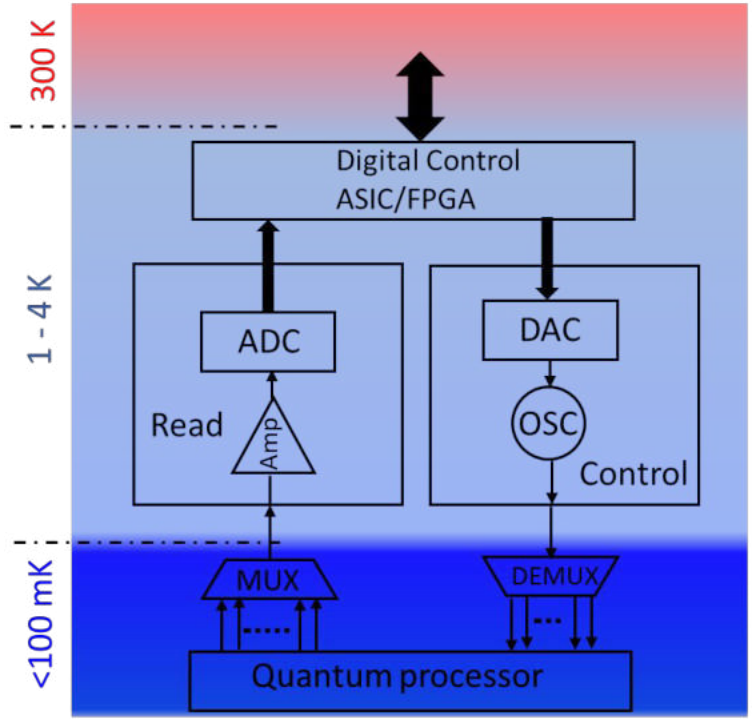
Analog

- Voltage reference, Low Noise Amplifiers

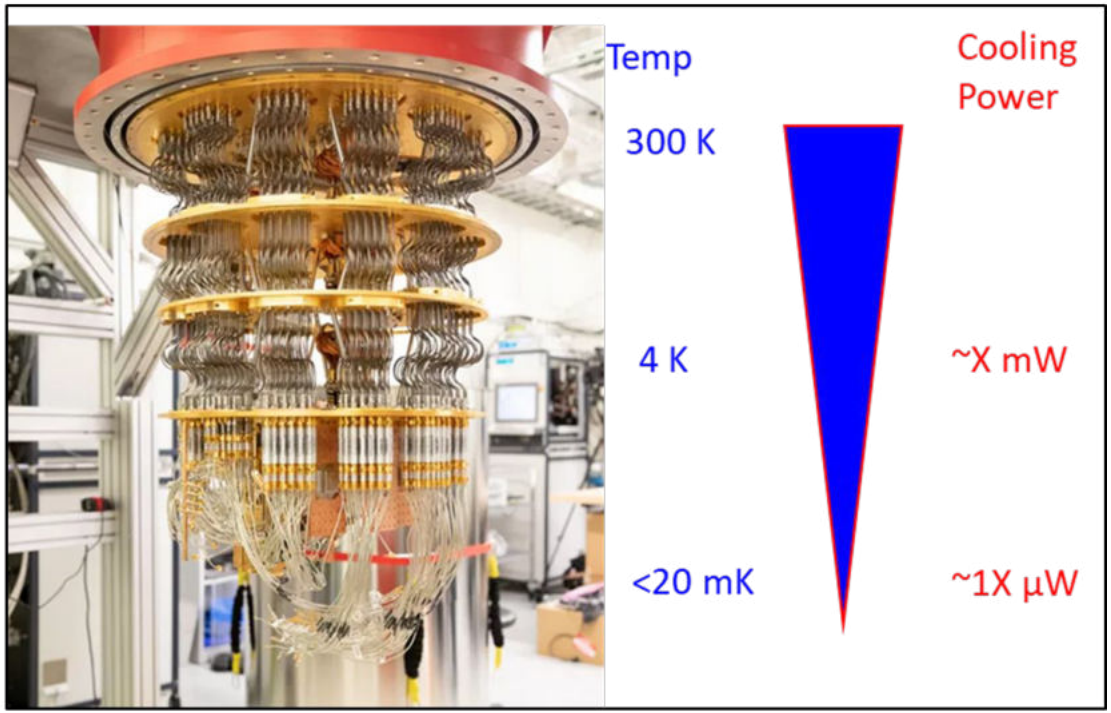


https://phys.org/news/2020-08-google-largest-chemical-simulation-quantum.html ; https://www.cnet.com/news/google-quantum-supremacy-only-first-taste-of-computing-revolution, Amundson, J.; Sexton-Kennedy, E. J. E. W. C., Quantum Computing. 2019

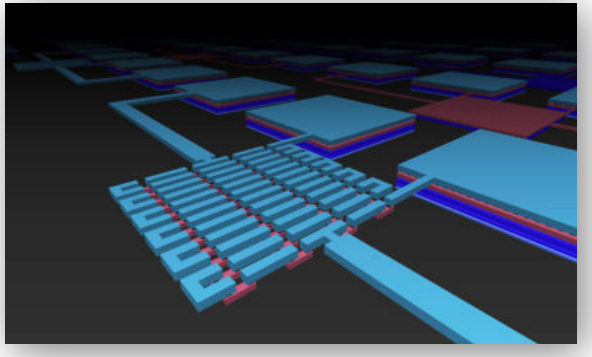
Requirement of Low Operating Power

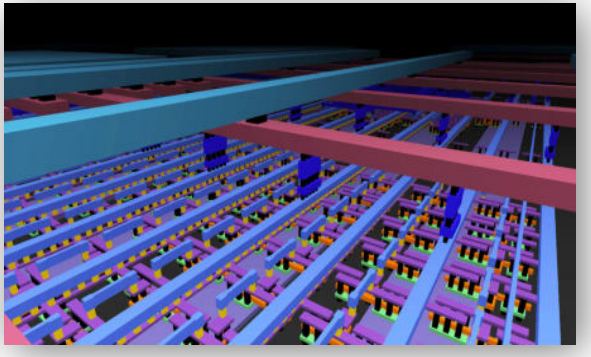


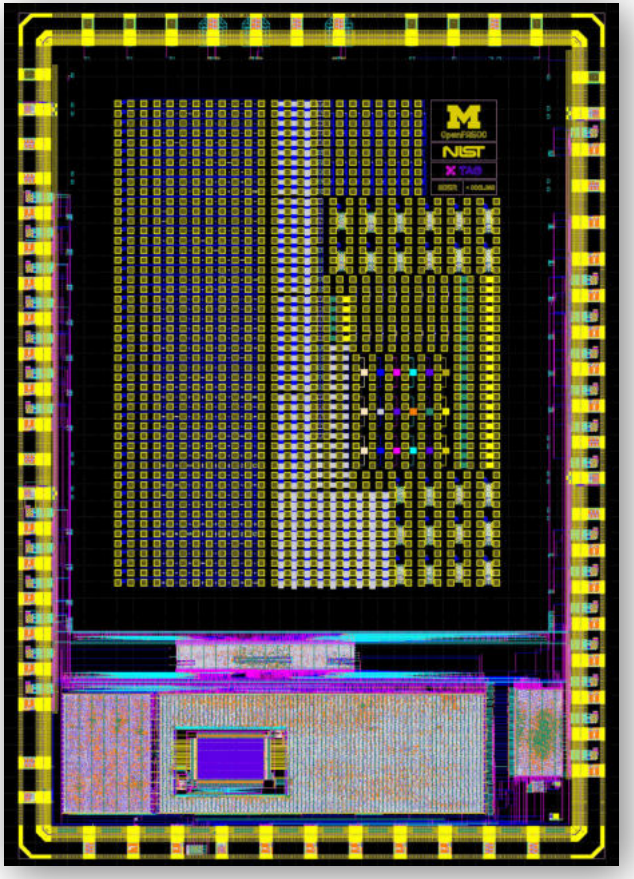
Low power operation



Cryogenic Test Structures with NIST on MPW-5



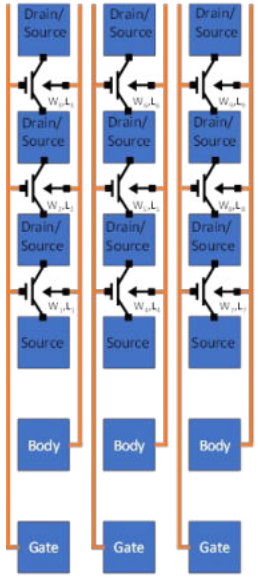


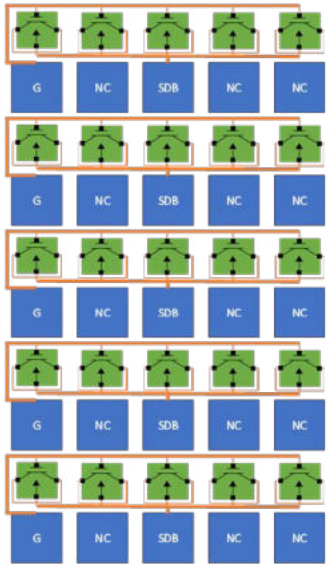


Google + NIST National Institute of Standards and Technology U.S. Department of Commerce

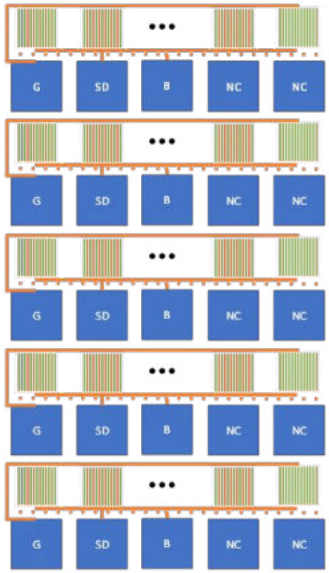
- Partnership with NIST:
  - Re-characterization of SKY130 with wide range temperatures including cryogenic (4K)
  - Automated test structures platform

Cryogenic Test Structures - test interface

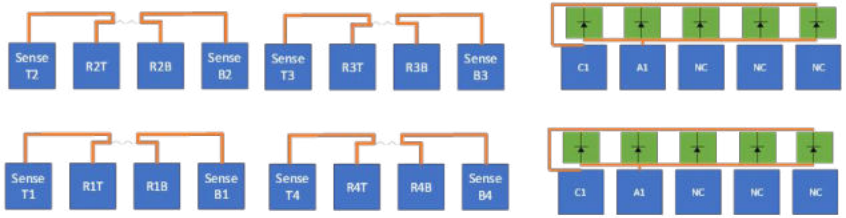




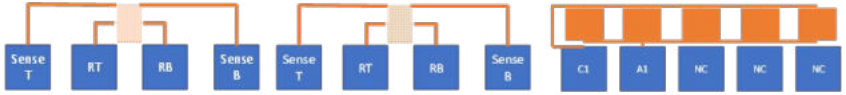
MOSCAP Arrays



Overlap MOSCAP Arrays



Precision Resistors

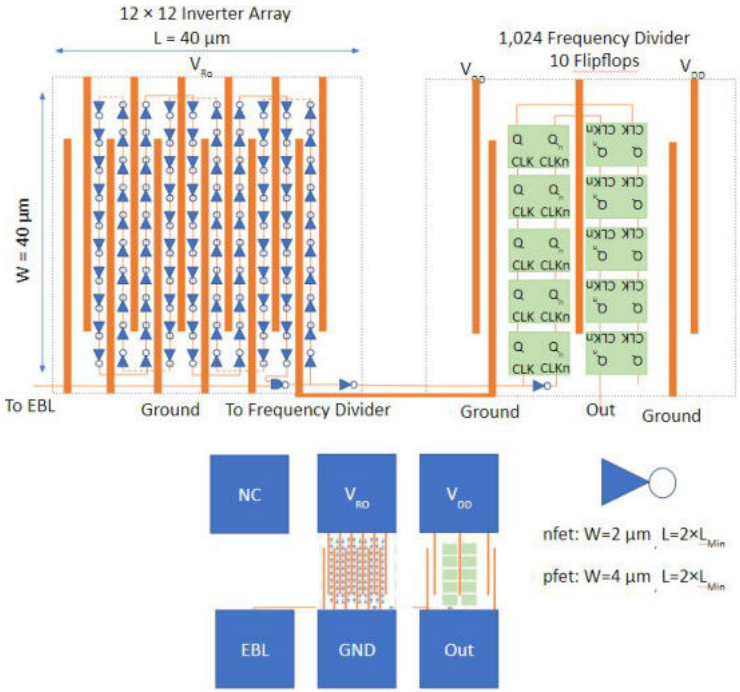


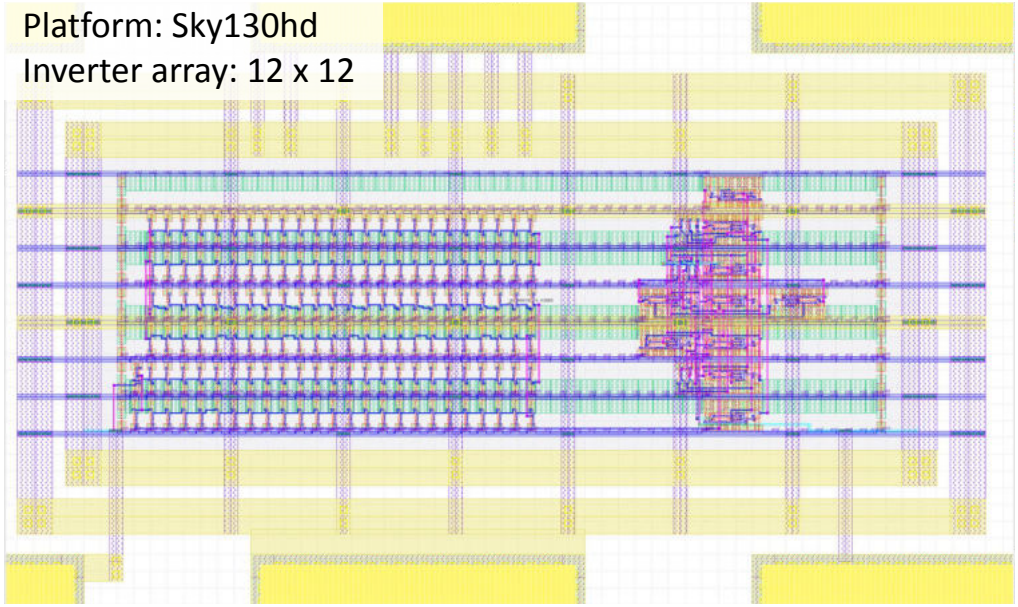
Line Resistance

Via Resistance

To Validation Modules

Interleaved Placement in OpenROAD





- Uses DEF manipulation using Python but could be integrated within OpenROAD

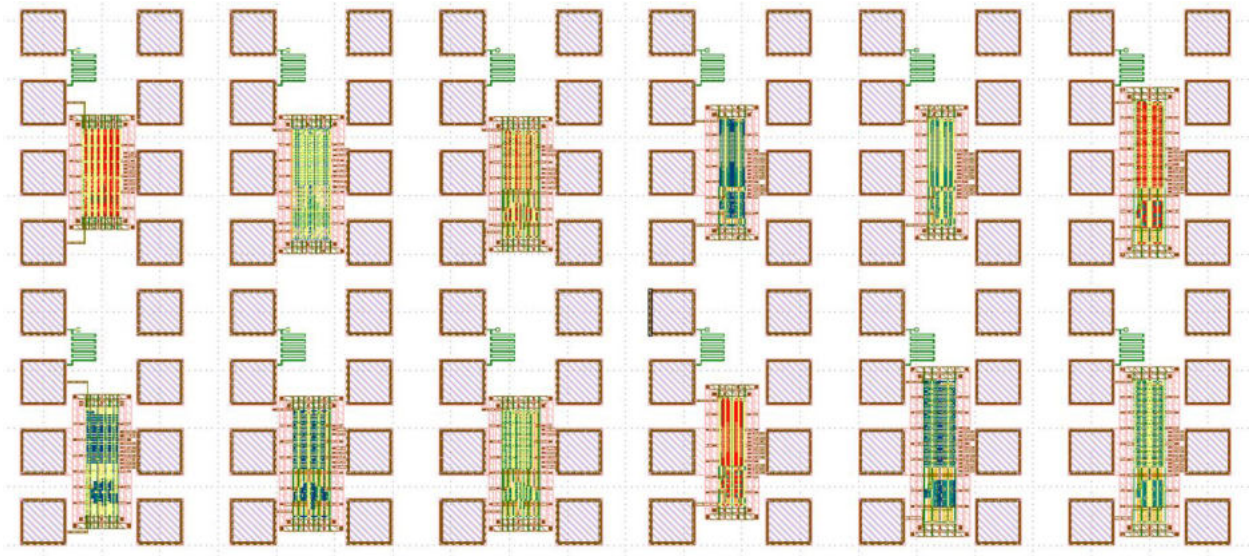
Interleaved Placement in OpenROAD

Implemented 3 Standard Cell Inverter Classes:

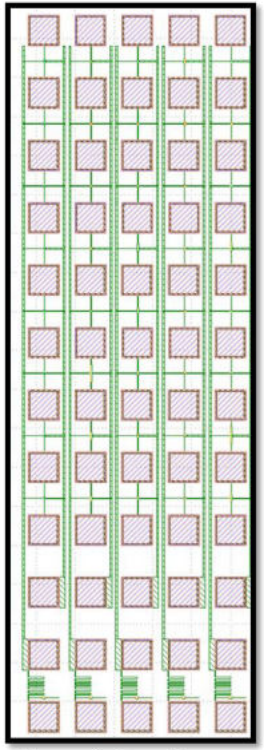
HD, HS, and HVL inverters

9 Additional OSU Standard Cell Inverters

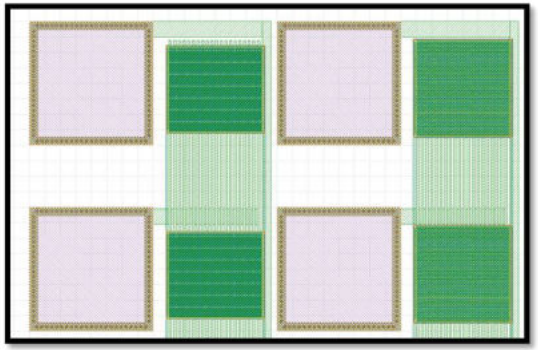
12T_hs, 12T_ls, 12T_ms,15T_hs,15T_ls, 15T_ls, 15T_ms, 18T_hs, 18T_ls, 18T_ms



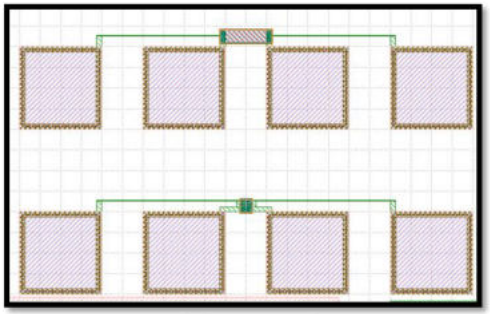
Gdsfactory - automated custom structures



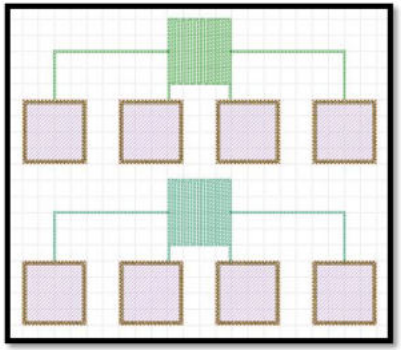
Transistor Arrays



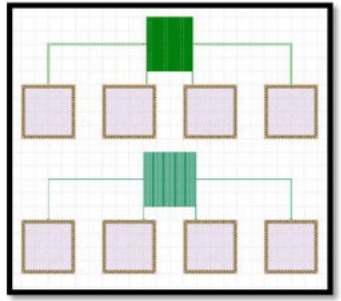
MOSCAP Arrays



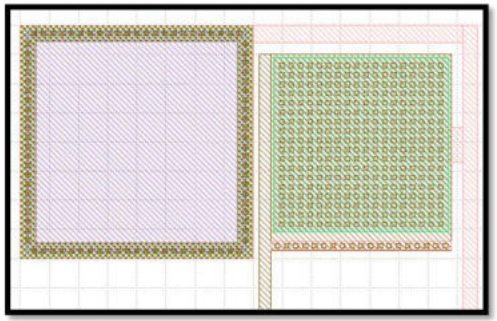
Precision Resistors



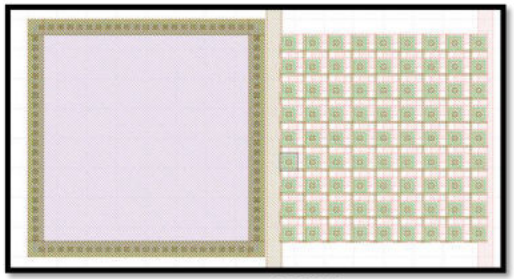
Line Resistance



Via Resistance



Diode Modules



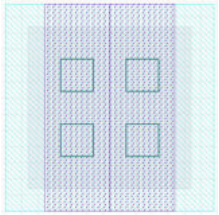
MIM
Capacitor Modules

MIM Cap Generation using Gdsfactory

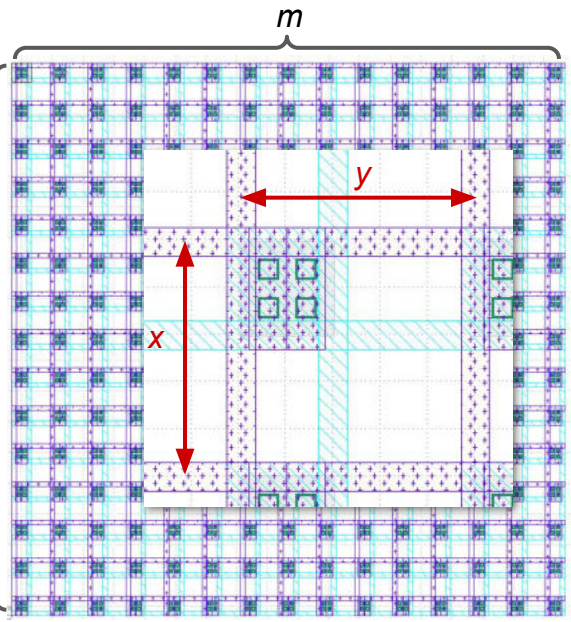
GDSFACTORY Array creation routine

GDSFACTORY Mesh creation routine

Inputs:
Mesh dimension *n,m*
Mesh pitch *x,y*
Mesh layers



gf.path()
gf.add_ref()
gf.move()



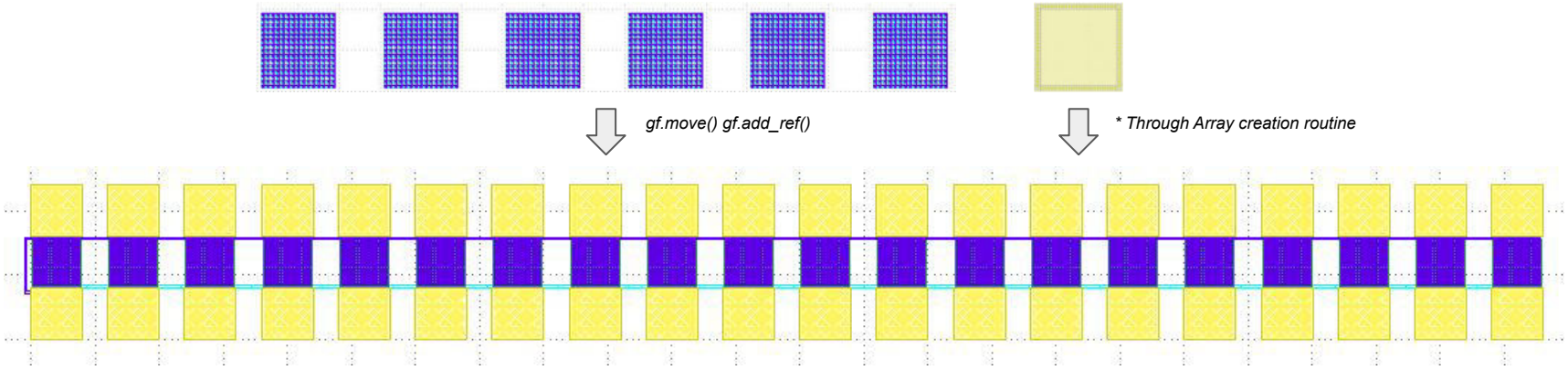
Inputs:
Multiplicity *a,b*
Offsets *x,y*

gf.move()
gf.add_ref()

Example - Array of Flying MiM caps + Custom Padring

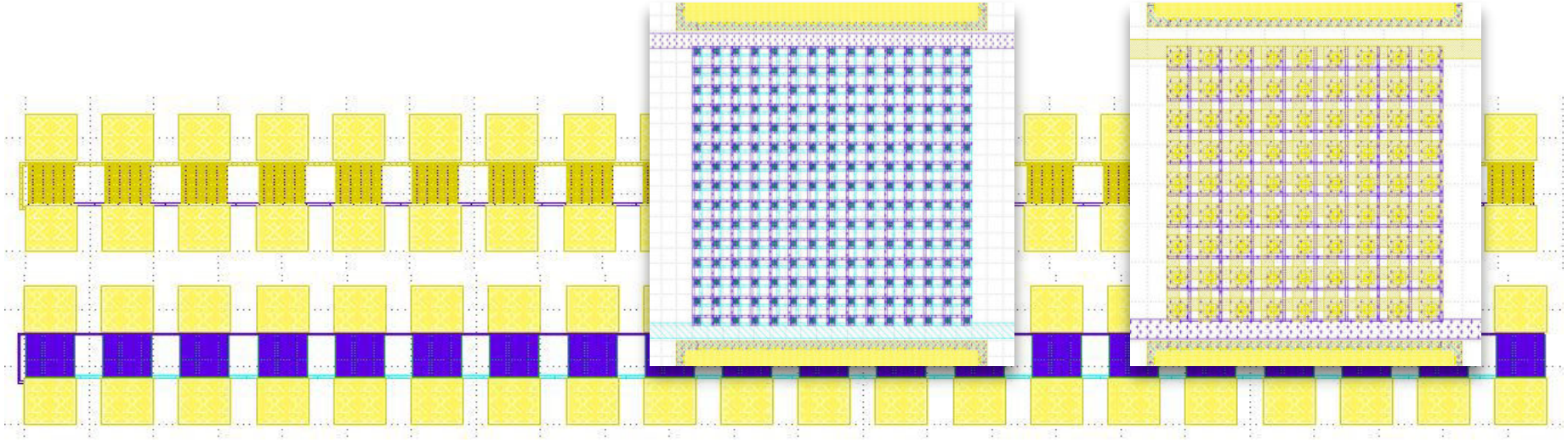
GDSFACTORY Pad-ring place & route routine

Inputs:
Pad ring array spec
Connection definitions (semi-custom)



MIM Cap Generation using Gdsfactory

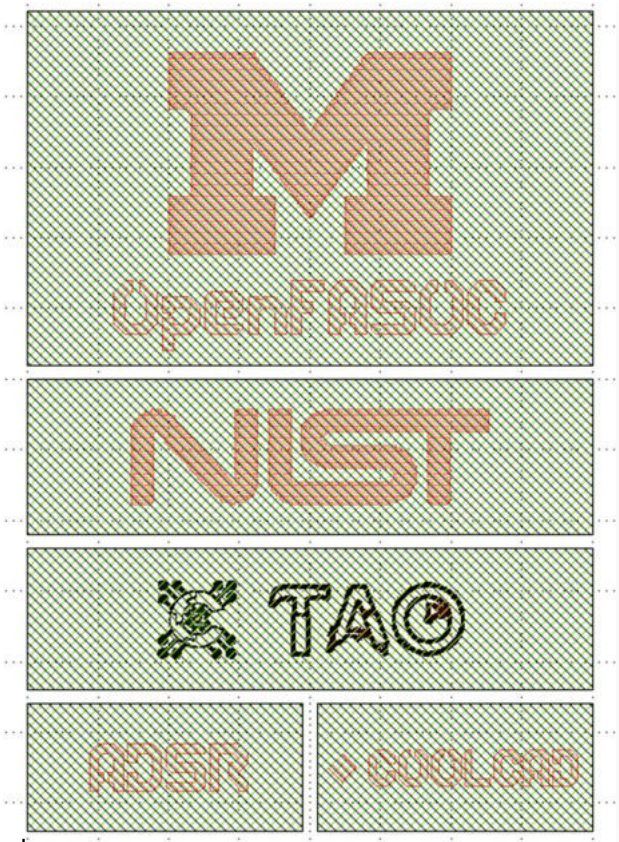
- Computes the grid and places capacitor on grid
- Generates connecting metals (with minimum metal spacing)
- Replicates and connects the structures to pads

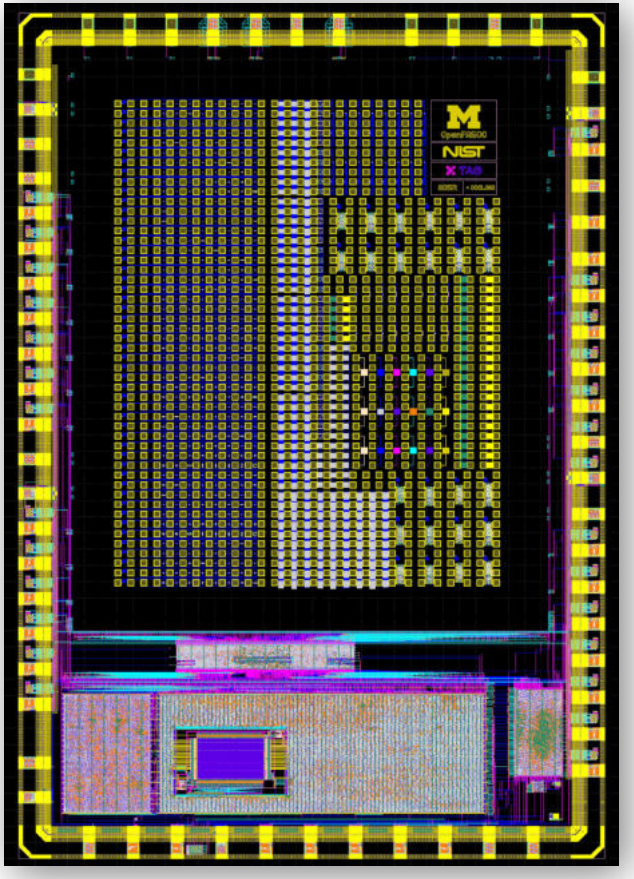


Resultant Test Die

Major Highlights!

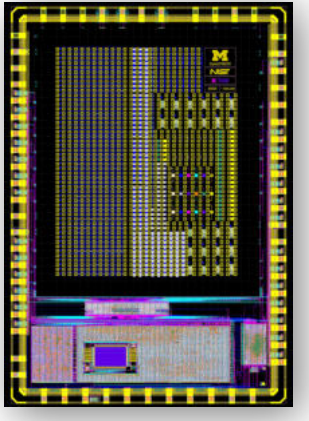
- Over 1400 Pads
- 400+ Transistor Structures
- 30 Capacitor Test Structures
- 24 Ring Oscillators
- 18 line and via chain modules
- 7 Diode Test Structures



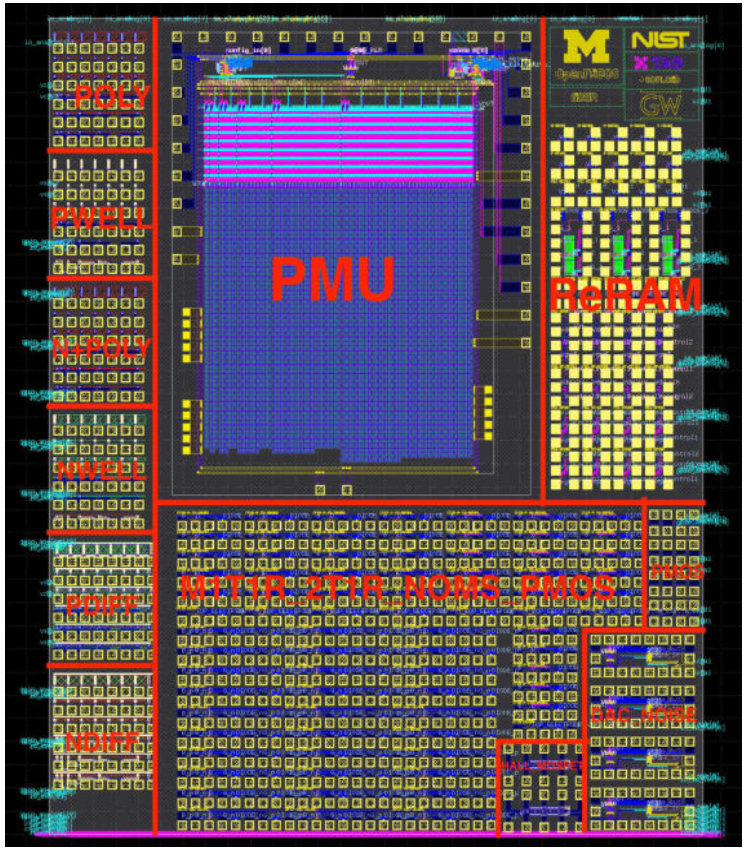


https://github.com/msaligane/openfasoc_cryo_caravel

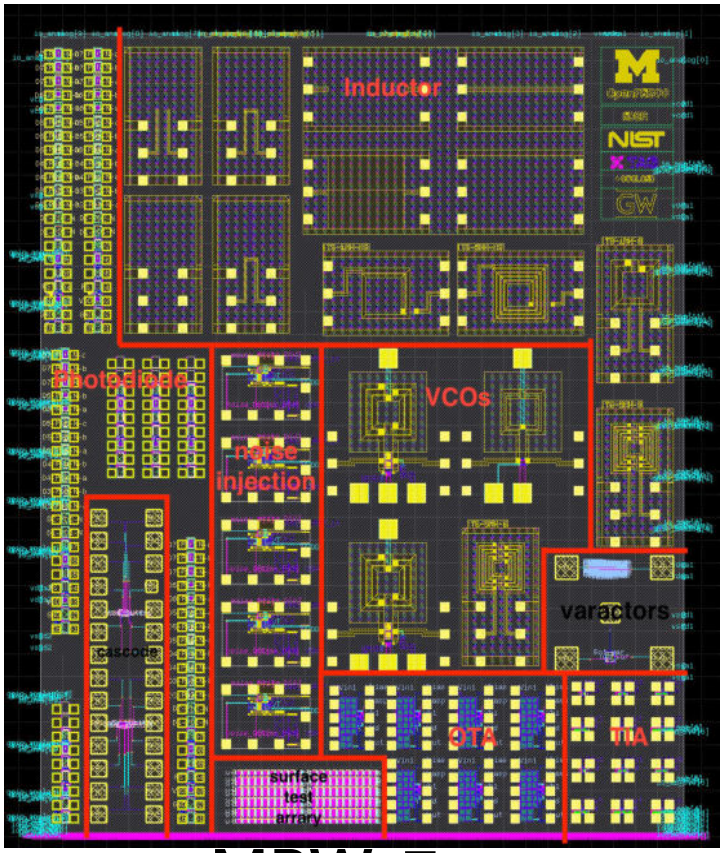
3 Tapeouts Already!



MPW-5



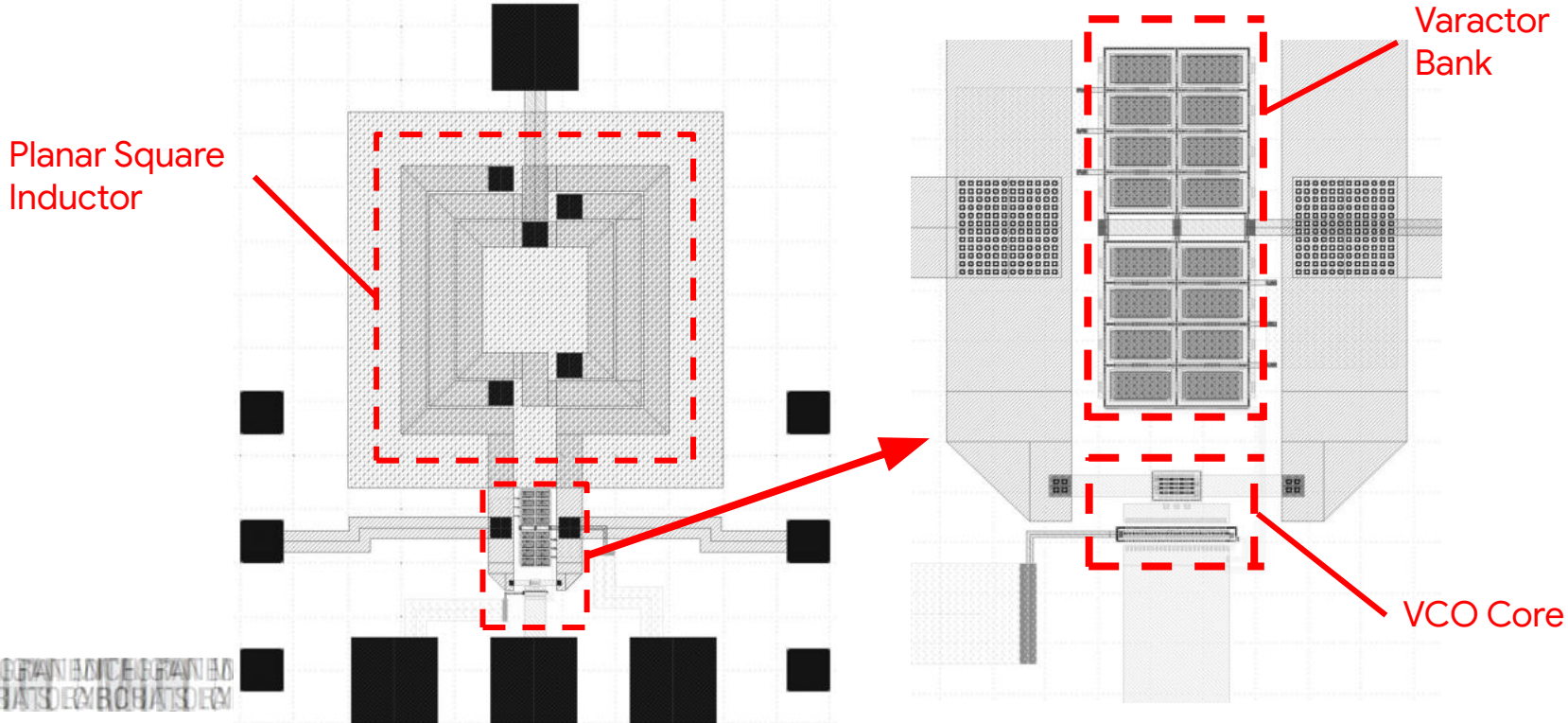
MPW-6



MPW-7

2.4GHz LC-VCO in MPW-7

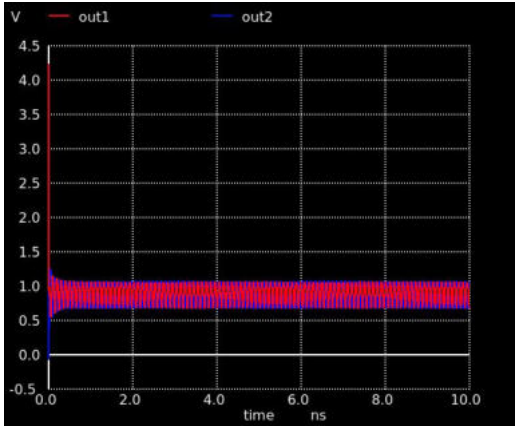
- Automated using OpenFASOC - calls gdsfactory
- A handful of variants designed by a high school student in less than a month
  - https://github.com/ryanrocket/vco-design-notebook/blob/main/VCONotebook.ipynb

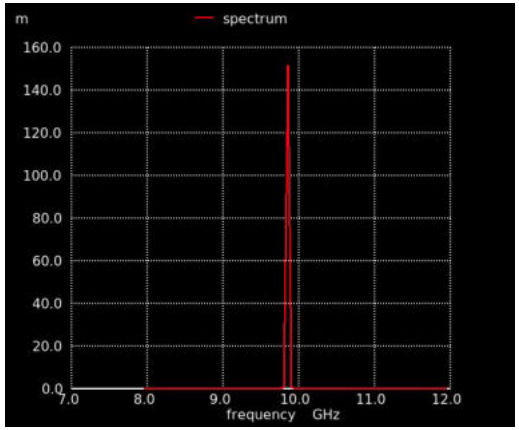


2.4GHz LC-VCO in SKY130 (cont.)

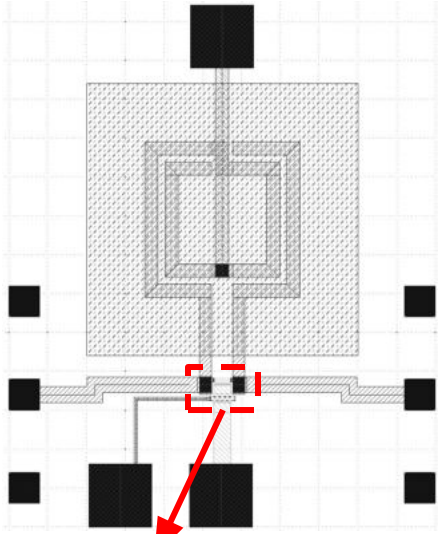
An additional 10GHz oscillator was included that relied solely on parasitic capacitances (no tuning). A resized XCP and current source was needed for this.

Output Voltage

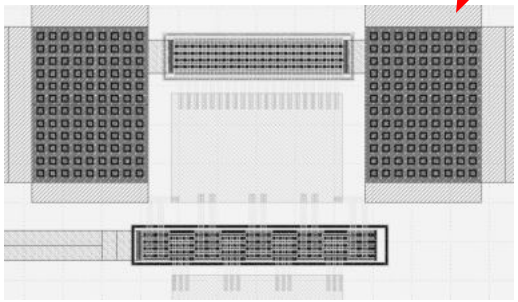




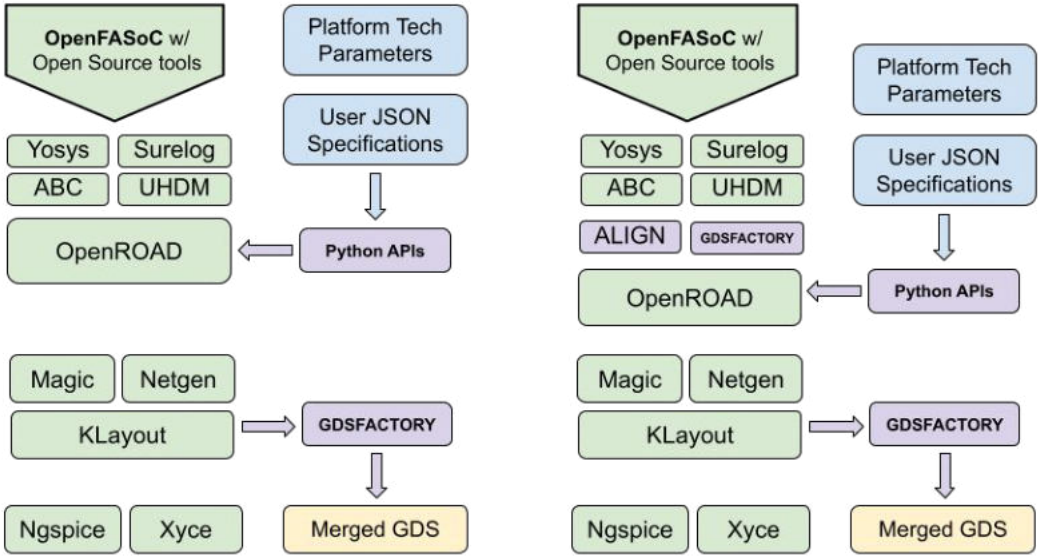
Output Spectrum
(8 - 12 GHz)



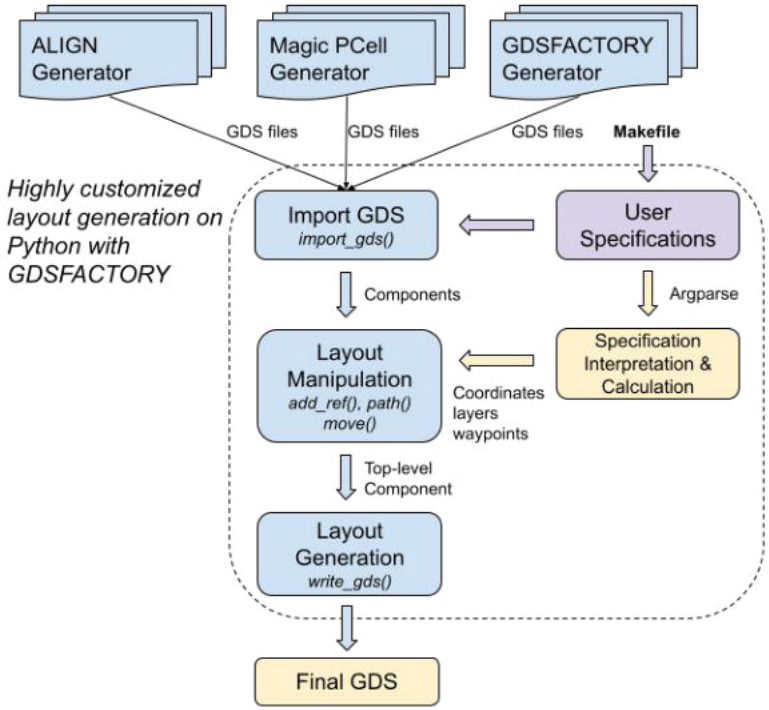
Larger Core



New tools and Python-based APIs

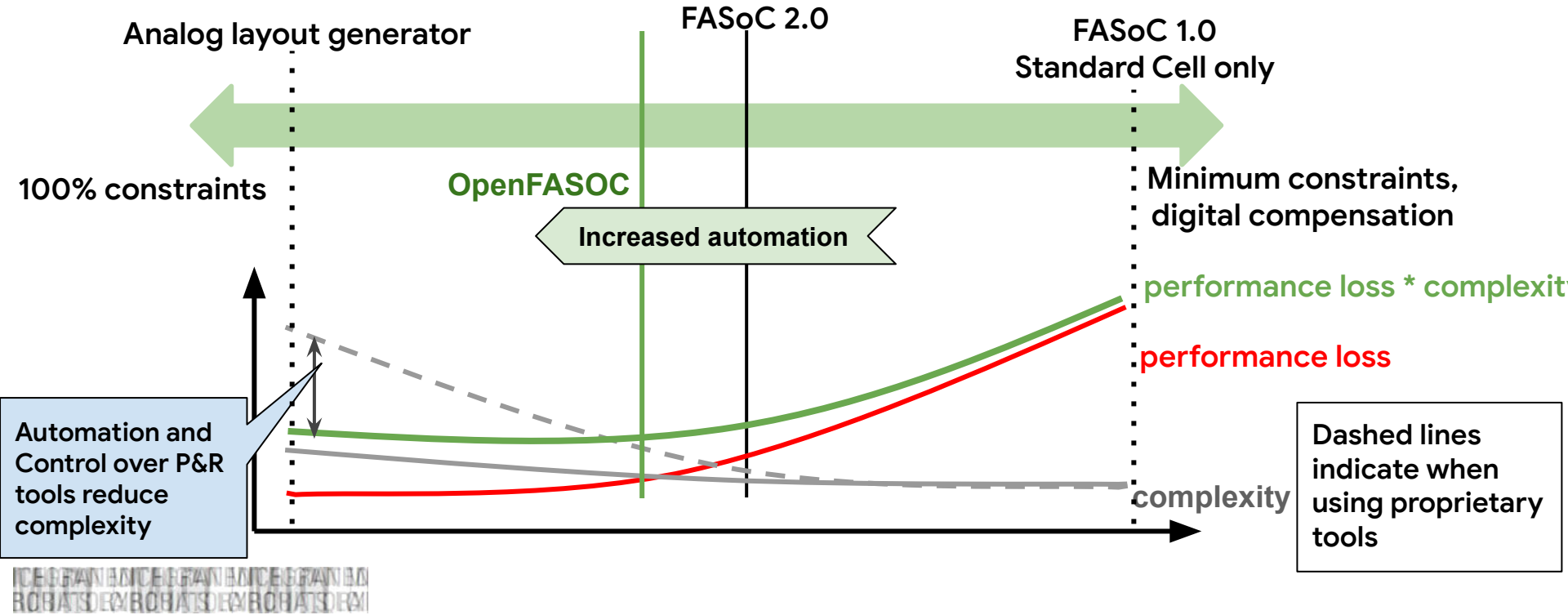


https://github.com/idea-fasoc/OpenFASOC



Performance / Complexity Tradeoff (OpenFASOC)

- FASoC augments digital flow with APR tool placement/routing constraints and minimizes the (performance loss * complexity)



Get involved!

Chipathon

https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-design-contest

Code-a-Chip Notebook Competition ISSCC'23

https://github.com/sscs-ose/sscs-ose-code-a-chip.github.io

Deadline: Nov. 21st

Key Event in 2020: First Open-Source PDK

Google Partners with SkyWater and Efabless to Enable Open Source Manufacturing of Custom ASICs

First open source foundry PDK enables full manufacturing chain for open hardware;

Google-sponsored MPW shuttle program now accepting design submissions

BLOOMINGTON, Minn. and SAN JOSE, Calif. – November 12, 2020 – SkyWater Technology, the trusted technology realization partner, and Efabless, a crowdsourcing design platform for custom silicon, today announced design submissions are now being accepted for a series of Google-sponsored open source Multi-Project Wafer (MPW) shuttles that will run at SkyWater. Through a partnership between Google, SkyWater and Efabless, open source designs selected by the program will be fabricated at no cost to the designers. The MPW program is enabled by the first foundry-supported open source process design kit (PDK) for 130 nm mixed-signal CMOS technologies (SKY130 process). The initiative will enable a complete open source manufacturing supply chain for custom application specific integrated circuits (ASICs) and has been discussed in a series of talks produced by the FOSSi (Free and Open Source Silicon) Foundation including presentations by Google and Efabless.

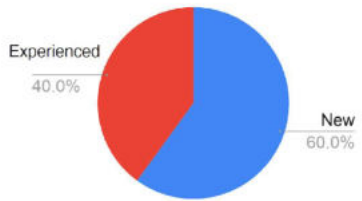
Google-Sponsored Free Shuttle Runs

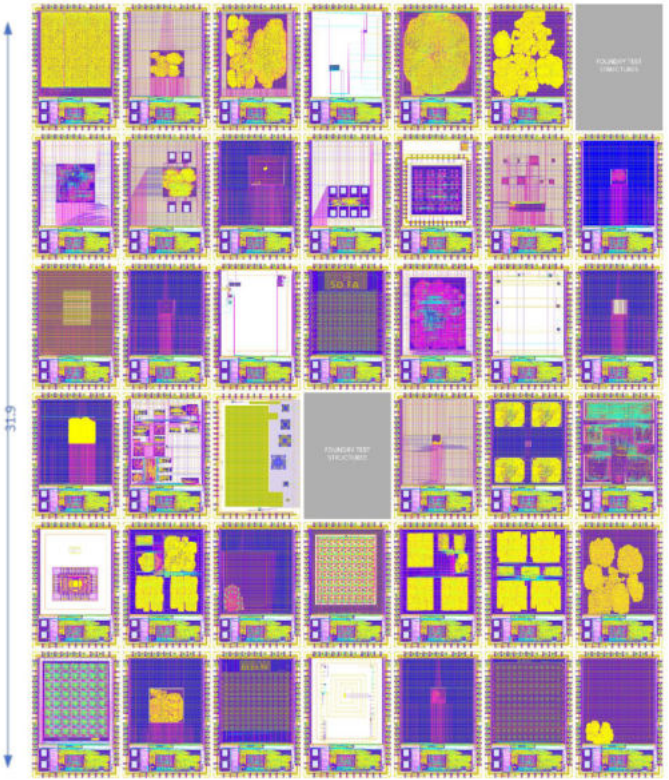
GOOGLE's MPW-ONE

First MPW Overbooked 45/40

45 designs submitted in 30 days!

60% by first time designers!





Source: efabless

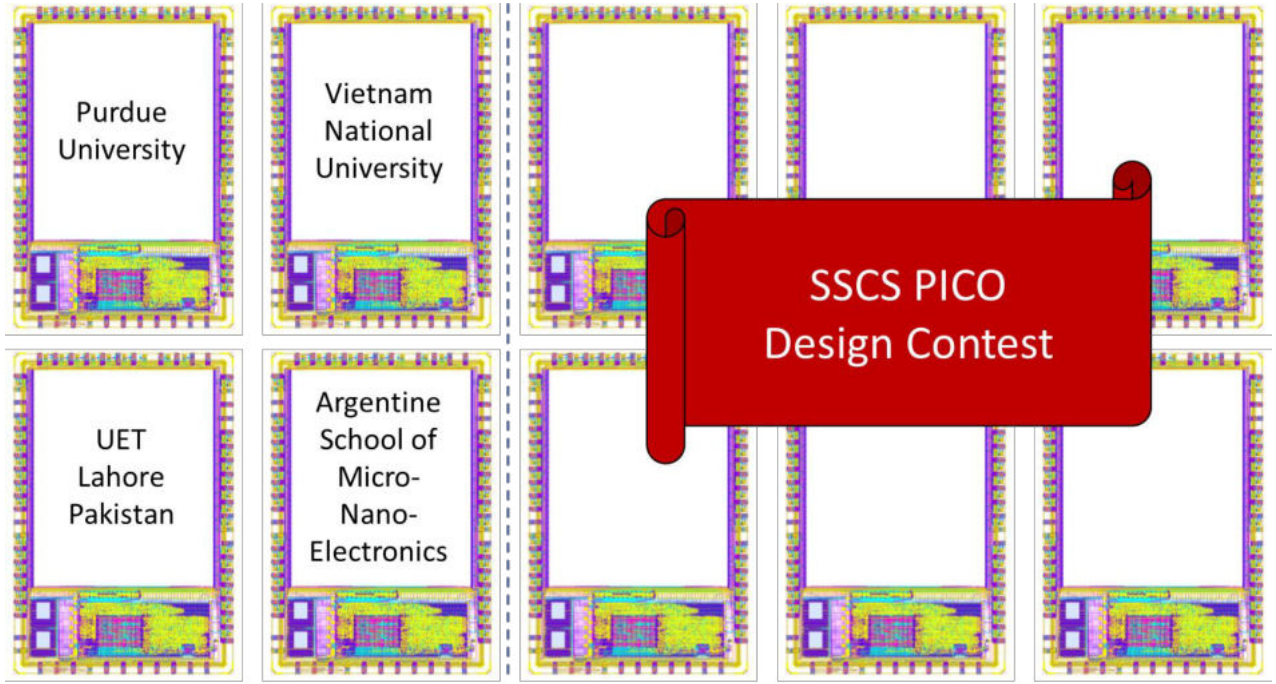
Democratizing IC Design: The SSCS PICO Program

The Solid-State Circuits Society is committed to improving diversity, inclusion, and accessibility in integrated circuit (IC) design. We envision a future in which chips can be designed through a web browser, by anyone, anywhere, and through open worldwide collaboration.

Through its Platform for IC Design Outreach (PICO) program, the SSCS is working with the rapidly growing open-source community to help accelerate the construction of the required ecosystem. Our goal is to help build and connect to new communities that share our excitement about IC innovation and its democratization toward a new wave of global impact.

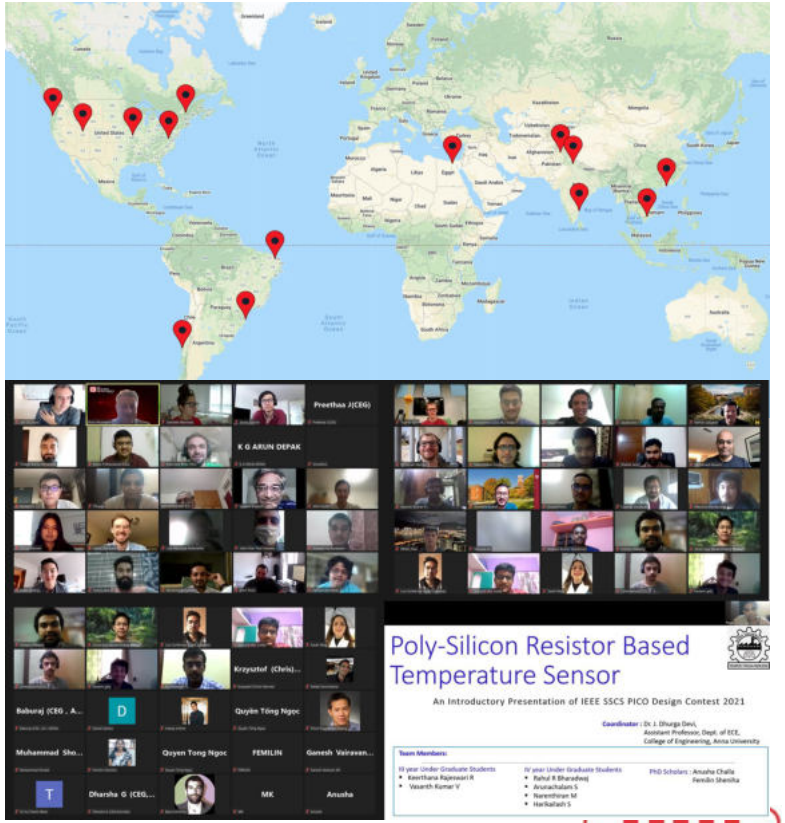
https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program

SSCS Sponsored Fab Runs in 2021



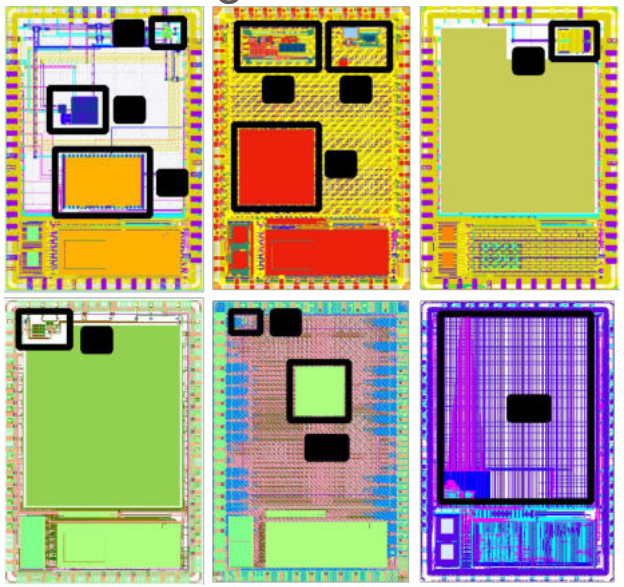
2021 IEEE SSCS “PICO” Design Contest

- 61 design proposals
  18 selected
  11 taped out
- Free IEEE & SSCS student memberships offered to all participants
- Pakistan team starting a new SSCS Student Branch Chapter



Designs Completed & Taped Out

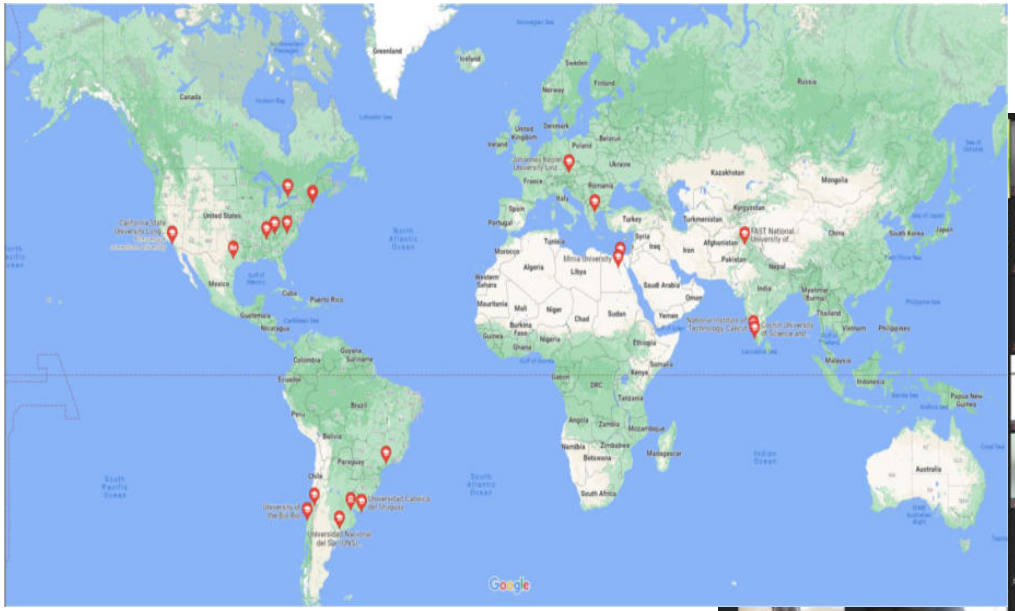
- Tape-out via Efabless chipIgnite (130nm SkyWater)
- All designs shared on GitHub

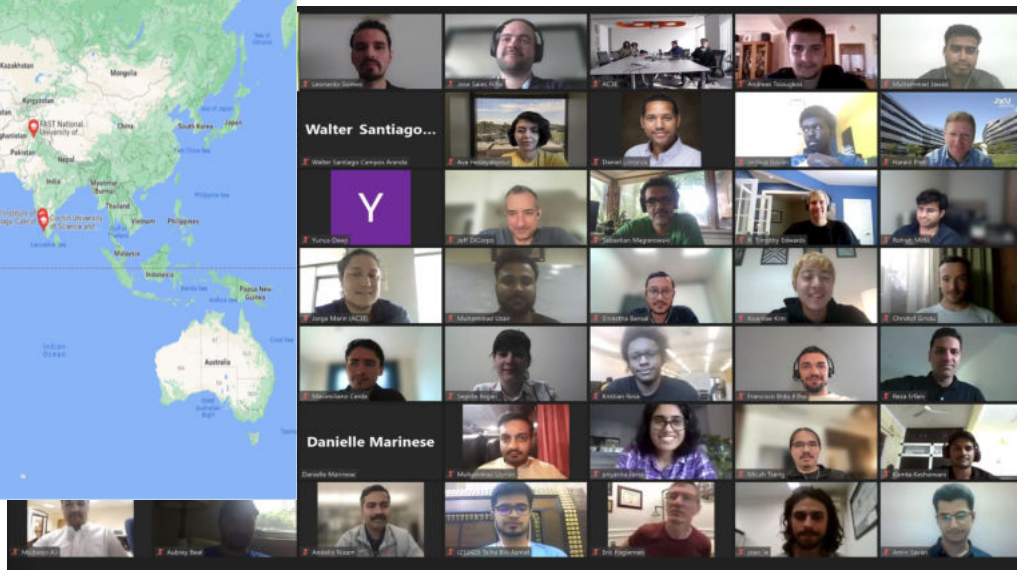


	Function	Team	Chip URL
1	5G bidirectional amplifier	Pakistan3 (FAST National University)	https://efabless.com/projects/560
2	Wireless power transfer unit	Pakistan2 (FAST National University)	
3	Variable precision fused multiply-add unit	Pakistan1 (FAST National University)	
4	Oscillator-based LVDT readout	India2 (Anna University)	https://efabless.com/projects/474
5	Temperature sensor	India1 (Anna University)	
6	GPS baseband engine	India3 (Anna University)	
7	Ultra-low-power analog front-end for bio signals	Brazil2 (U. Federal de Santa Catarina)	https://efabless.com/projects/476
8	TIA for quantum photonics interface	USA4 (University of Virginia)	https://efabless.com/projects/470
9	Bandgap reference	Egypt (Cairo University)	https://efabless.com/projects/473
10	Neural network for sleep apnea detection	USA2 (University of Missouri)	
11	SONAR processing unit	Chile (University of the Bio-Bio)	https://efabless.com/projects/540

B. Murmann, "SSCS PICO Contestants Cross the Finish Line," https://ieeexplore.ieee.org/document/9694491

2022 Chipathon – Selected Teams





22 teams selected, see:
https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program

SSCS TC “Open-Source Ecosystem”

Boris Murmann
Stanford
USA

Thomas Brandtner
Infineon
Austria

Francisco Brito Filho
Fed. Univ. Semiarido
Brazil

J. Dhurga Devi
Anna Univ.
India

Jaeduk Han
Hanyang Univ.
Korea

Chiraag Juvekar
Apple
USA

Rana Muhammad
FAST National Univ.
Pakistan

Harald Pretl
Kepler Univ., Linz
Austria

Priyanka Raina
Stanford
USA

Mehdi Saligane
Univ. Michigan
USA

Mirjana Videnovic-Misic
Silicon Austria Labs
Austria

The end!

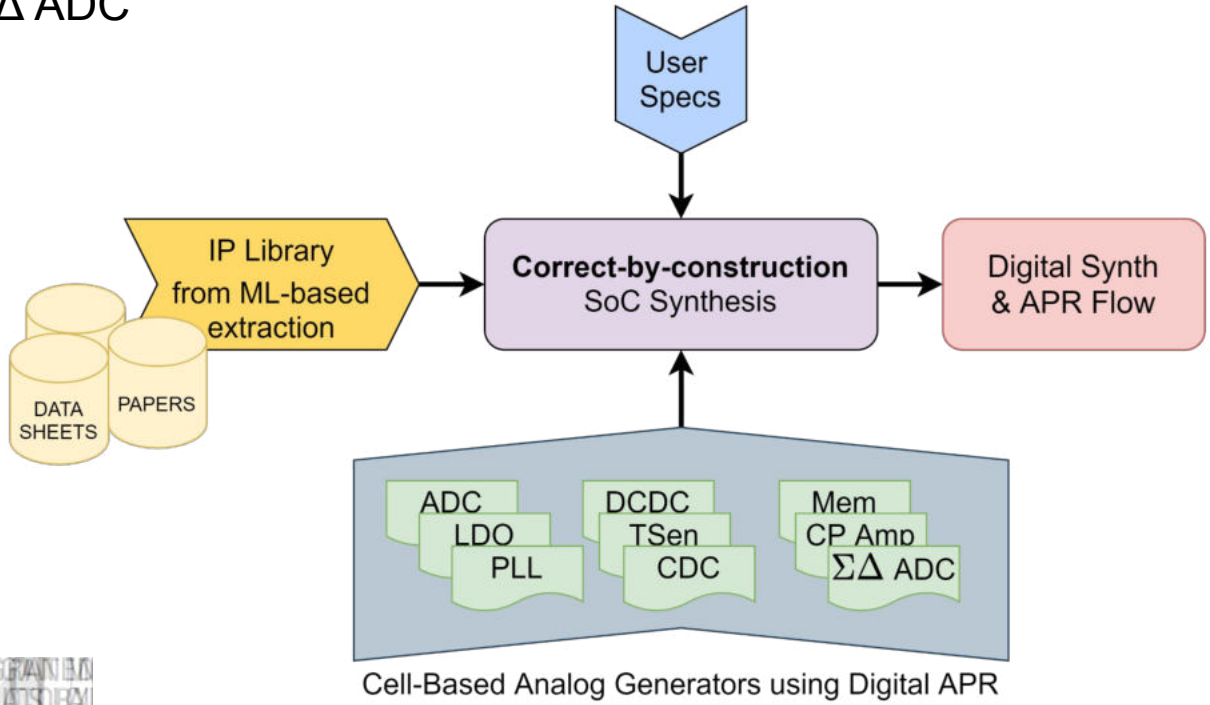
Bonus slides

Questions

1. How do I help the OpenFASOC project move forward?
   a. Joining or introduce your work in our Weekly call
   b. Send Pull Requests on Github
   c. Read our New Contributors guidelines on: https://openfasoc.readthedocs.io/en/latest/developers-guide.html
   d. All the above
2. Why do you think open-source analog automation would succeed?
   a. Access to more flexible and up-to-date open-source software development tools
   b. Open collaboration and exchange of expertise
   c. Open PDK and shuttles and shuttles allow to lower barrier to chip design and reduces the risk of failure
   d. All the Above

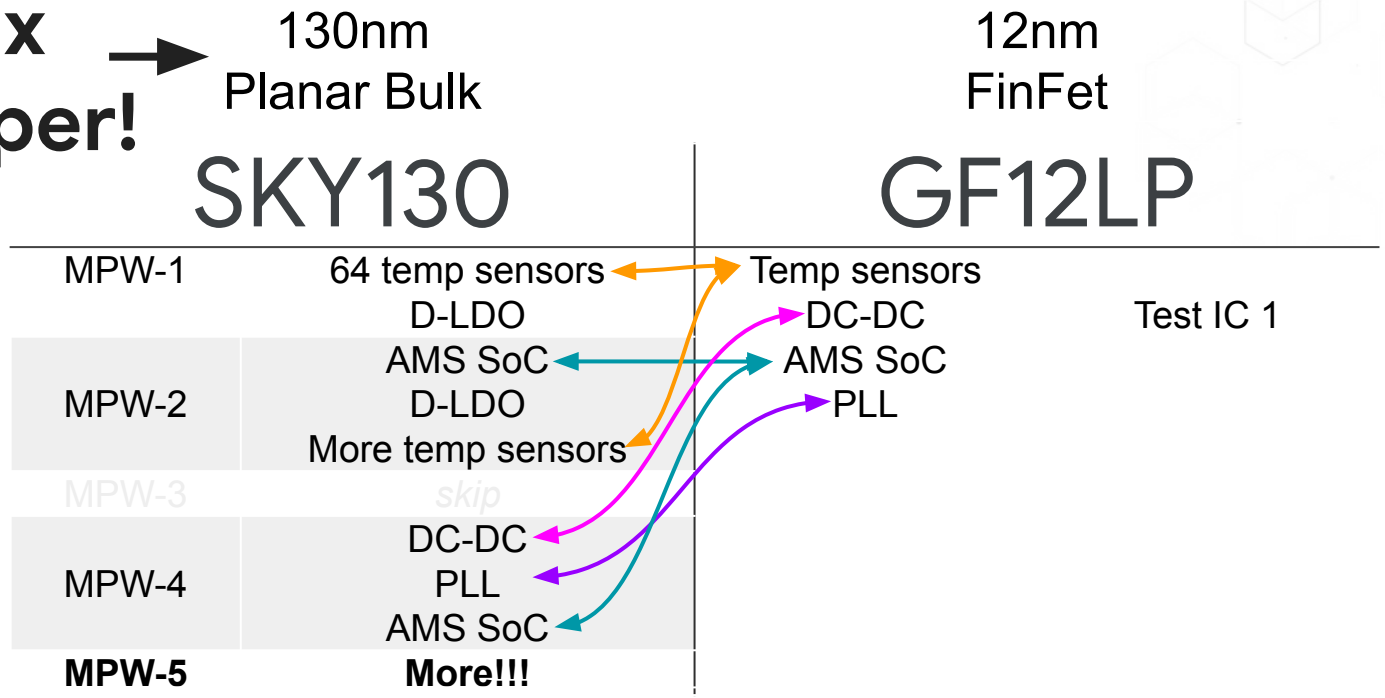
FASoC: Fully-Autonomous SoC Synthesis

- Correct-by-construction SoC design leveraging IP-XACT and Arm Socrates
- Analog generation tools for xDC, PLL, SRAM, DCDC, temp sense, CP Amp, ΣΔ ADC



OpenFASoC - *Portable* **Transferrable** Analog

>10x cheaper! →



Same **fully** open source tools
Same scripting generators

UNIVERSITY OF MICHIGAN

OpenFASoC - *Portable* Analog

- Analog generators - Power DCDC + LDO, Temperature Sensors, PLLs, ADCs.
- Example mixed signal SoC integration.
- Silicon proven with increasingly more tape outs, increasingly faster!

- Fully open source flow using fully open source tooling (OpenROAD, Xyce).
- Demonstrating **acceleration** of velocity and productivity.

SKY130 ⟷ GF12LP

130nm
Planar Bulk

12nm
FinFet

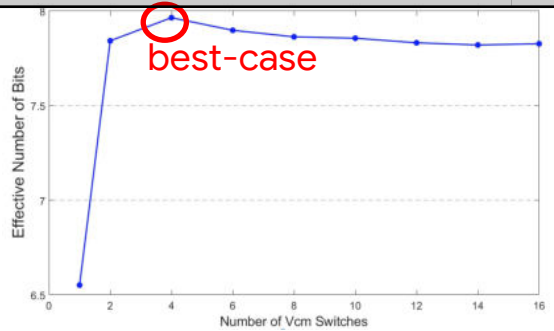
>10x ↗ cheaper!

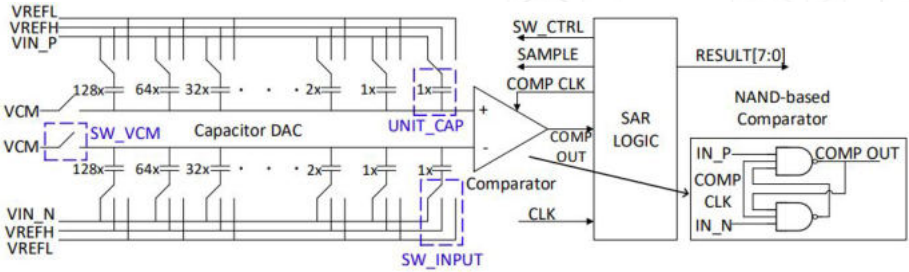
Same **fully** open source tools
Same scripting generators

SAR ADC Common Centroid Placement

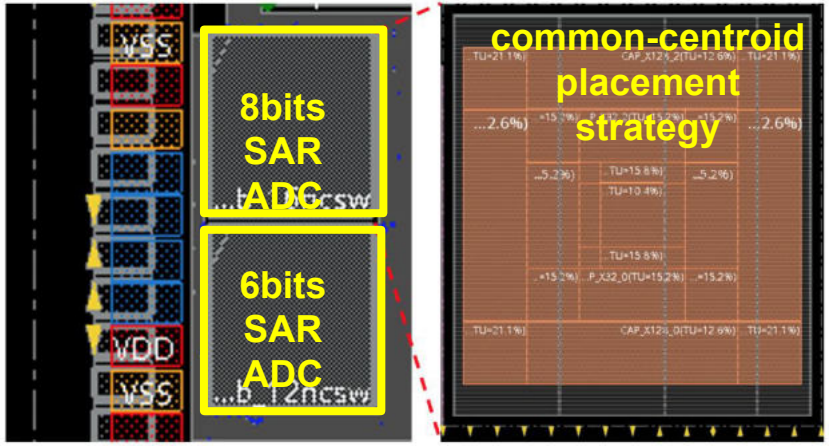
- Symmetrical Placement of unit caps and switches

Output Spec.	CDL	PEX
$F_{SAMPLING}$ (MHz)	1	
Unit Cap Value (fF)	2.6	
Area (mm^2)	-	0.04
Power (μW)	6.72	11.2
Effective Number of Bits	7.86	7.75





SAR ADC Block Diagram



Open Source RoT