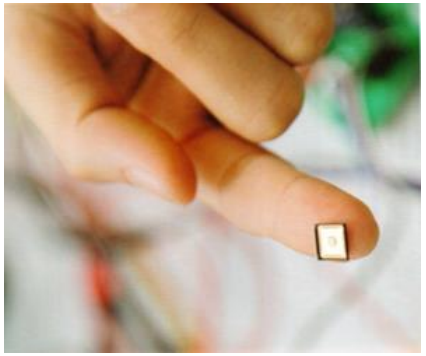
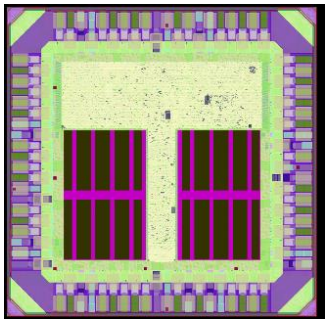
VIETNAM NATIONAL UNIVERSITY HANOI (VNU)
VNU UNIVERSITY OF ENGINEERING AND TECHNOLOGY

SISLAB
http://sis.uet.vnu.edu.vn

Research and Development Activities on RISC-V and its Applications for IoTs

Duy-Hieu Bui & Xuan-Tu Tran
VNU Key Laboratory for Smart Integrated Systems (SISLAB)

Outline

- Introduction to SISLAB
- RISC-V ecosystem for IoT applications
- Our works & demonstration
- Our research & training directions
- Conclusion

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Introduction to SISLAB

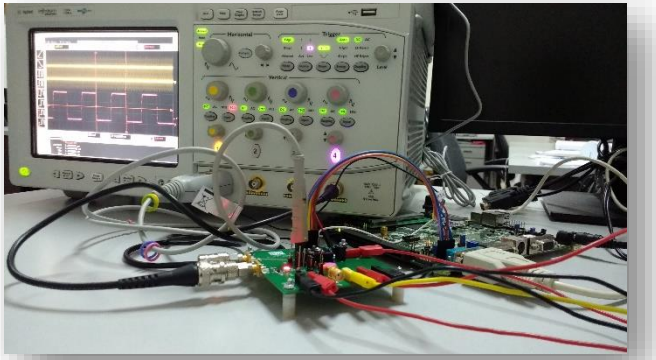
Research interests

- ✓ System-on-Chip/Network-on-Chip
- ✓ Low-power techniques
- ✓ IoT and AI accelerator
- ✓ Fault-tolerance & Design-for-Test
- ✓ LSI design

Established in 2016 by the President of VNU

Opening ceremony: 22 December 2016

Offices: 2.1 Building E4, UET campus & 203 Building HBI, Hoa Lac



Chip testing at SISLAB, VNU-UET

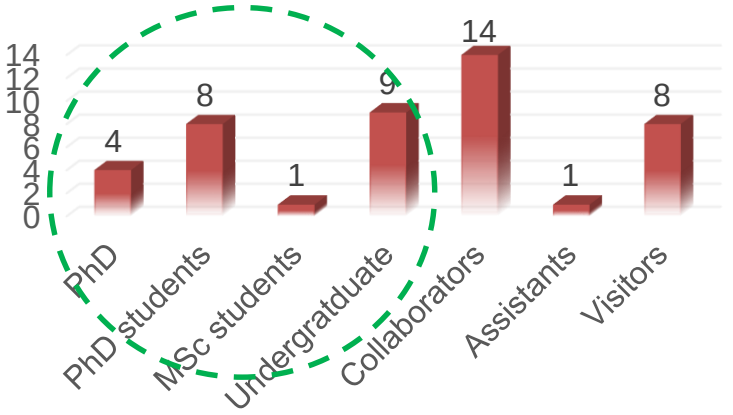
Demonstration at Hoa Lac high-tech park

Introduction to SISLAB

- Total: 23 members

(as June 2019)

Hoa Lac campus



Hanoi campus

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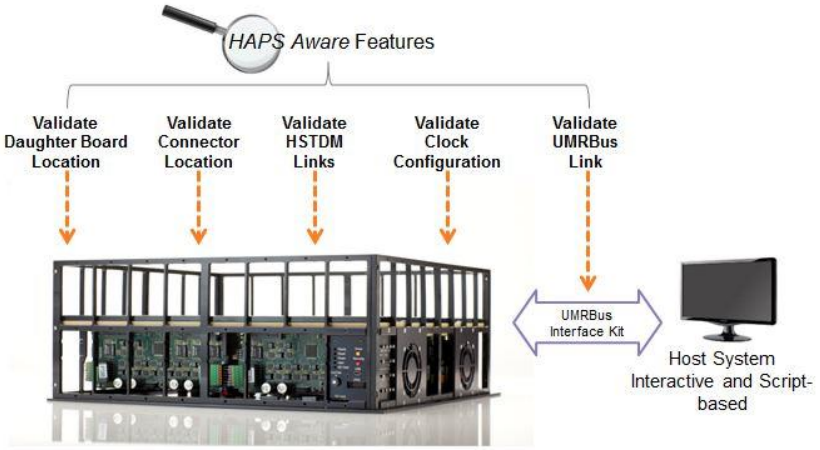
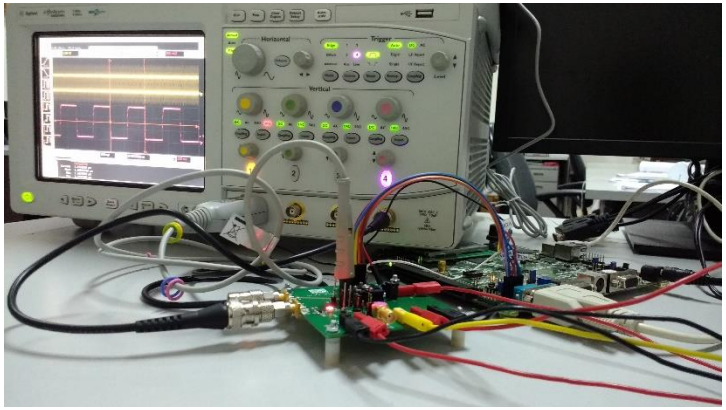
Facilities/Equipment

- Computer Aided Design tools
  - **Synopsys EDA Tools *(until 2022)***
    - Front-end & back-end tool sets for digital design
    - Analog & mix-signal design
  - Xilinx:
    - Vivado tool suite



- **Prototyping/Testing Equipment**
  - **Synopsys HAPS-70**
  - Xilinx FPGA development kits (Virtex-7)
  - Artix-7
  - UltraSoC ZCU 106



These tools & hardware are open for students, universities, start-ups and companies

Collaborations *(active)*

- CEA-LETI, Minatec (France)
- University Paris-Sud XI (France)
- Grenoble INP (France)
- The University of Aizu (Japan)
- University of Electro-Communications (Japan)
- University California, Davis (USA)
- **Toshiba (Japan);** DxCorr (USA)
- CMP & ams AG; Global Foundry & LYNxemi
- Synopsys; Mentor Graphics
- Vietnamese universities/institutions

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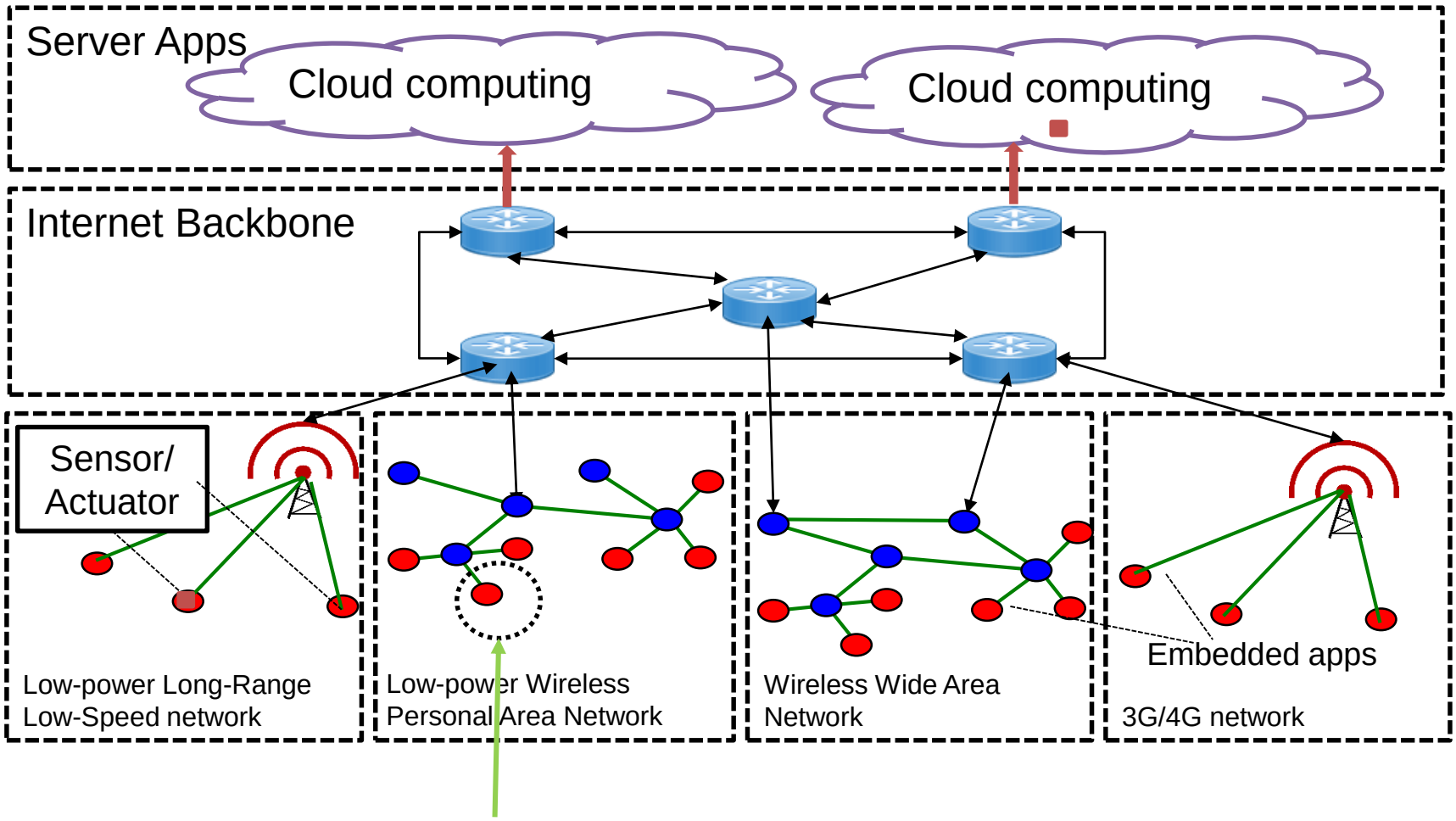
IoT's organization

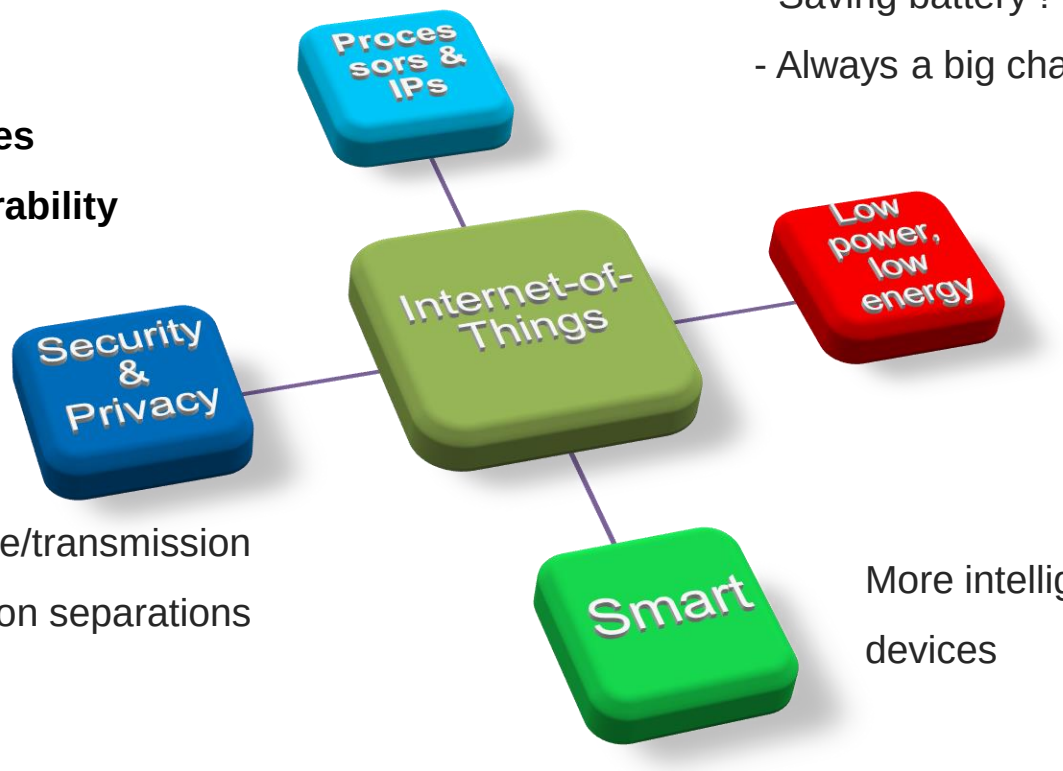


Ultra-low-power, ultra-low-cost constrained devices or edge devices

Key research issues related to IoT

Different IoT workloads

- **Sensor nodes**
- **Edge/gateway devices**
- **On-demand/configurability**



- Saving battery !
- Always a big challenge in LSI design

Sensitive data in storage/transmission

Application separations

More intelligent & smarter edge devices

RISC-V & Opensource ecosystem

- Ready to use SoC platforms

Pulp-platform

  - RISC-V processors: Rocket chip, Arian
  - Simulator: Validator, Firesim (FPGA)
  - Configurable IPs: SHA-3, testchip IPs
  - Interconnect: AXI4, Tilelink

- Libraries
  - BSG BaseJump STL: clk_gen, async_fifo, synchronizers, Front-Side Bus, Network-on-chip IPs, etc.
  - Chips Alliance
- Security

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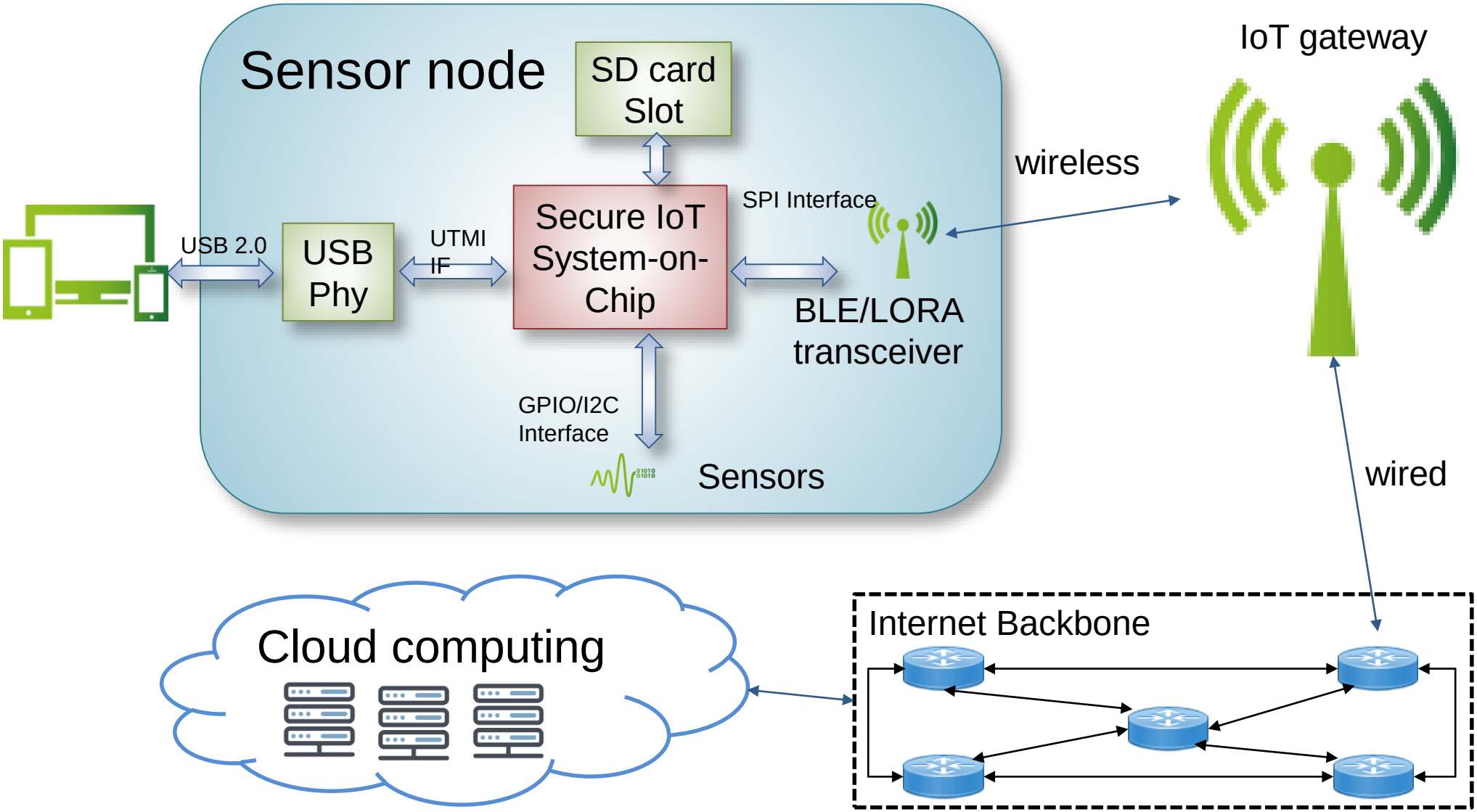
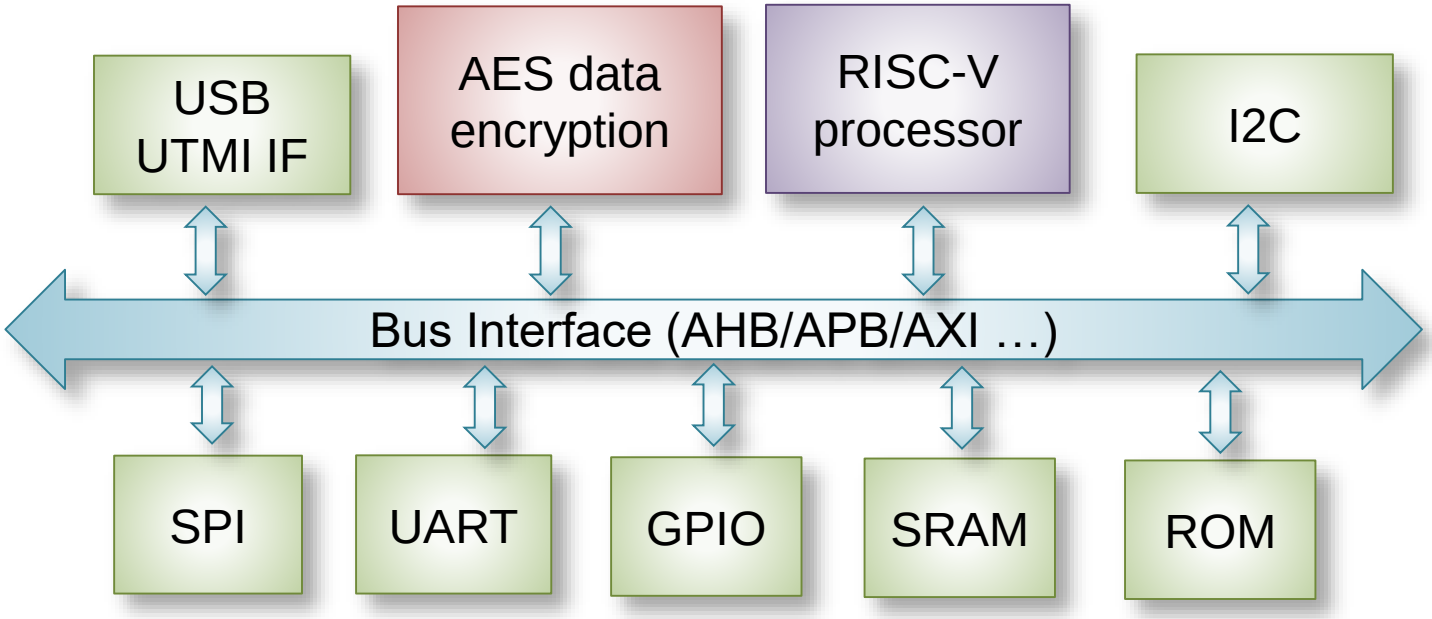
ADEN4IOT: Low power sensor nodes



Integrated IoT systems with security features



- AES Encryption with AEAD modes
- Low power RISC-V core for configuration, control and data acquisition
- Communication interface: SPI, UART, I2C, GPIO

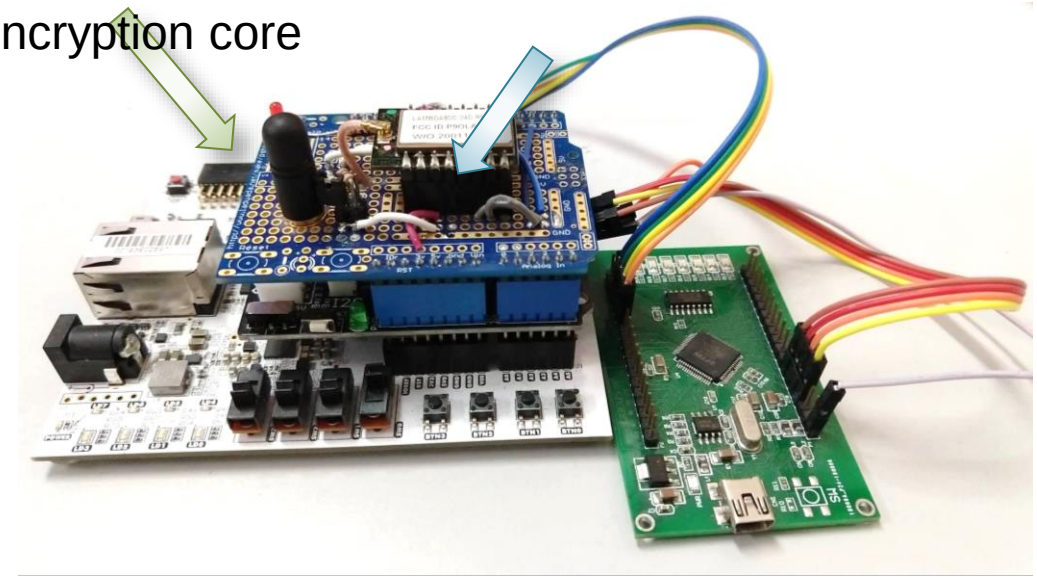
⇒ System-on-chip based on RISC-V for Ultra-Low-Power consumption

ADEN4IOT prototype

- Processor: RISCY (Pulp-platform)
- Default clock: 25MHz
- SISLAB IPs through AXI4 bus

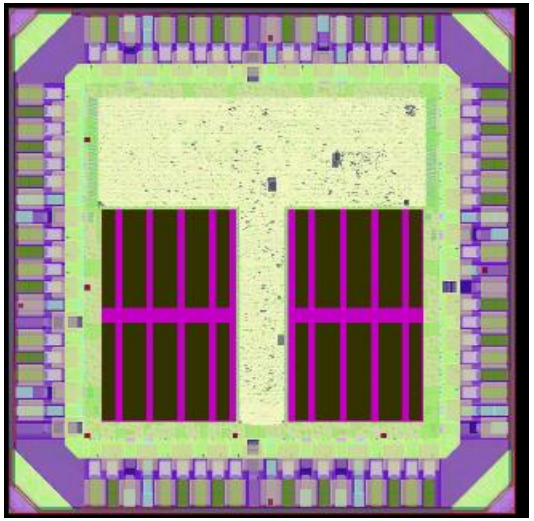
RISCY & our encryption core

BLE/Lora transceiver



FPGA Prototype for early software development

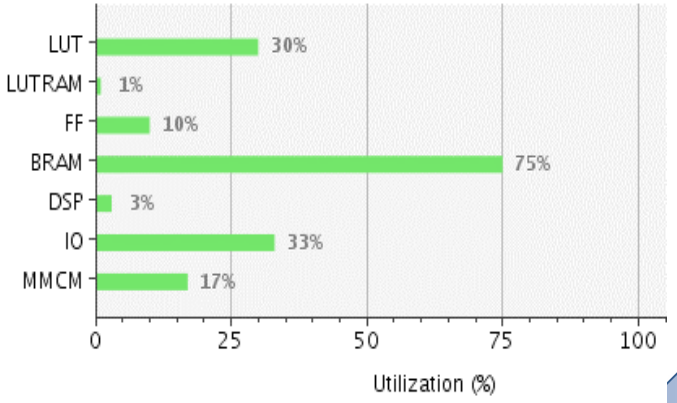
- AES core + Interface: ~23kGEs
- Enc. Throughput: 123Mbps@60MHz
- Enc. Power: 0.7mW@60MHz
- Full chip: 10mW



ASIC prototype on TSMC 65nm (tapeout in September)

Nguyen *et al.*, "A Lightweight AEAD Encryption core to secure IoT applications, APCCAS'20.

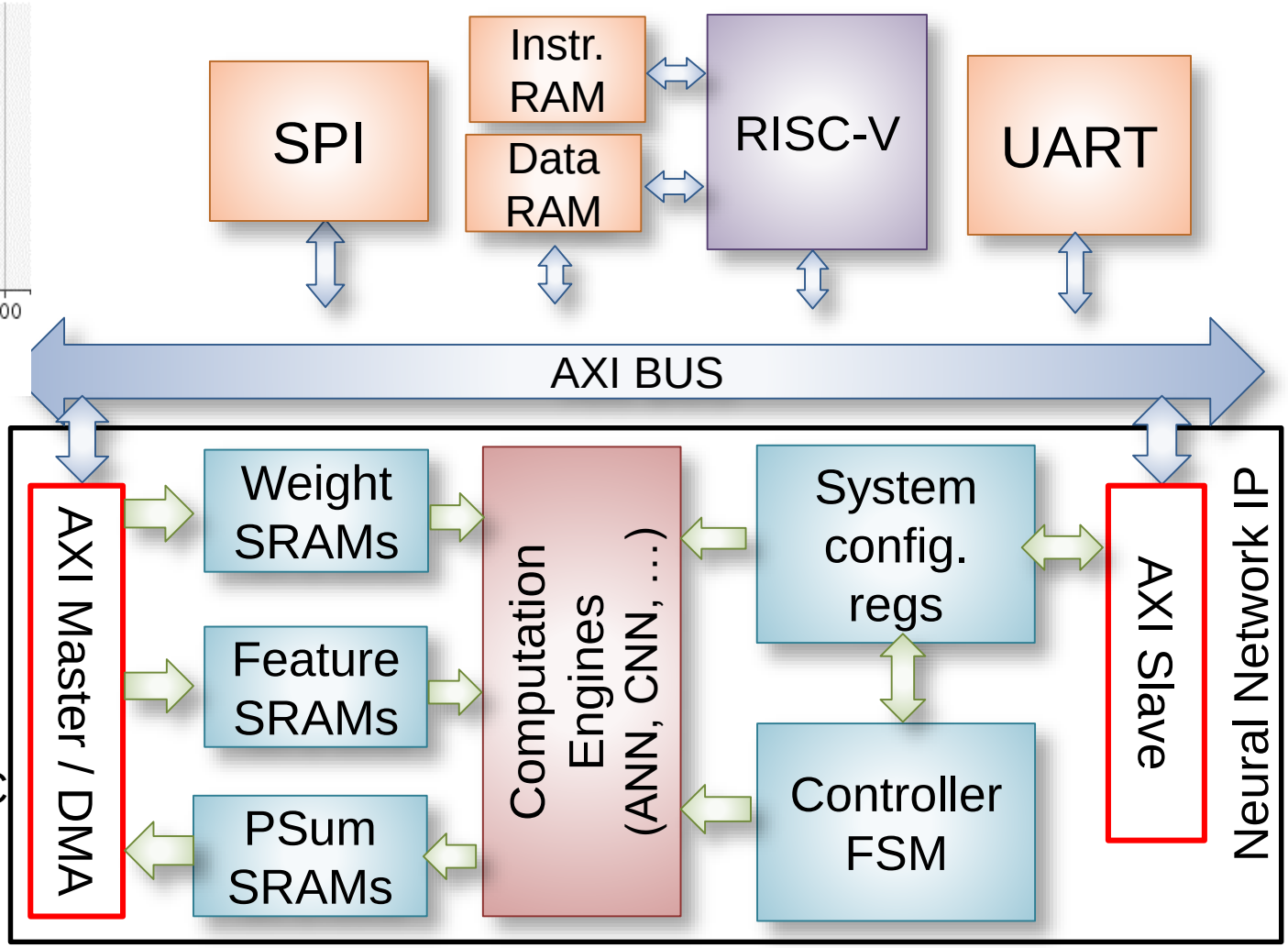
Tiny Neuron Network IP



HW utilization for ANN core with VBP MAC on Arty-A7-100T

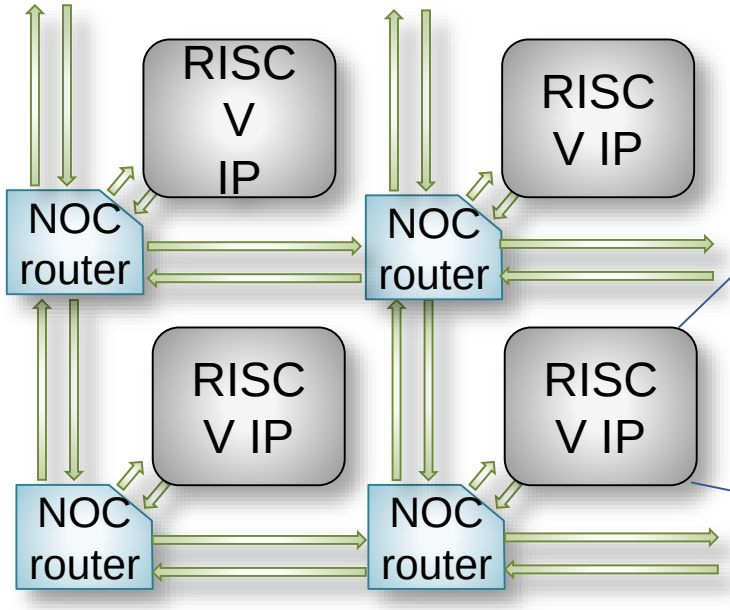
Different MACs:

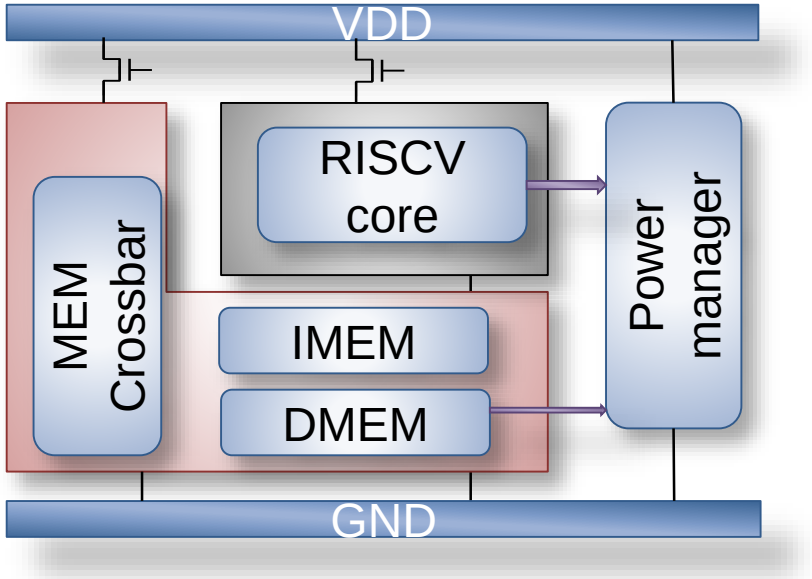
- Normal MAC
- Stochastic MAC
- Variable-bit-precision MAC



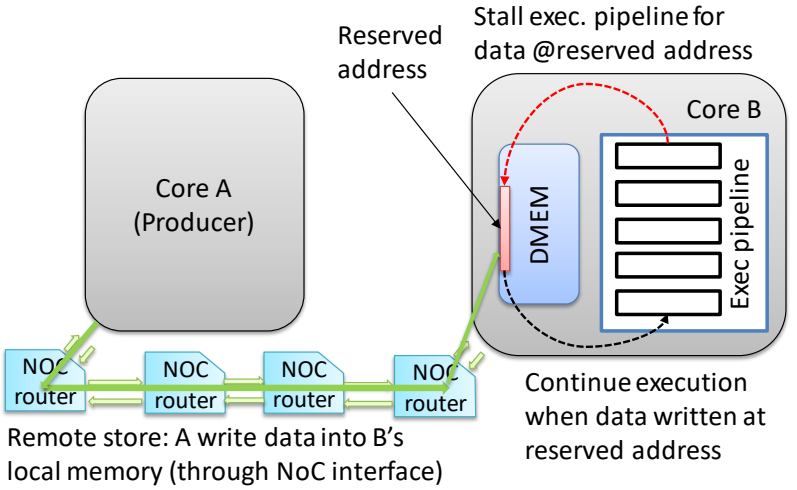
1. Nguyen *et al.*, 'An Efficient Hardware Implementation of Artificial Neural Network based on Stochastic Computing', NICS'18
2. Tran *et al.*, 'A Variable Precision Approach for Deep Neural Networks', ATC'19

Power optimization for multicore RISC-V





- Programming model:
  - Remote Store Programming (RSP)
- Power-gating based on Network Interface & RSP
- Reference system: https://github.com/bespoke-silicon-group/bsg_manycore



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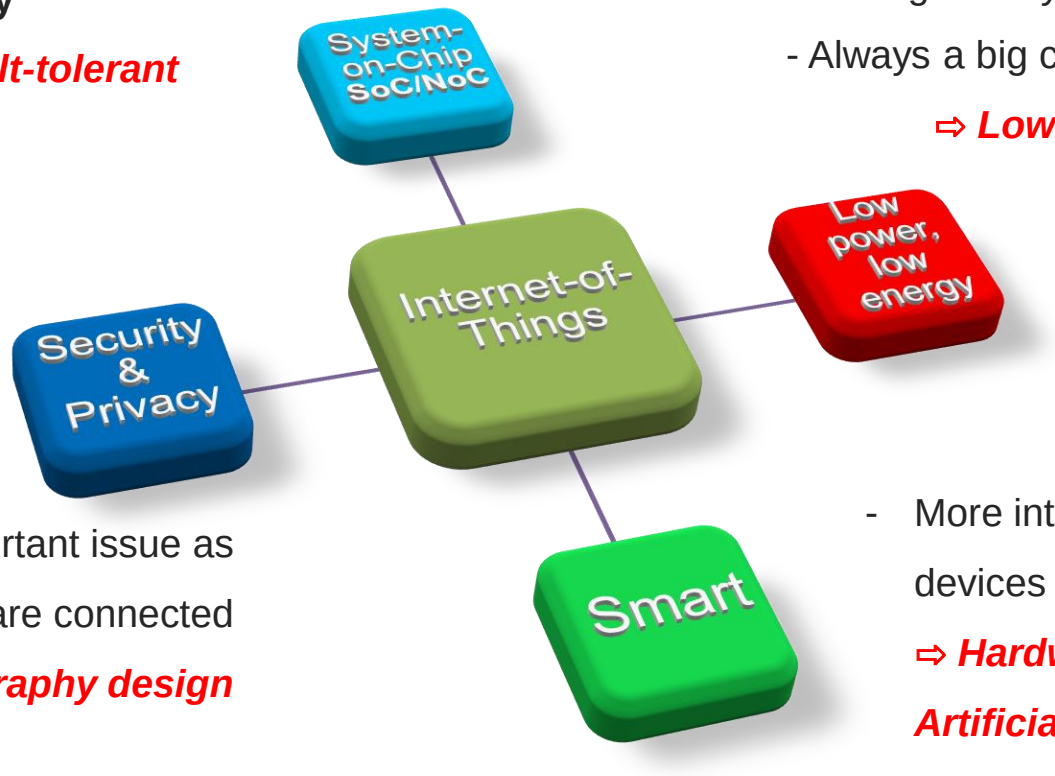
Key research directions

- Multi/many-core system-on-chip
- Testability & **Reliability**

⇨ ***Reconfigurable & fault-tolerant architectures***



- Saving battery !
- Always a big challenge in LSI design

⇨ ***Low Power techniques***

- Become an important issue as the devices are connected

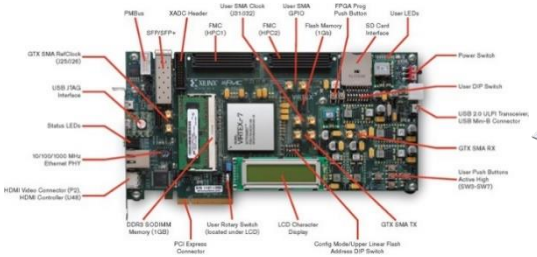
⇨ ***Hardware Cryptography design***

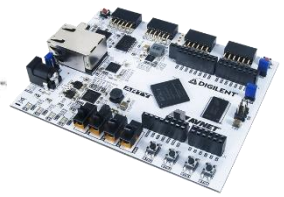
- More intelligent & smarter edge devices

⇨ ***Hardware Acceleration for Artificial Intelligent (AI)***

Building community & ecosystem

- Open source hardware community
  - Share experiences, how-tos, know-hows and resources
  - Support other universities, companies and start-ups





Pushing Hardware design industry in Vietnam

- New projects build around open source ecosystem

CHISEL

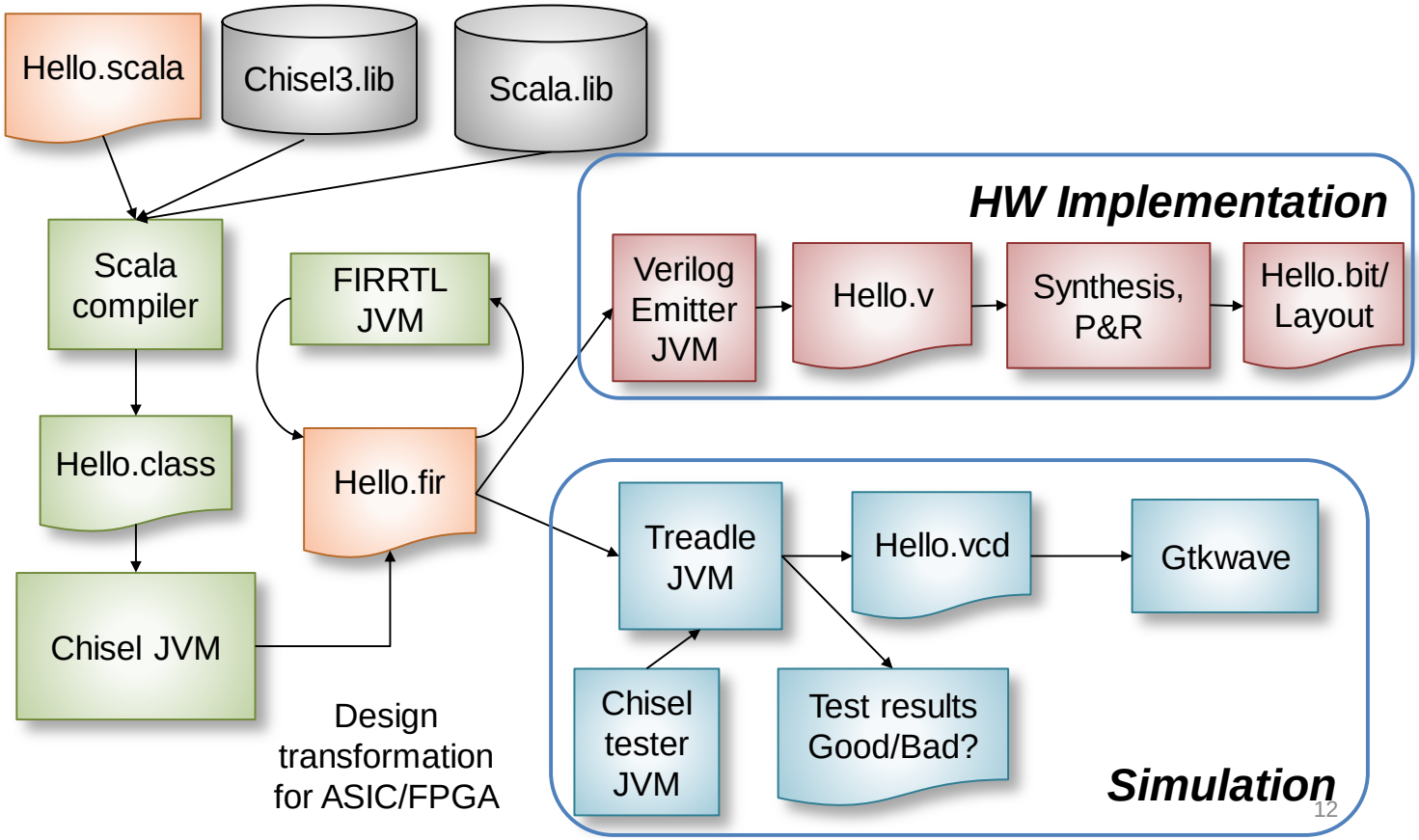
CHIPYARD

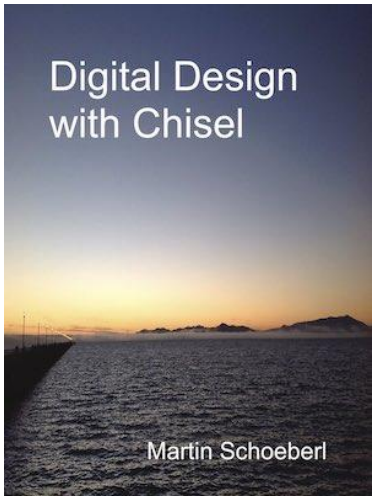
Rocket Chip Generator

SiFive

Education & training

- Chisel training for VNU-UET students (starting from Jan 2020)





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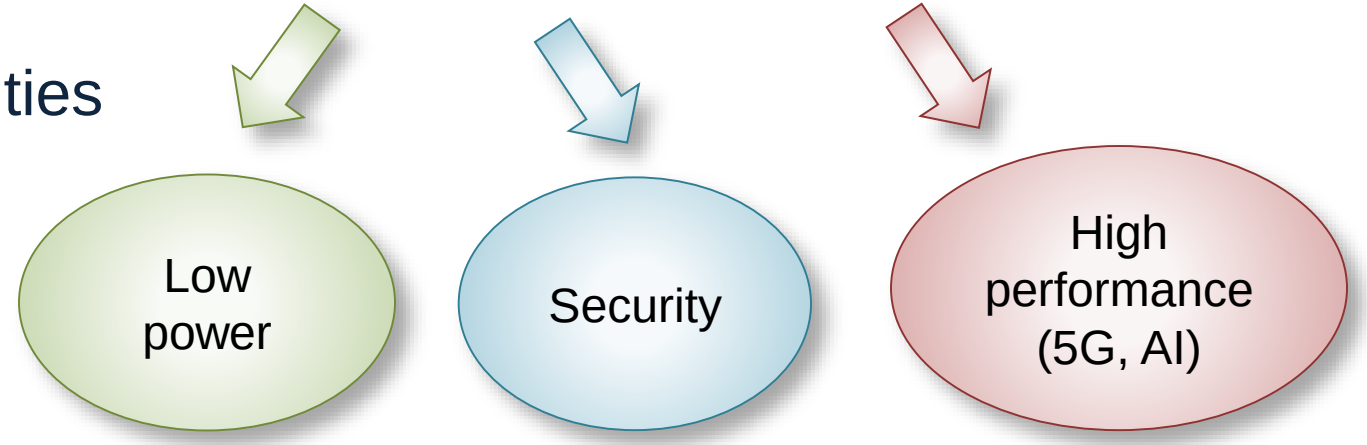
Conclusions

- Open source hardware is maturing

Pulp-platform

- New opportunities



- SISLAB is willing to support the community in Vietnam

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Thank you for your attention!

Xuan-Tu Tran, Duy-Hieu Bui

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