RISC-V Day Tokyo
2023 Summer Conference

SoC Functional Visibility – Introduction to Tessent Embedded Analytics

Hiroshi Fujimatsu

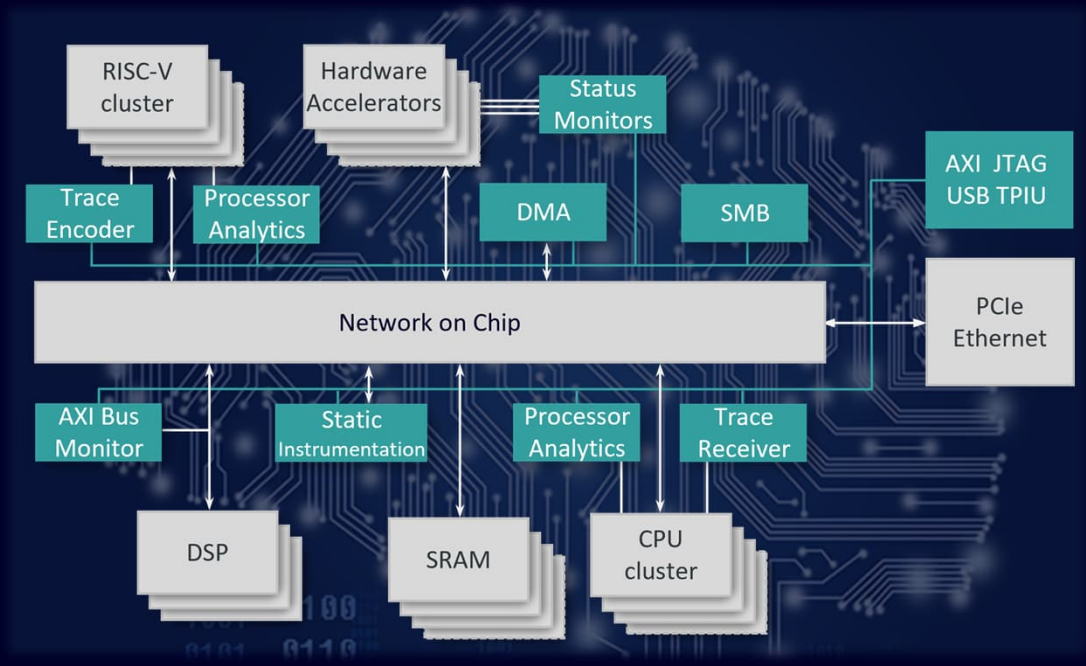
SIEMENS

Born after the acquisition of UltraSoC by Siemens EDA (Mentor Graphics)
Tessent Embedded Analytics targets real technical pain points for SoC developers

A family of non-intrusive RTL modules that observe if your SoC behaves the way it was meant to

A real-time debug and trace environment

- Functional monitoring
- Performance degradations
- Root-cause memory corruption
- Detects malicious security attacks
- Responds at wire speed



SIEMENS

From In-Lab Debug to Analytics In-Life

Monitor the behavior of your device in the lab and in the field

In-Lab

In-Life

SIEMENS

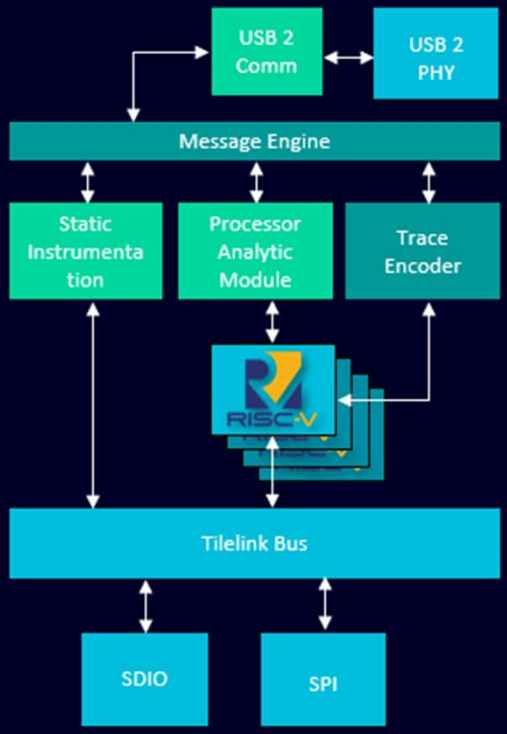
Wireless Start-up Shaves Multiple Months Off Development Cycle

Challenges faced

- New design, new CPU core, tight schedules, limited engineering resources
- Lack of visibility, many unknows in a new core during initial power-up and bring-up
- Engineers looking for a mechanism to monitor program execution of CPU in real time
- Traditional debugging methods are just too slow

Solution with Embedded Analytics IP

- Trace CPU execution, perform run-control, insert breakpoints and watchpoints
- Use the Static Instrumentation IP module for code instrumentation and tracing
- Accelerate debug in the lab by looking at instruction and data trace
- Significantly reduce repair cycle time of both hardware and software



SIEMENS

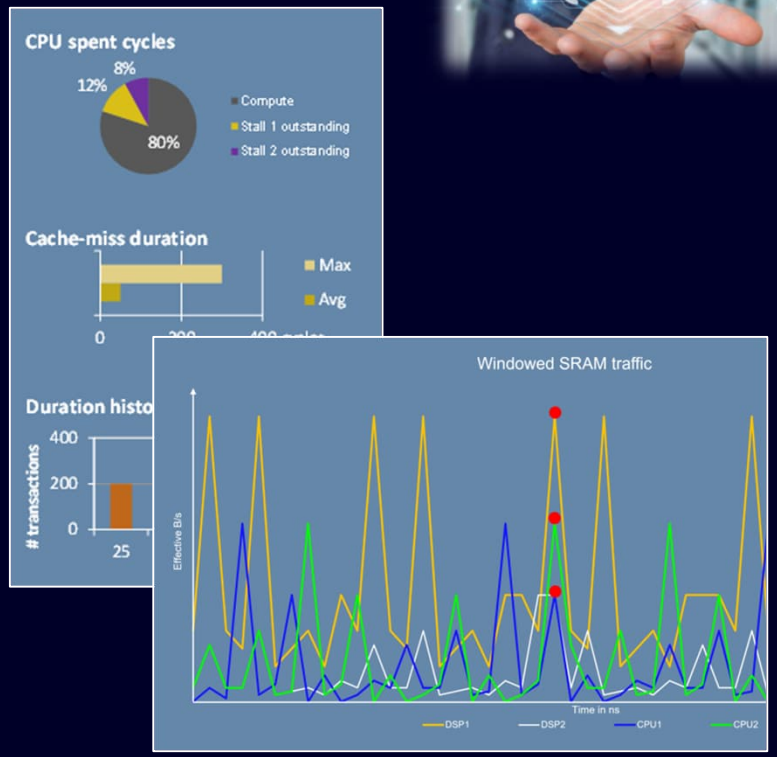
5G Company Solves Performance Degradation Caused by Inefficient Software

Challenges faced

- Extreme complexity in 5G baseband processing
- More frequent software upgrades in the field
- Problems show up years after deployment
- Very difficult to debug in the lab, even worse in the field

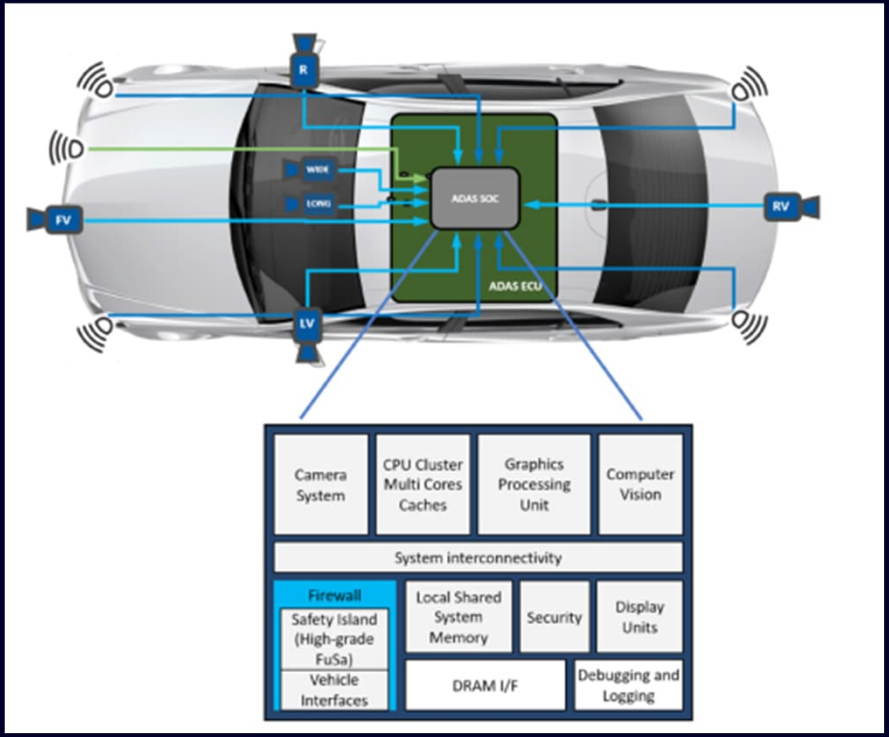
Solution with Embedded Analytics IP

- Optimize code
- Determine efficiency of branch predictor
- Calculate min/max/average duration of cache traffic
- Identify cause of bandwidth degradation

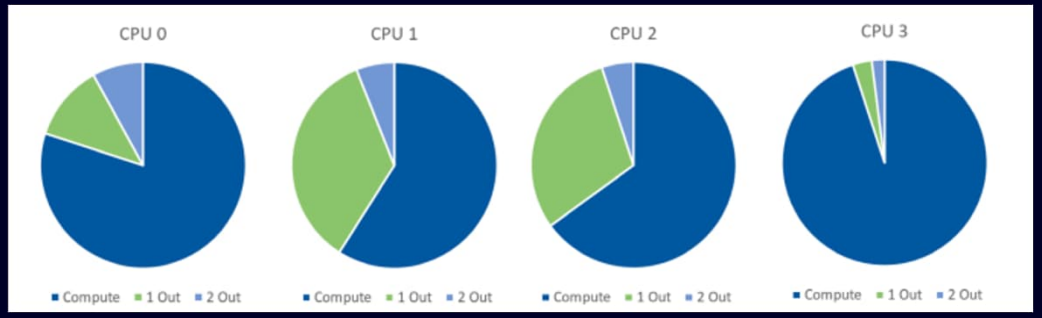


SIEMENS

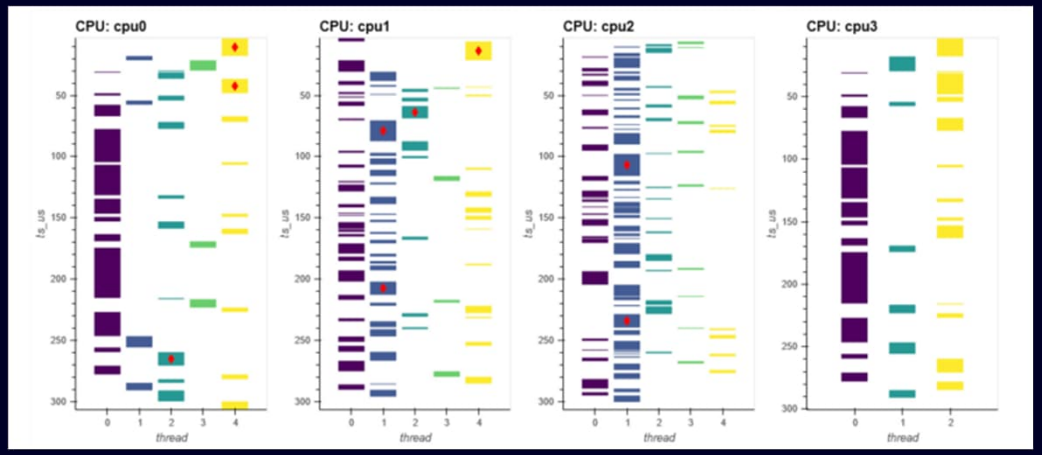
ADAS Performance Monitoring



System behavior is observed on an automotive system instrumented with Tessent Embedded Analytics



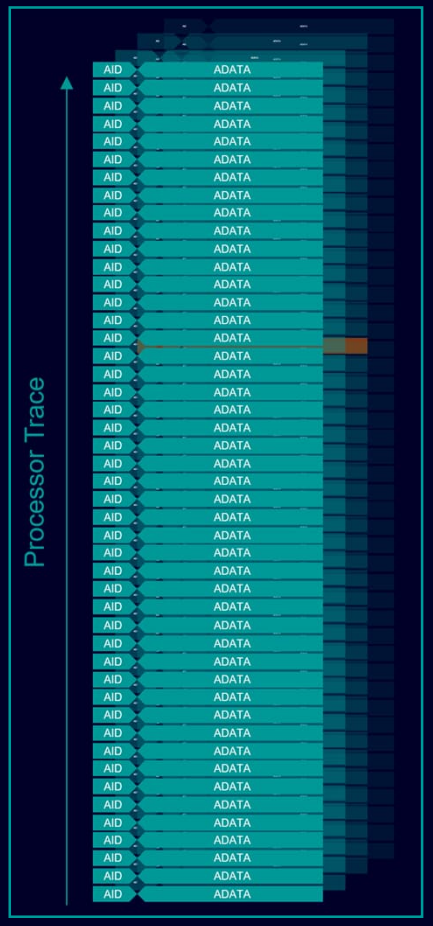
Large number of cache misses on CPU1 & 2, causing bus traffic and impacting overall performance



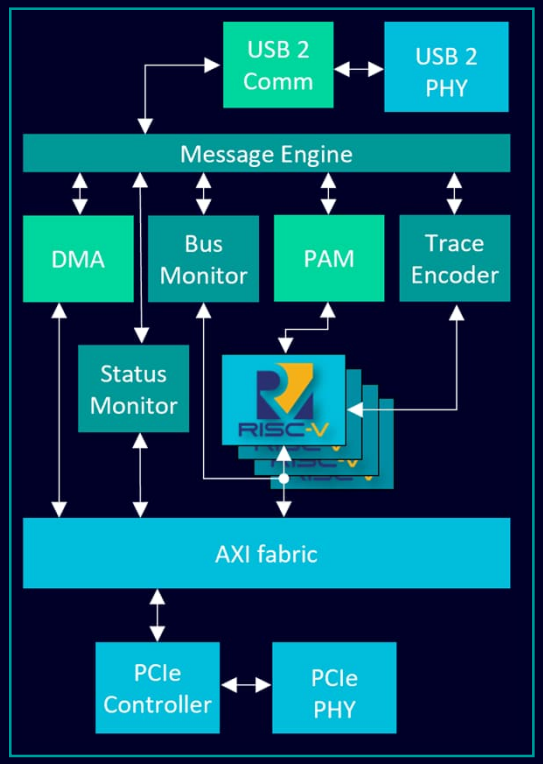
The higher software thread switching behavior on CPU1 & 2 may explain the higher cache misses

SIEMENS

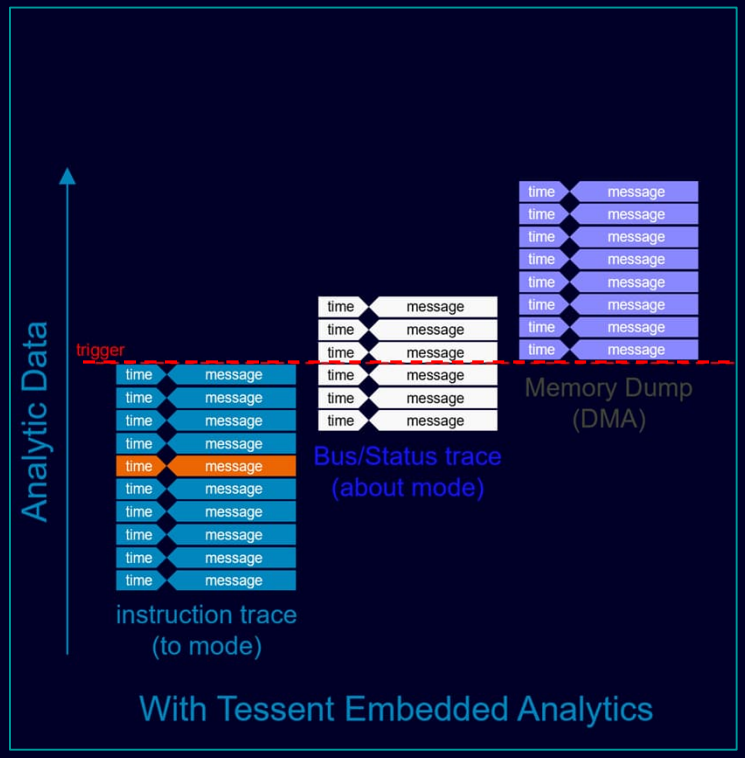
AI Startup with massively parallel AI inference engines Identifies Source of Deadlock using Dynamic Cross Triggering



Traditional methods produce very large amount of trace data



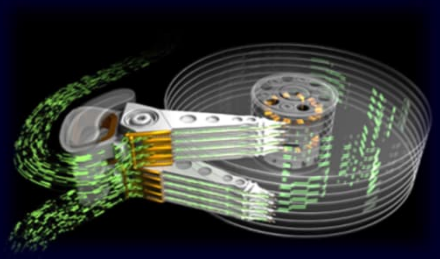
SoC instrumented with Embedded Analytics IP



Capture relevant data around trigger condition Debug trace before, during and after failure

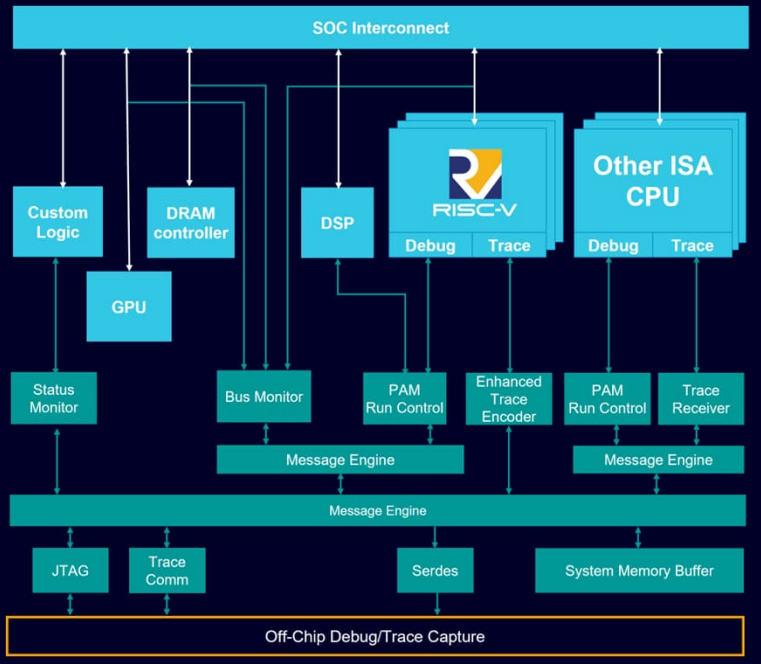
SIEMENS

Storage Company Improves Debug Timeline Using Efficient Trace Encoder



Challenges faced

- Explosive data growth, enormous opportunity for enterprises
- New area-optimized core targeting security applications
- Need for real-time debug not impacting performance

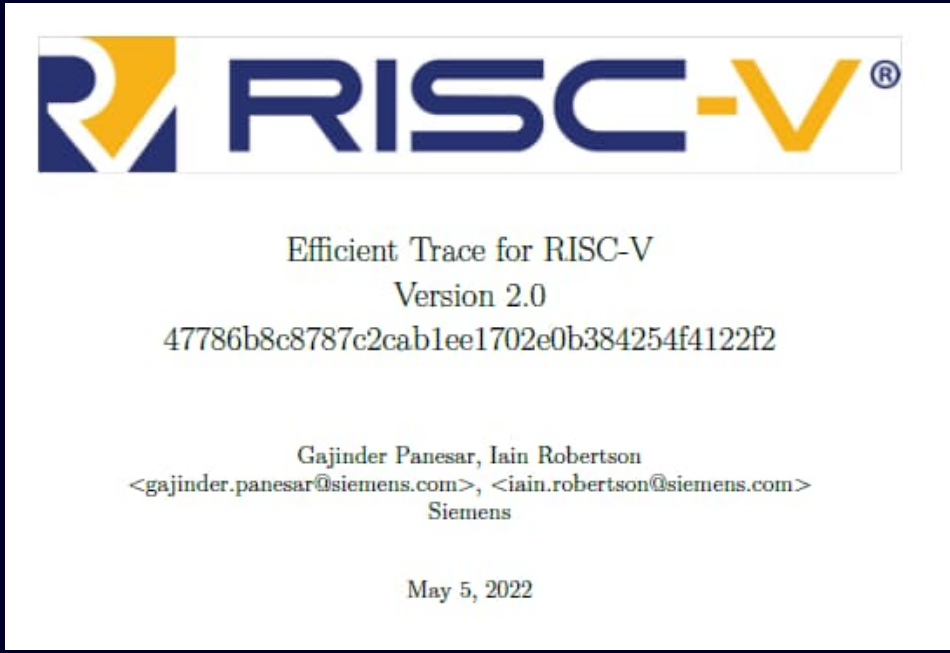


Solution with Embedded Analytics IP

- Trace for longer time periods
- Reduce trace memory buffer requirements
- Avoid trace loss due to backpressure
- Reduce bandwidth requirements on the off-chip transport system

SIEMENS

RISC-V E-Trace Standard

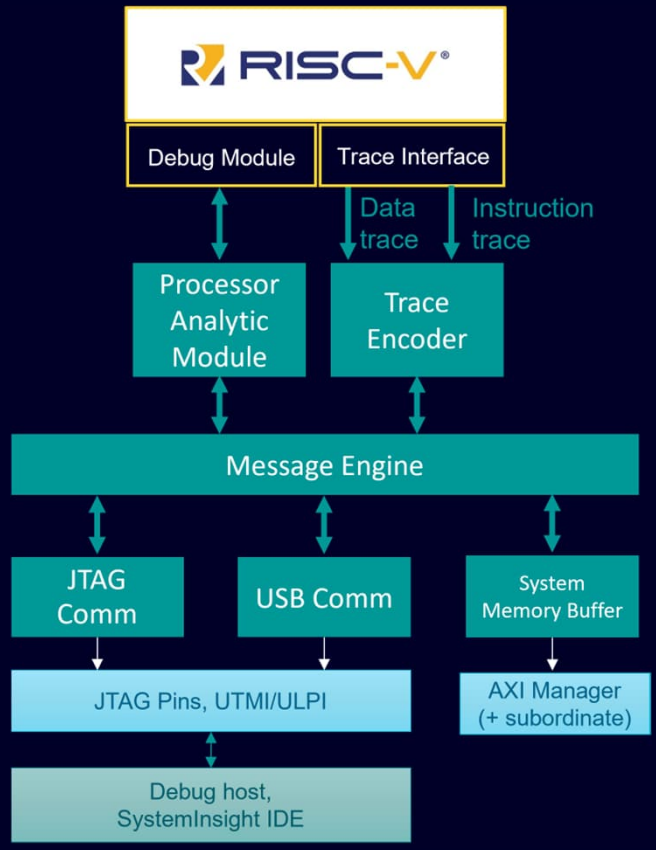


RISC-V®

Efficient Trace for RISC-V
Version 2.0
47786b8c8787c2cab1ee1702e0b384254f4122f2

Gajinder Panesar, Iain Robertson
<gajinder.panesar@siemens.com>, <iain.robertson@siemens.com>
Siemens

May 5, 2022



SIEMENS

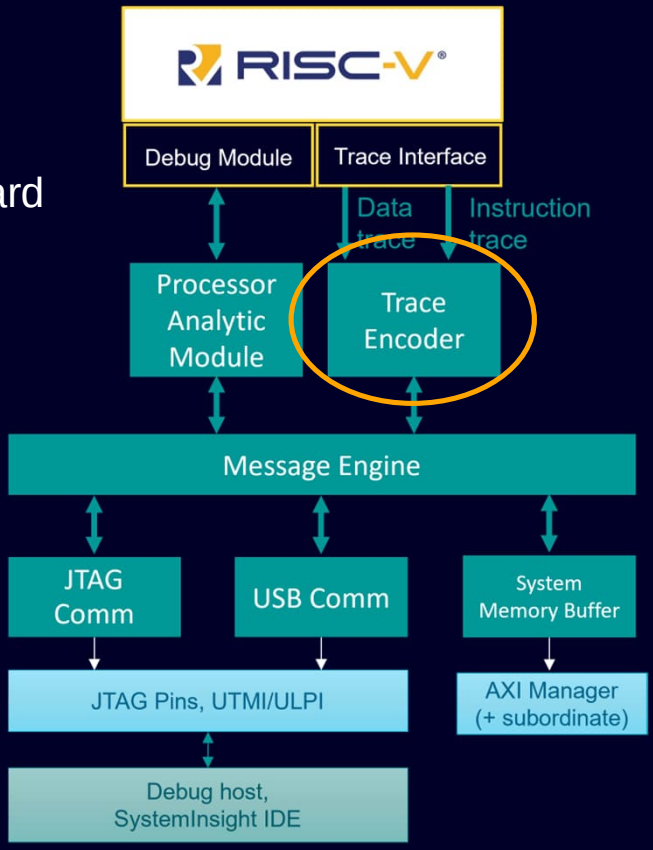
E-Trace Encoder IP

Siemens EDA developed the E-Trace Encoder IP

- Compliant with the hart to encoder interface defined in the standard
- Implements the trace algorithms defined in the standard
- Integrates seamlessly into the Tessent Embedded Analytics infrastructure

The IP supports a wide range processor trace scenarios

- Single and Multi-retirement harts
- Instruction and data trace (optional)
- Cycle-accurate instruction trace (optional)
- Additional optional modes to improve trace efficiency



SIEMENS

Summary

Tessent Embedded Analytics helps deal with the systemic complexity of large SoCs, providing intimate visibility of the real-world behavior of entire systems

The ultimate benefits include:

- **Faster time-to-market**
- **Lower development cost**
- **Robustness against malicious intrusions**
- **Enhanced product safety**
- **Reduced system power consumption**
- **Better performance overall, including fine-tuning of end products even after they are deployed in the field**

SIEMENS

Thank you

Published by Siemens DISW

Hiroshi Fujimatsu
Field Application Engineer
Tessent™ Silicon Lifecycle Solutions
E-mail hiroshi.fujimatsu@siemens.com

SIEMENS