Imagination

Imagination university programme

RVfpga-SoC

How to go from a RISC-V Core to a RISC-V SoC?

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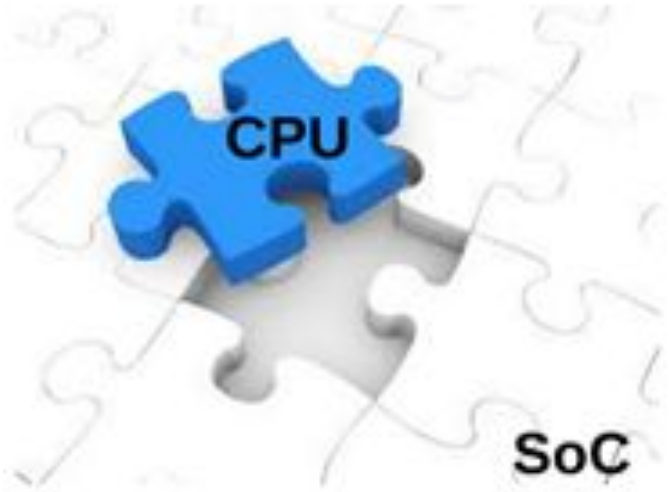
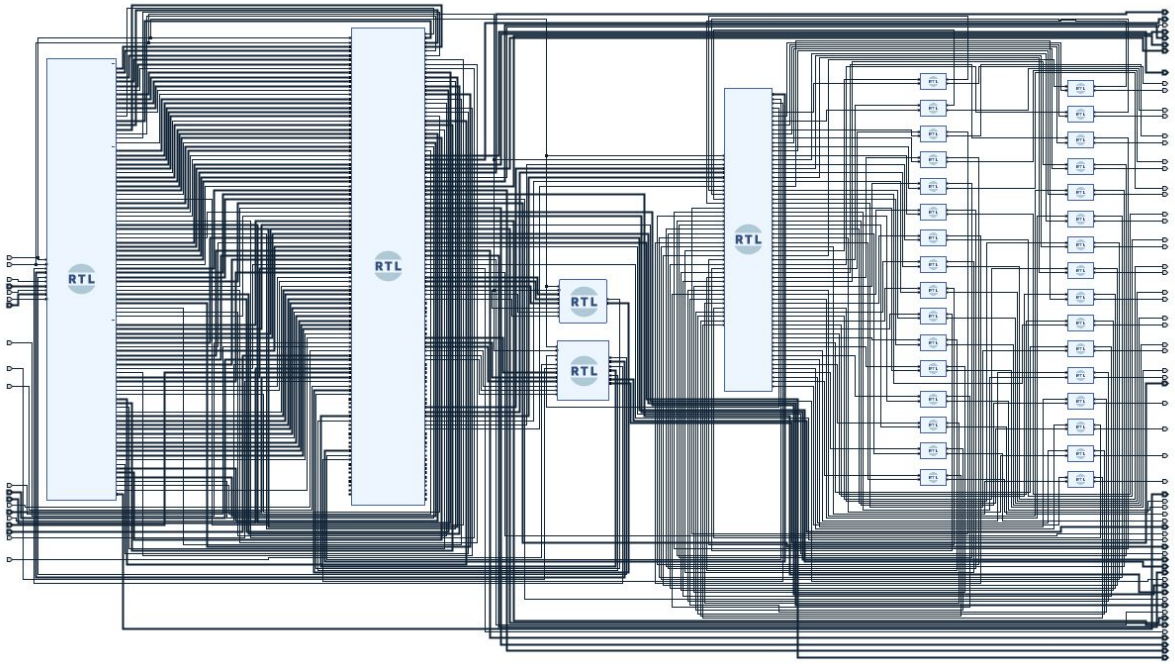
What is a System on Chip (SoC)?

An **SoC** is an integrated circuit or an IC that integrates an entire electronic or computer system onto it.



The challenge

Very little material about how to **make** an SoC



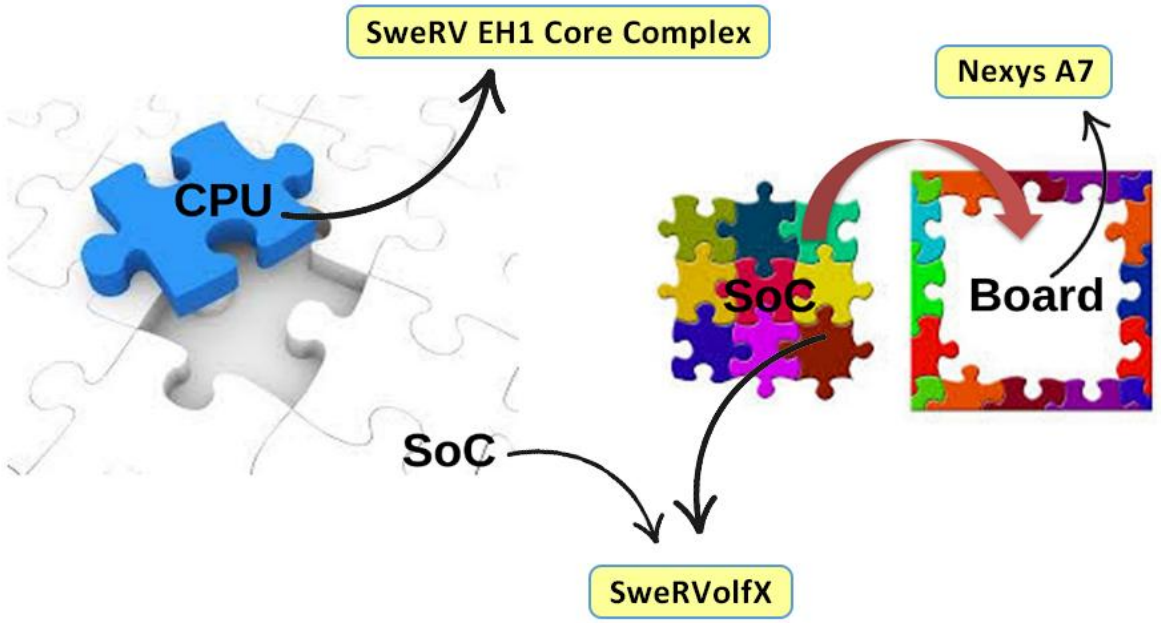

```
//*****************************************************
module swerv
   import swerv_types::*;
(
   input logic                 clk,
   input logic                 rst_l,
   input logic                 dbg_rst_l,
   input logic [31:1]          rst_vec,
   input logic                 nmi_int,
   input logic [31:1]          nmi_vec,
   output logic                core_rst_l,   // This

   output logic [63:0] trace_rv_i_insn_ip,
   output logic [63:0] trace_rv_i_address_ip,
   output logic [2:0]  trace_rv_i_valid_ip,
   output logic [2:0]  trace_rv_i_exception_ip,
   output logic [4:0]  trace_rv_i_ecause_ip,
   output logic [2:0]  trace_rv_i_interrupt_ip,
   output logic [31:0] trace_rv_i_tval_ip,
```

What is RVfpga-SoC?

A set of teaching materials explaining how to design and build an SoC

- **CPU**
  - SweRV EH1
- **SoC**
  - SwerVolfX
- **Board**
  - Nexys A7
- **Simulator**
  - Verilator



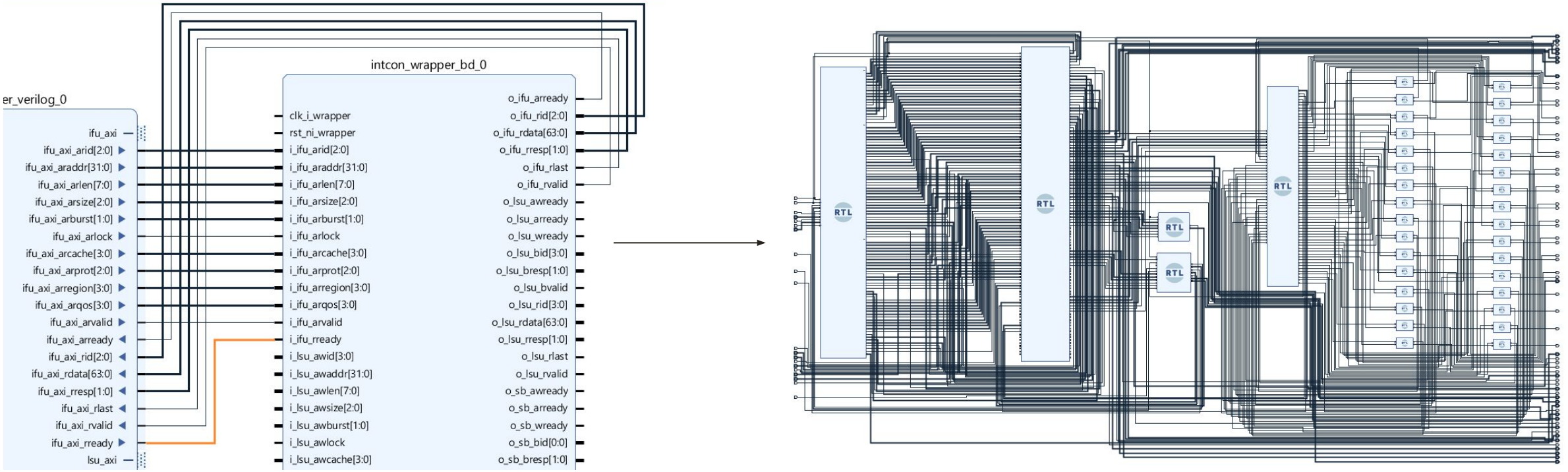
What does RVfpga-SoC include?

RVfpga-SoC Course includes following five extensive labs:

1. Introduction to RVfpga-SoC
2. Running Software on the RVfpga-SoC
3. Introduction to SweRVolf and FuseSoC
4. Building and Running Zephyr on SweRVolf
5. Running Tensorflow Lite on SweRVolf

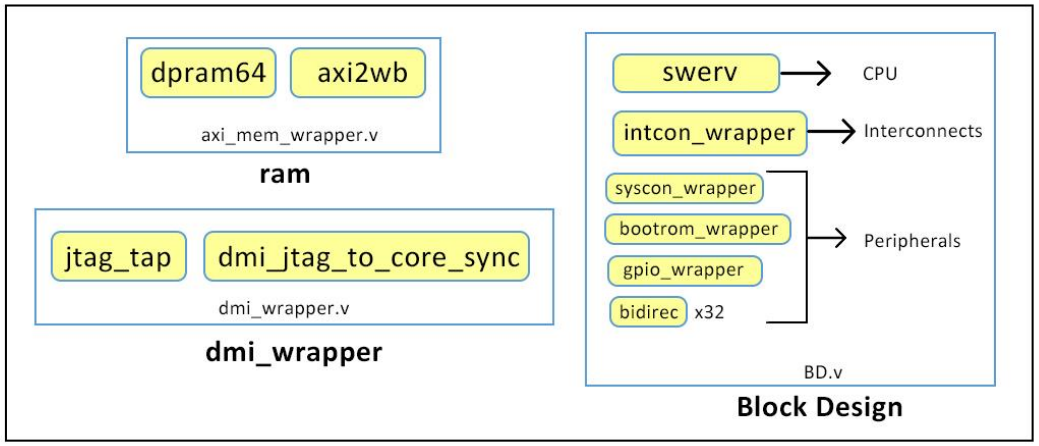
Lab 1: Building an SoC (Visual approach)

Wire CPU, Interconnect, Peripherals, Clock, Memory, Reset etc.

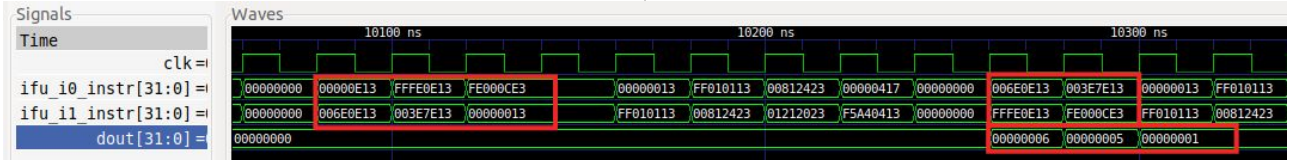


Lab 2: Running Software on RVfpga-SoC

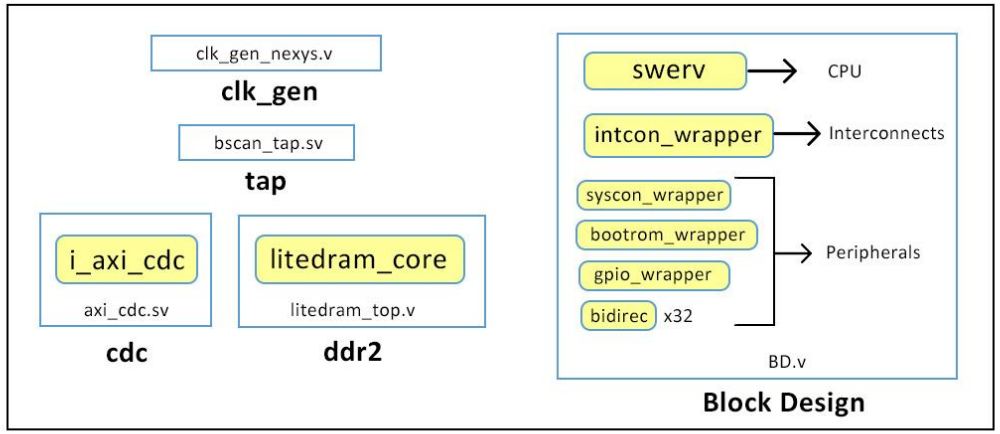
Run C programs on the SoC created in Lab 1



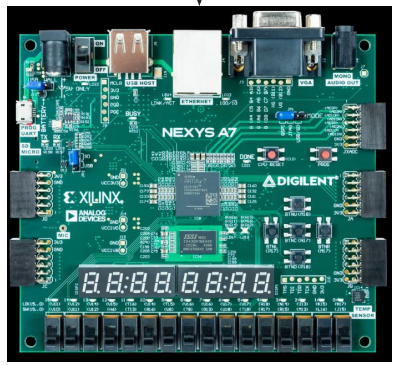
RVfpga Sim



Simulation



RVfpga Nexys



Nexys A7 Implementation

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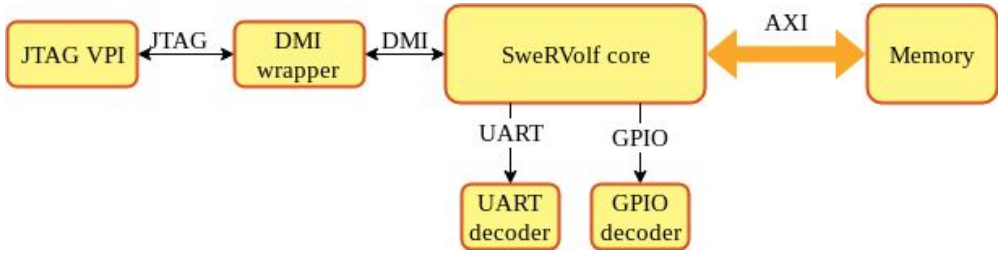
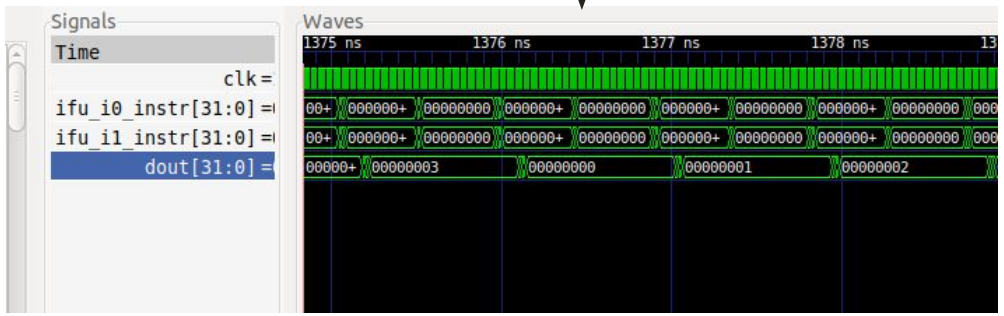
Lab 3: FuseSoC approach to SoC design

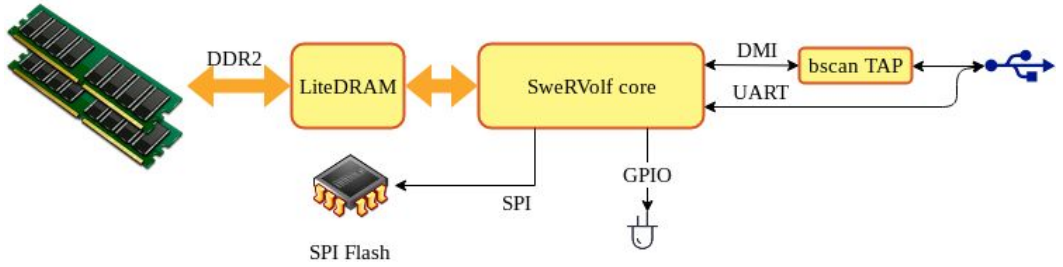
FuseSoC does all of this tedious work that we manually did in Labs 1 and 2



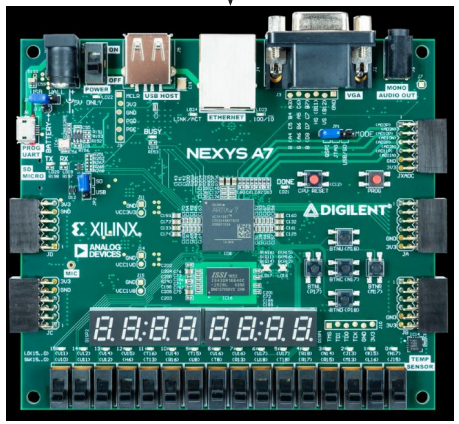
SweRVolf Sim



Simulation



SweRVolf Nexys



Nexys A7 Implementation

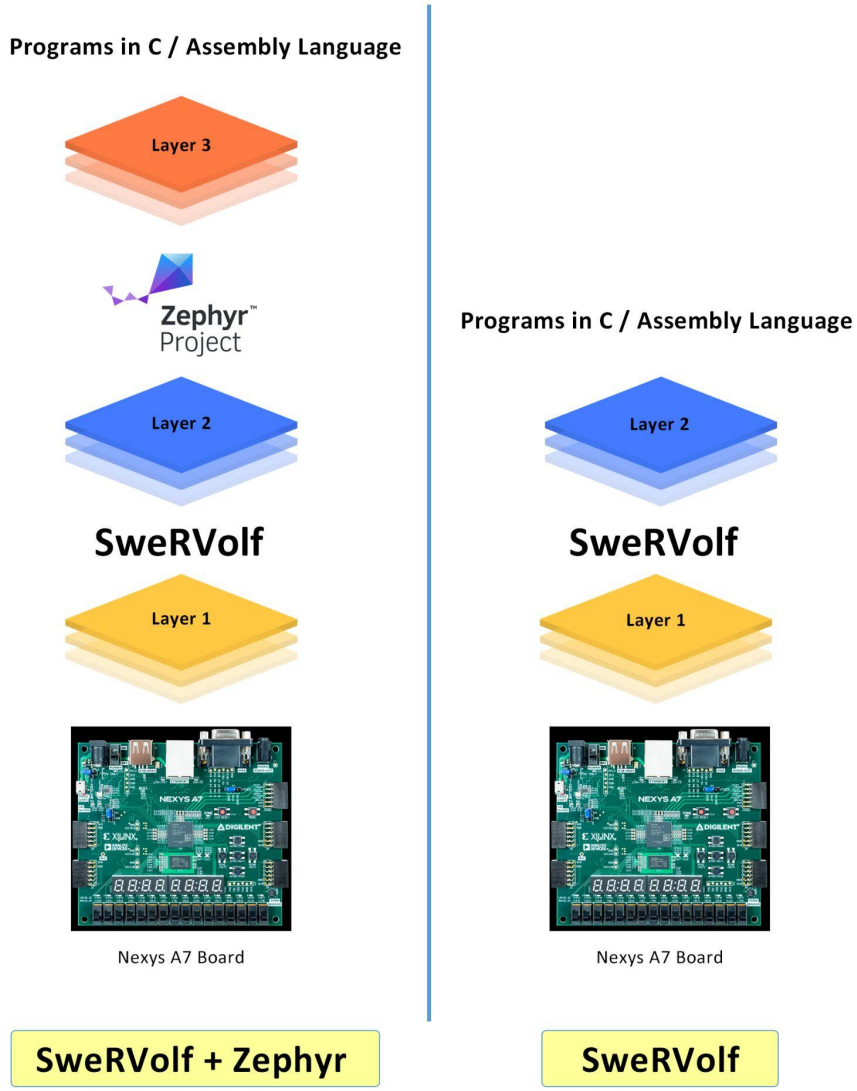
Lab 4: Running Zephyr on SweRVolf

Building and Running Zephyr (an RTOS: Real Time Operating System) on SweRVolf.

```
make[1]: Leaving directory '/home/hamza/SweRVolf/build/swervolf_0.7.3/sim-verilator'
INFO: Running
INFO: Running simulation
Loading RAM contents from /home/hamza/SweRVolf/zephyr/samples/philosophers/App.hex
Releasing reset
*** Booting Zephyr OS build zephyr-v2.4.0  ***

Philosopher 0 [P: 3]    HOLDING ONE FORK
Philosopher 1 [P: 2]   EATING  [  125 ms ]
Philosopher 2 [P: 1]  THINKING [  175 ms ]
Philosopher 3 [P: 0]   EATING  [  325 ms ]
Philosopher 4 [C:-1]  THINKING [  400 ms ]
Philosopher 5 [C:-2]        STARVING
```

```
Demo Description
----------------
An implementation of a solution to the Dining Philosophers
problem (a classic multi-thread synchronization problem).
This particular implementation demonstrates the usage of multiple
preemptible and cooperative threads of differing priorities, as
well as dynamic mutexes and thread sleeping.
```



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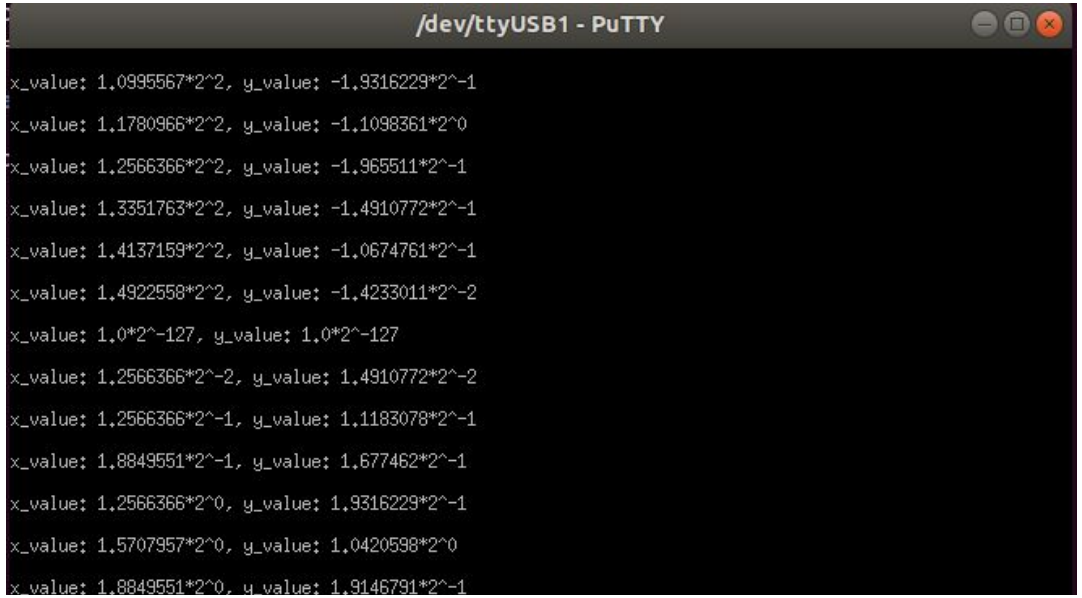
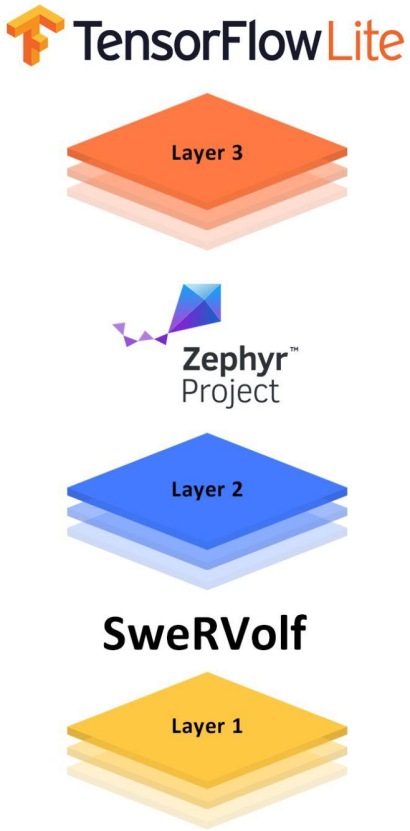
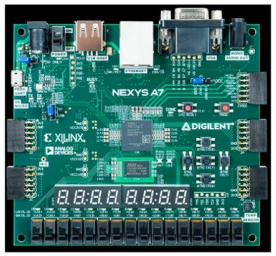
Lab 5: Run Tensorflow Hello World

The Hello World example is designed to demonstrate the absolute basics of using TensorFlow Lite for Microcontrollers. This program trains and runs a model that replicates a sine function.







Nexys A7 Board

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Two Courses: RVfpga vs. RVfpga-SoC (1)

RVfpga and RVfpga SoC are two courses. RVfpga focuses more on aspects inside the CPU core. RVfpga-SoC focuses more on aspects outside the CPU core.

Lab 0: RVfpga Experiment Overview
Lab 1: Creating a Vivado Project
Lab 2: Programming in C
Lab 3: RISC-V assembly language
Lab 4: Function calls
Lab 5: Image processing: C and assembly

Programming

Lab 6: Introduction to 1/O
Lab 7: 7-segment display
Lab 8: Timers
Lab 9: Interrupt driven I/O
Lab 10: Serial Bus

I/O systems

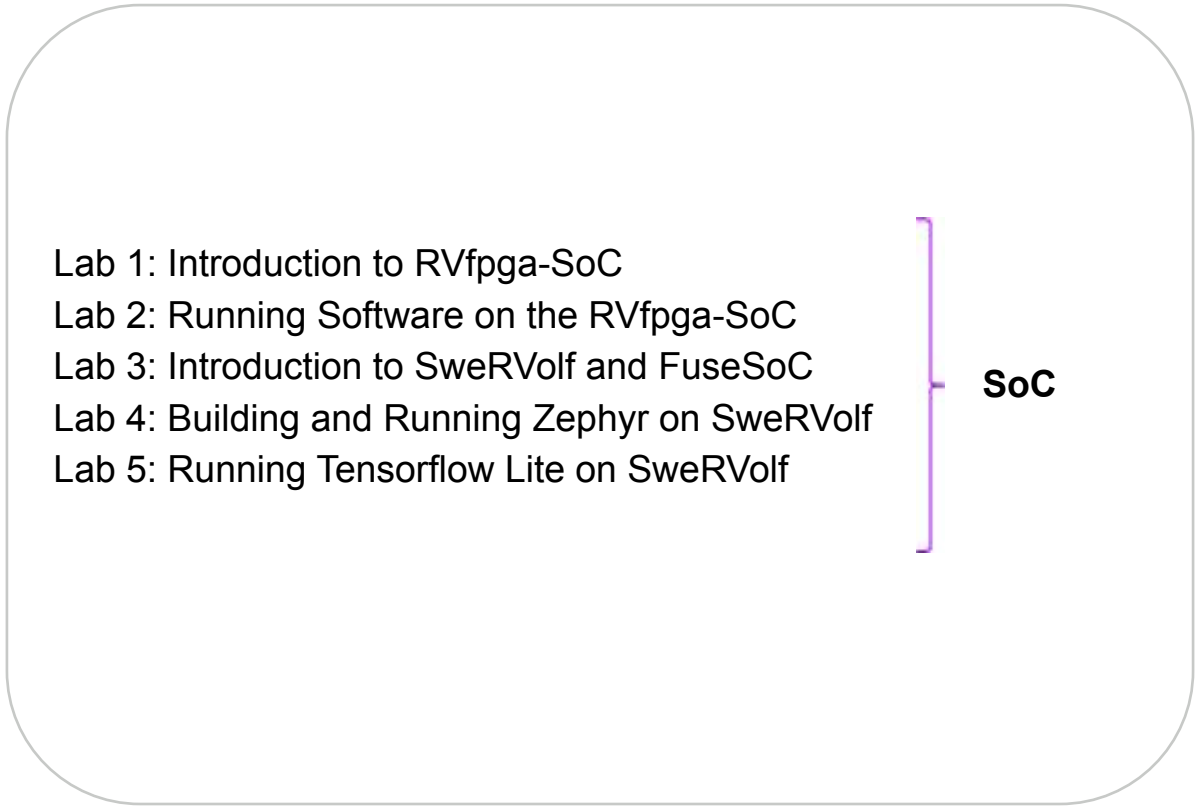
Lab 11: SweRV EH1 Configuration and Organization. Performance Monitoring
Lab 12: Arithmetic/Logical Instructions: the add instruction
Lab 13: Memory Instructions: the lw and sw instructions
Lab 14: Structural Hazards
Lab 15: Data Hazards
Lab 16: Control Hazards. Branch Instructions: the beq Instruction. The Branch.
Lab 17: Superscalar Execution
Lab 18: Adding New Features (Instructions, Hardware Counters) to the Core
Lab 19: Memory Hierarchy. The Instruction Cache.
Lab 20: ICCM and DCCM

Investigate, analyze, and modify the RISC-V core and memory system.

RVfpga

Two Courses: RVfpga vs. RVfpga-SoC (2)

RVfpga and RVfpga SoC are two courses. RVfpga focuses more on aspects inside the CPU core. RVfpga-SoC focuses more on aspects outside the CPU core.



RVfpga-SoC

Closing Remarks

From Verilog, to SoC, to RTOS, to Tensorflow

- All source code visible

A set of 5 labs that walk through students on how to set things up

Acknowledgements

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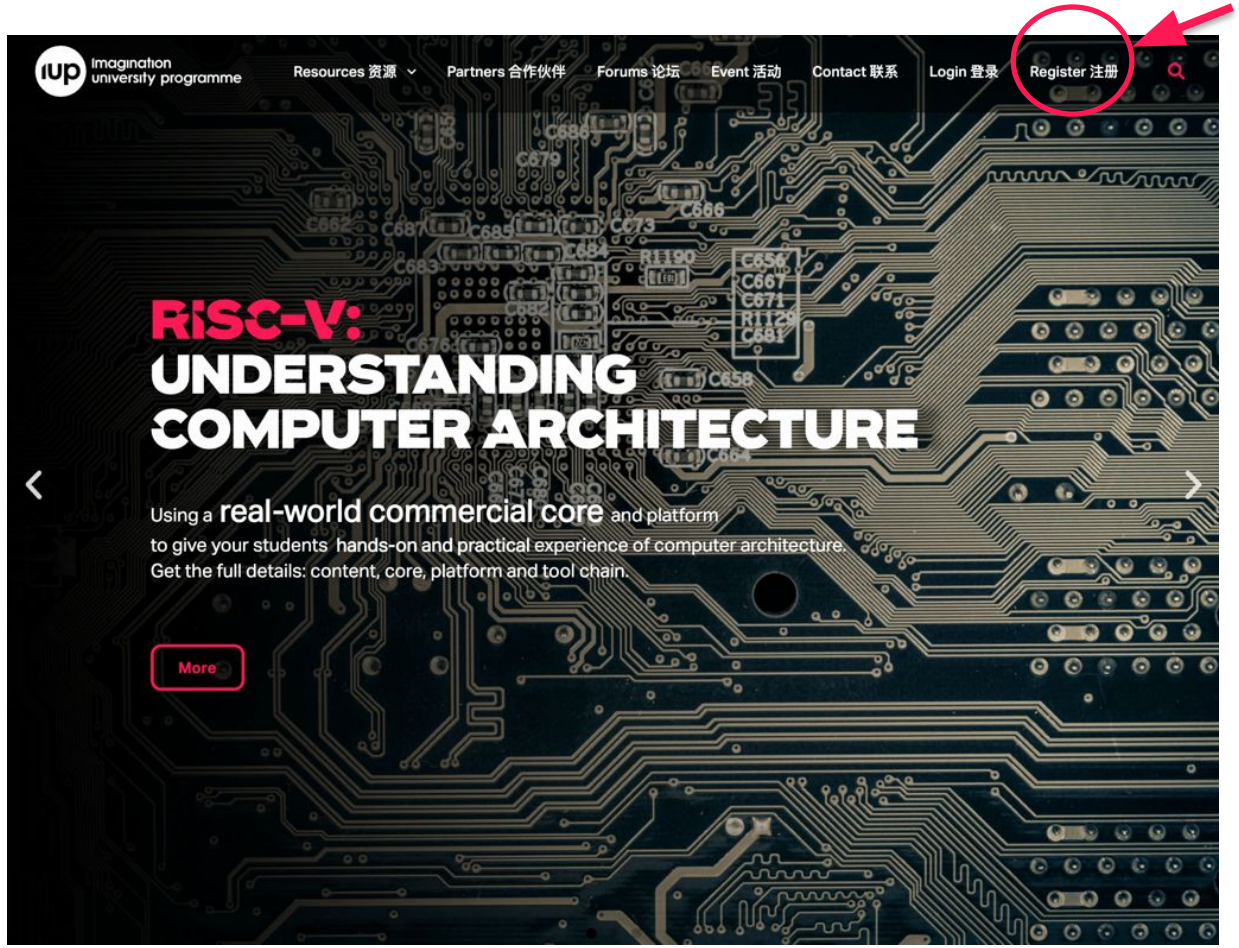

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