Why We Are Using RISC-V as a Model Processor for university education ?

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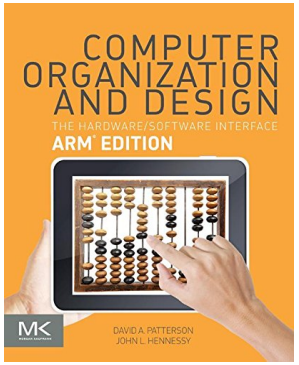
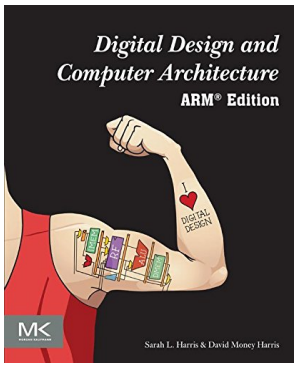
Most university used MIPS R3000 as a model processor for education

- Benefits:
  - Simple ISA and an elegant
    5-stage pipeline microarchitecture
  - Rich materials:
    - Harris&Harris “Digital Design and Computer Architecture”
    - Patterson&Hennessy “Computer Organization and Design”
    - Hennessy&Patterson “Computer Architecture”
    - MIPSfpga, simulators, compilers/assemblers
- Problems:
  - Almost not used in the real world.
    - Somehow old fashioned?
    - Poor scalability.
  - Software eco-system is rather poor.

How about ARM?

- There were trials to change MIPS to ARM.
  - Patterson&Hennessy “Computer Organization and Design: ARM edition”
  - Harris&Harris “Digital Design and Computer Architecture: ARM edition”
- Benefits
  - The most popularly used computer architecture in the world.
  - Rich eco-system.
- Problems
  - Complicated microarchitecture and old-fashioned ISA.
    - Harris&Harris’s textbook did the best to build MIPS-like ARM 5-stage pipeline, but it is still too messy for students.
  - Eco-system is rich but is not fully open for education.

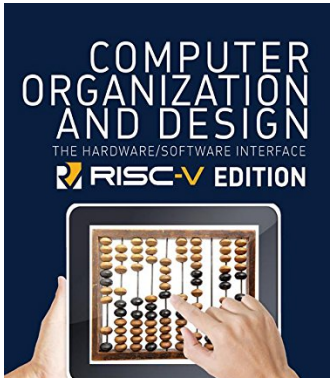


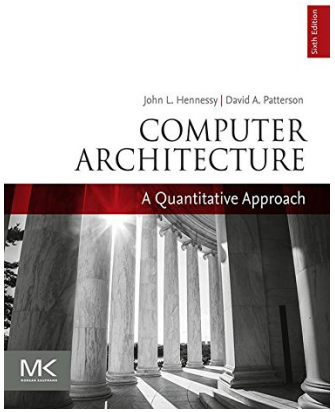


Is RISC-V ideal solution as a model processor for education?

- Benefits
  - Developing in the real world.
  - Rich and fully open software eco-system.
  - Modern and extendable ISA and simple microarchitecture
    - RV32I, the base ISA is simple, but there are a lot of extensions.
  - Materials are developing.
- But there are some problems.
  - Instruction field of RV32I is slightly complicated.
  - Some instructions stretch the critical path.

Sorry Kawasaki-san, it is not for simply admiring RISC-V.
But very practical for university teachers.





Instruction Set Architecture

RISCV RV32I vs. MIPS R3000

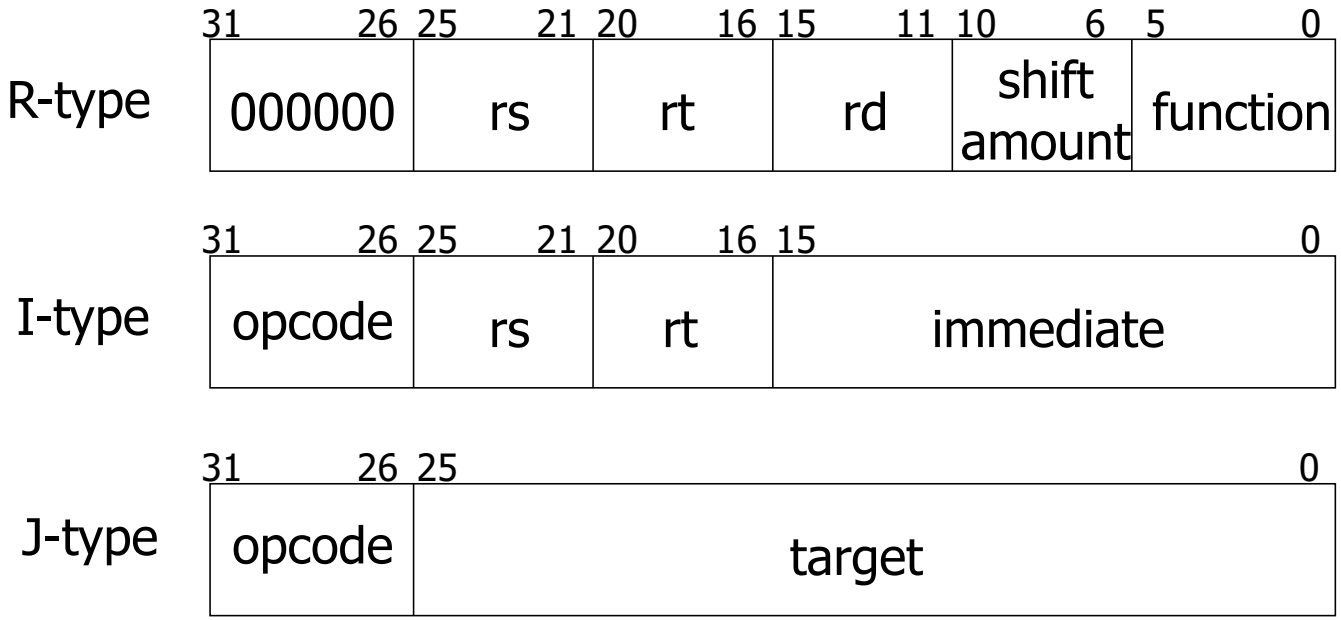
- Major instructions are common.
  - Typical RISC-style:
    - Register-register architecture
    - Fixed size instruction
    - Well selected, limited number of instructions
- Easy to switch from R3000 to RV32I.

Difference	RV32I	R3000
Instructions only provided	bge, bgeu, blt, bltu, auipc	nor, j, jr, lwl, lwr, swl, swr
Offset/Immediate/Branch target	12bit, Sign extension	16bit, sign extension is only for arithmetic instructions
Jump and Link	PC can be saved in any registers. j and jr are pseudo instructions.	jal and jalr save PC into $31.
Comparison in size	Both ways to use bge/blt and slt.	Only done with slt.

Instruction fields are completely different

MIPS R3000

- Only three types.
- Immediate field is fixed.
- The role of ‘rt’ is depending on the instructions.



Fielding of RV32I is rather complicated

Register-Register

000	add,sub(30b)	101	srl, sra(30b)
001	sll	110	or
010	slt	111	and
011	sltu		
100	xor		

Immediate

000	addi	101	srli, srai (30b)
001	slli	110	ori
010	slti	111	andi
011	srliu		
100	xori		

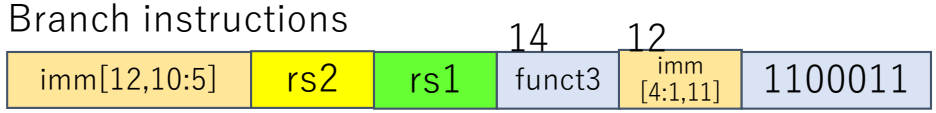
Load instructions

000	lb
001	lh
010	lw
100	lbu
101	lhu

Store instructions

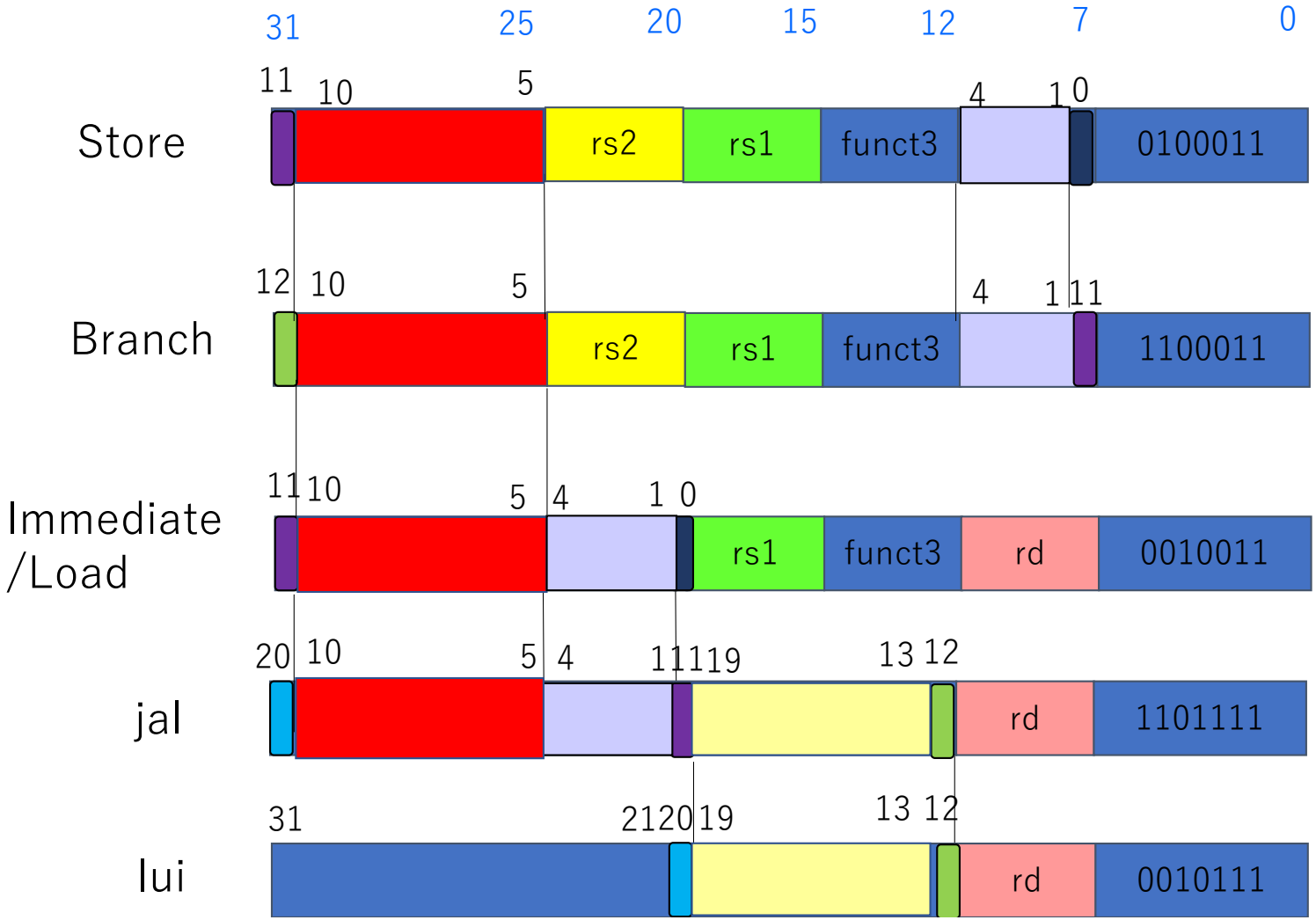
000	sb
001	sh
010	sw

Branch instructions



000	beq	001	bne
100	blt	101	bge
110	bltu	111	bgeu

Immediate bit location is considered to reduce multiplexors.



The benefits of complicated bit field

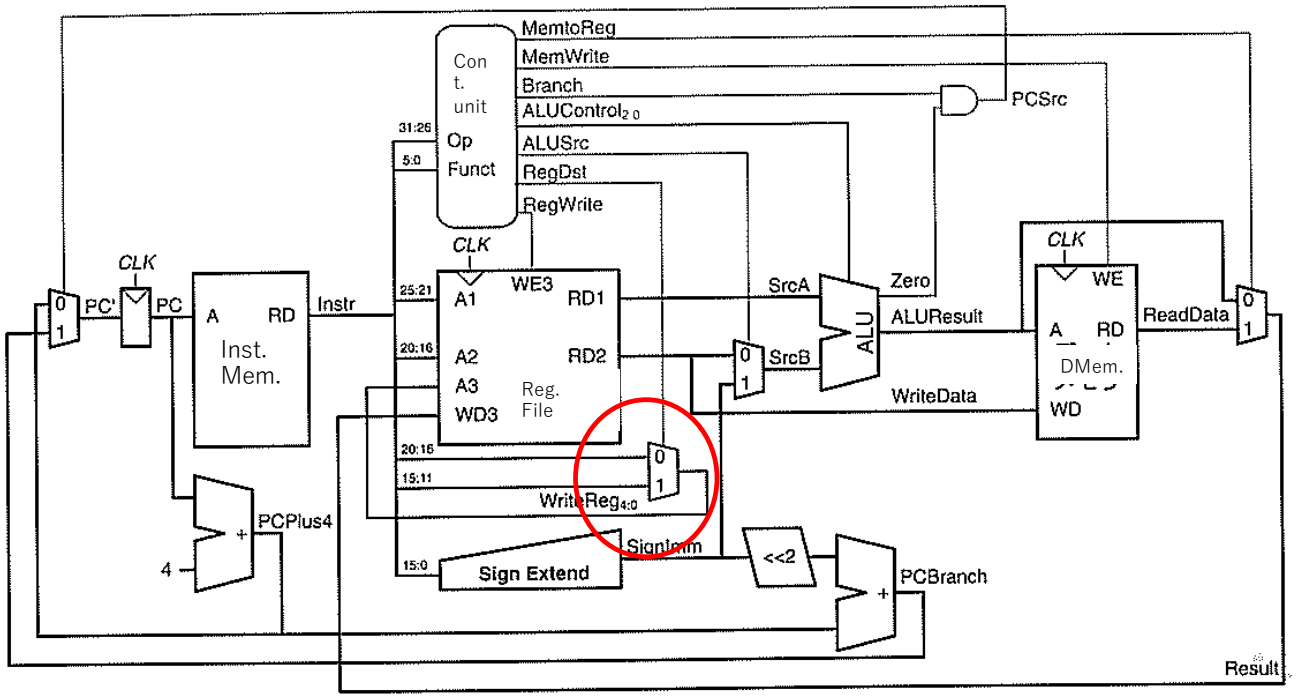
- Imitated TSMC 0.18 μ m library by Oklahoma university.
- Synopsys Design Compiler: N2017.09-SP1
- The combinatorial area is reduced by 1.3% compared with the case without consideration.
- The operational speed is not influenced.
- The problem in education:
  - Hand-assemble is almost impossible.
  - Verilog description becomes hard to be understood.

```
assign imm_i = {funct7,rs2};
assign imm_s = {funct7,rd};
assign imm_b = {funct7[6],rd[0],funct7[5:0],rd[4:1],1'b0};
assign imm_j = {instr[31], instr[19:12],instr[20],instr[30:21],1'b0};
assign imm_u = instr[31:12];
```

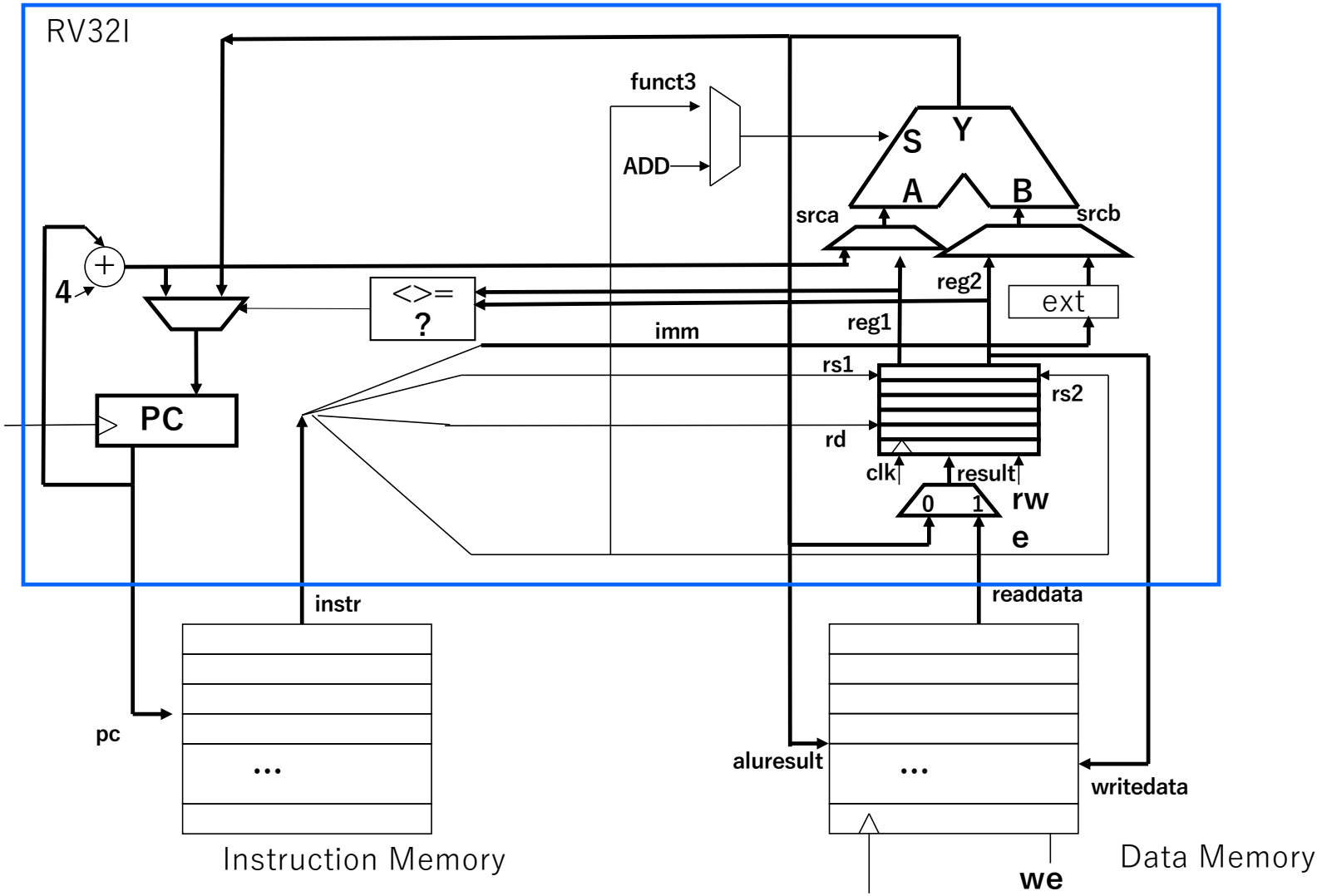
Microarchitectures

- We show three microarchitectures to students.
  - Single-cycle microarchitecture
  - Multi-cycle microarchitecture
  - 5-stage pipeline microarchitecture
  - Total structures are mostly similar.
- The datapath of R3000 is slightly complicated.
  - The role of rt must be switched.
  - ‘jal’ and ‘jalr’ of R3000 need to push PC to $31.
- The compare and branch with size instructions (‘bge’ or ‘blt’) may stretch the critical path.

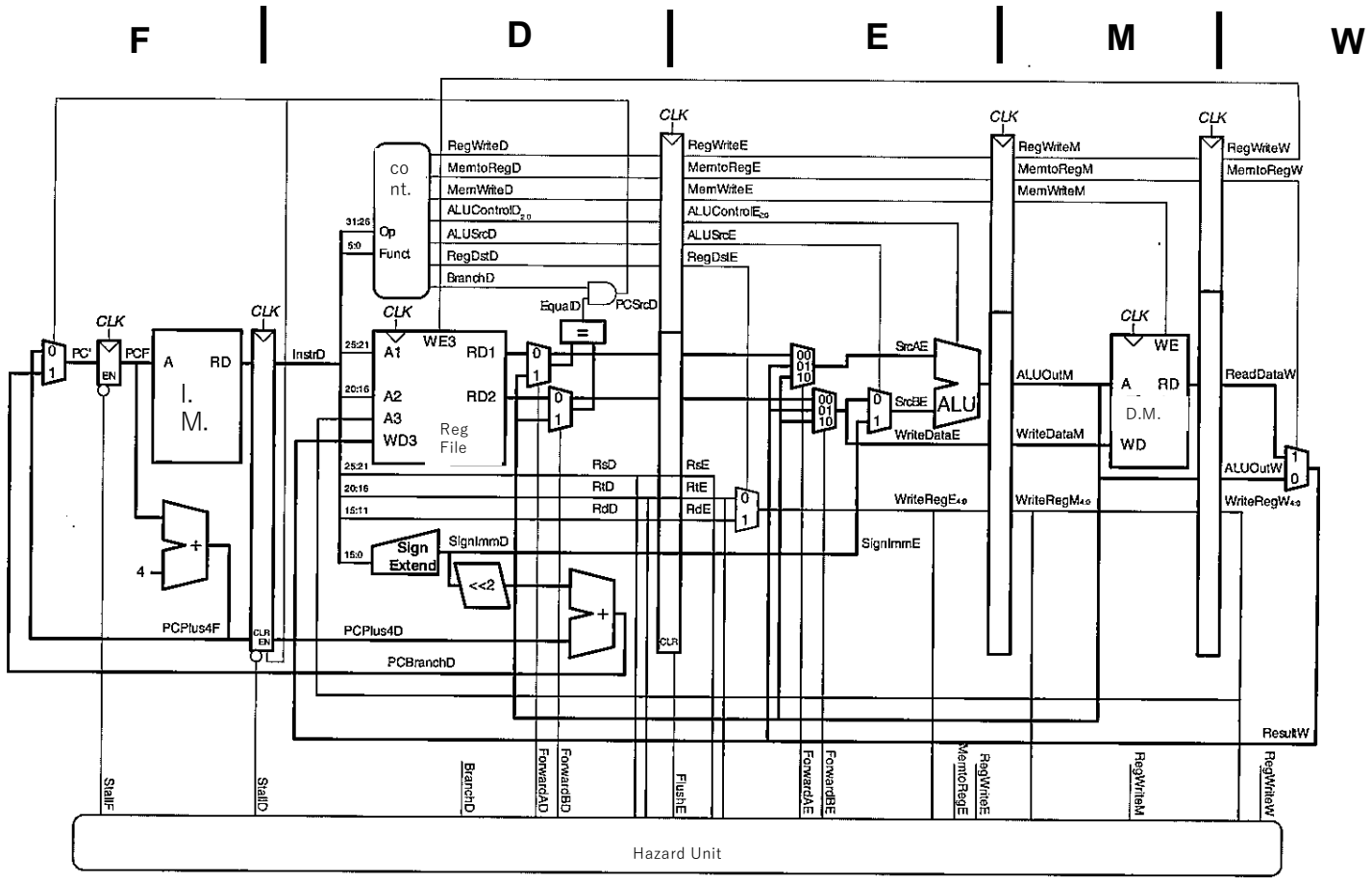
R3000 single-cycle microarchitecture



Single-cycle micro-architecture

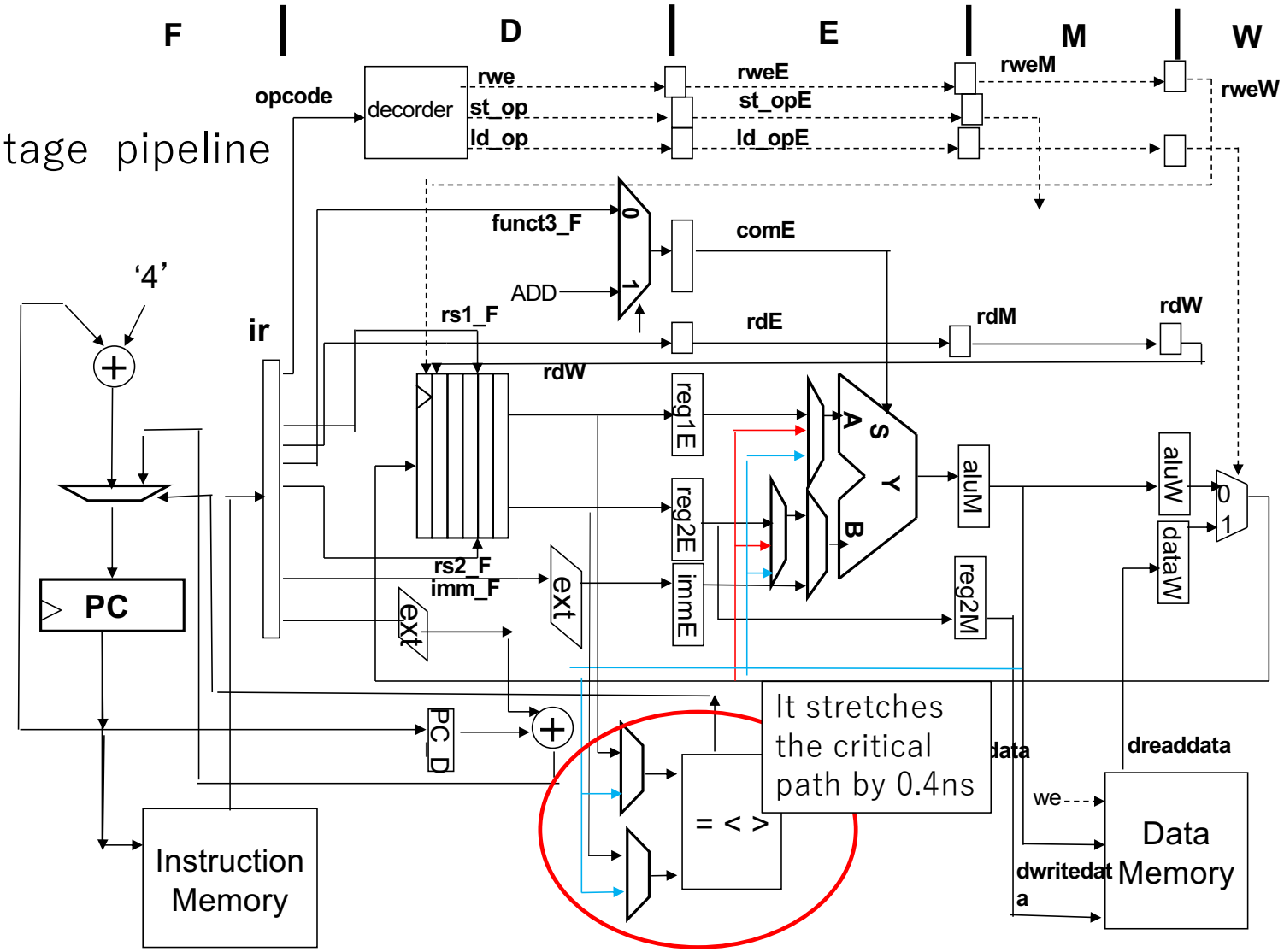


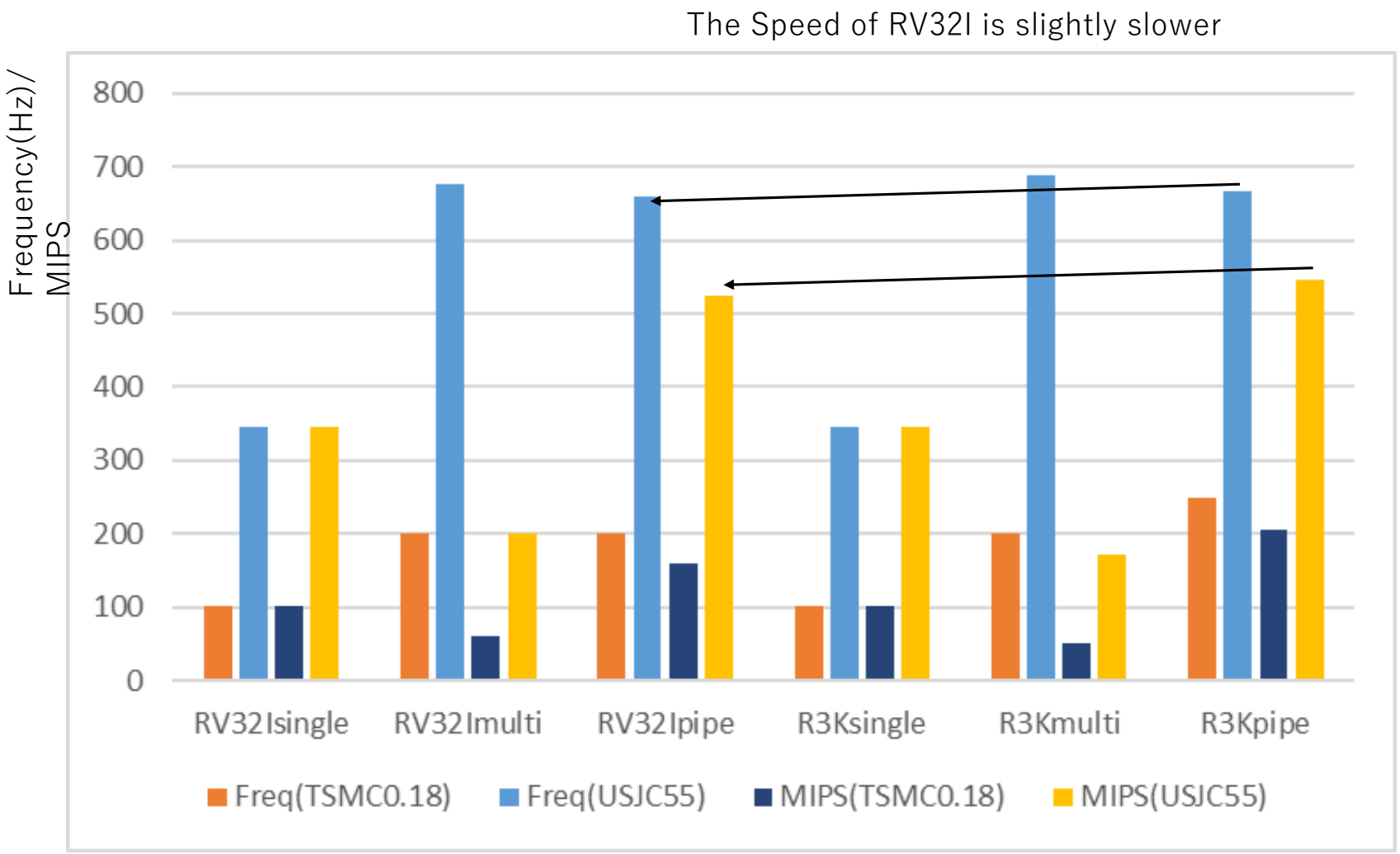
MIPS R3000 5-stage pipeline



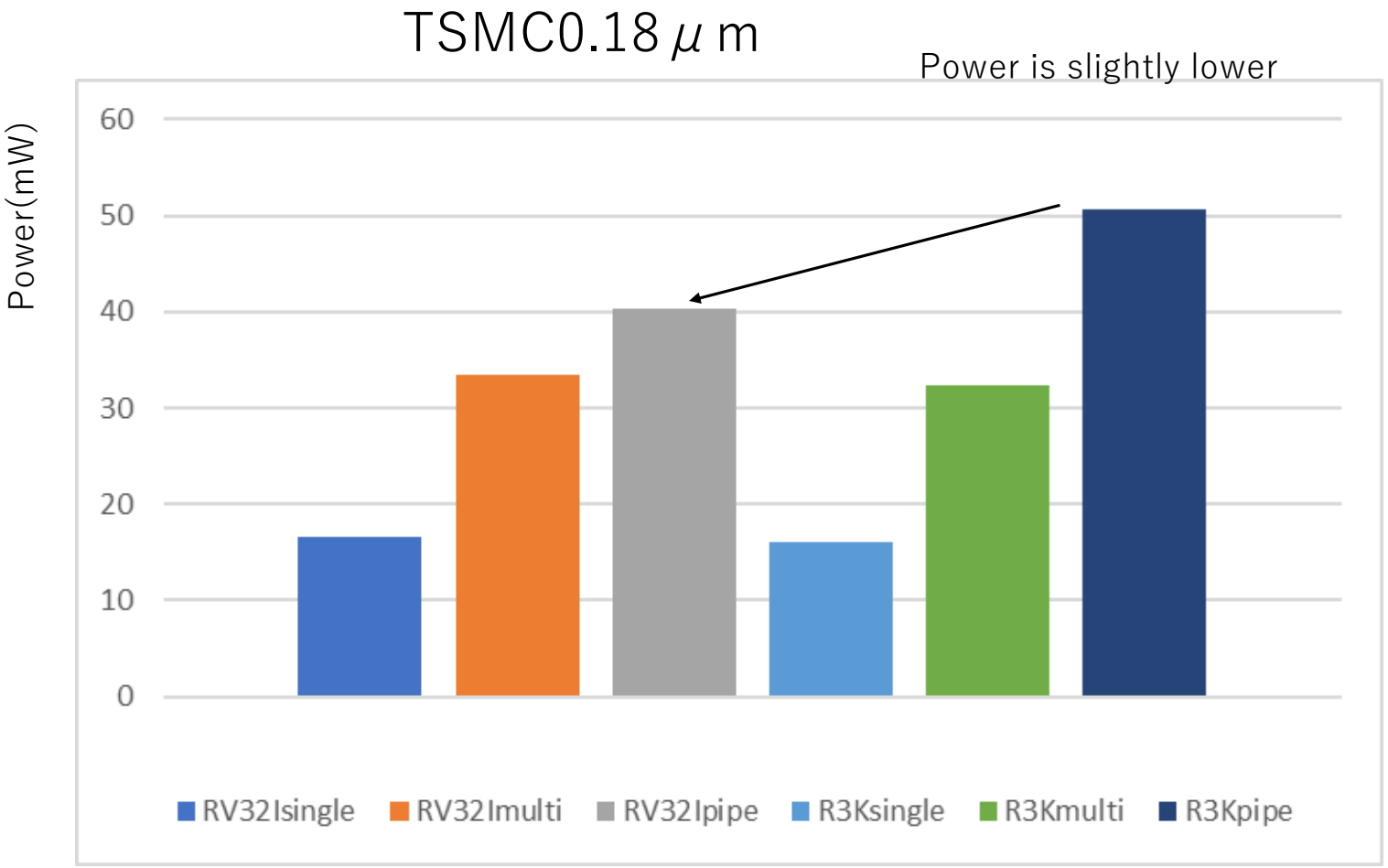
From Harris&Harris “Digital Design and Computer Architectures”

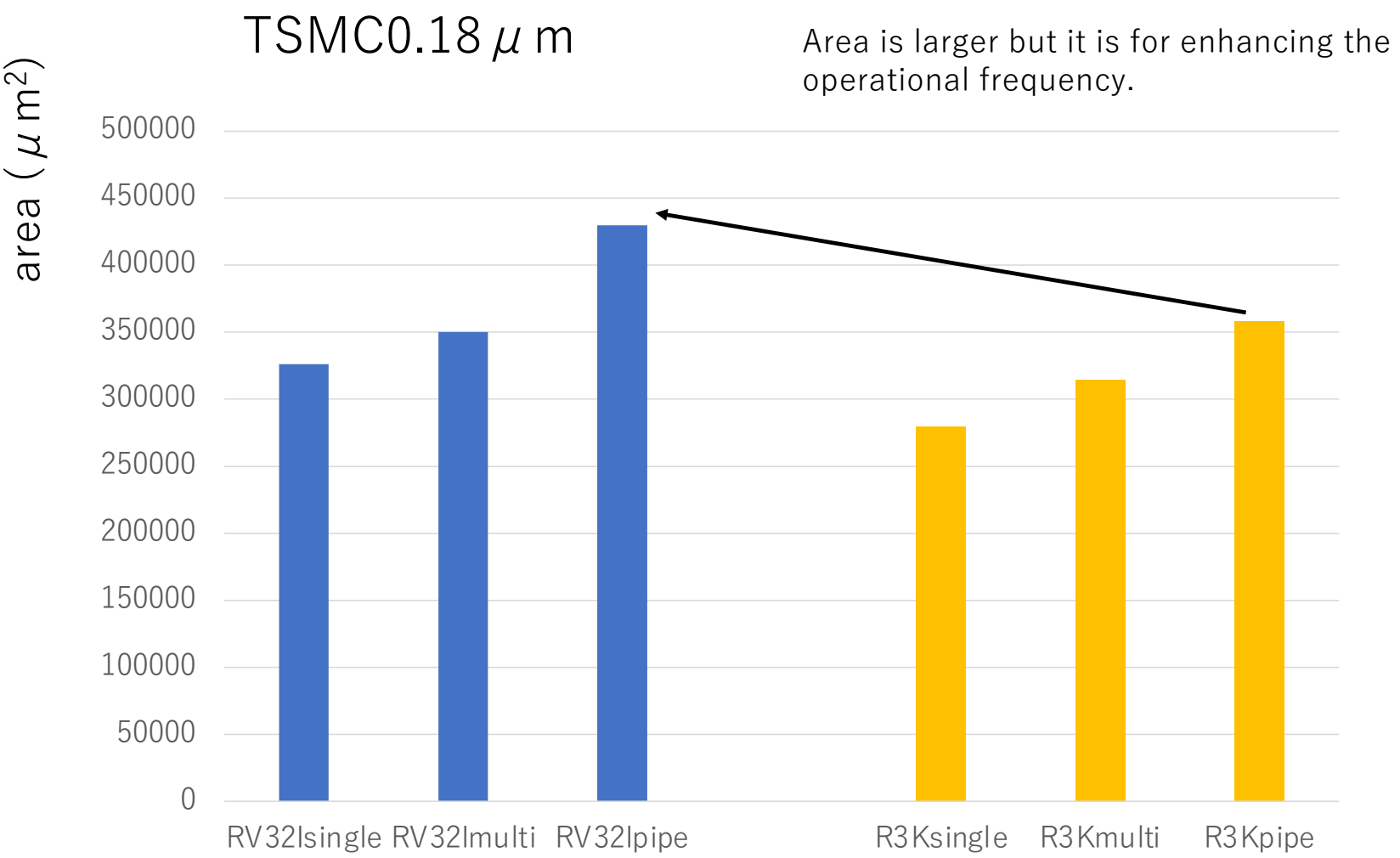
RV32I 5-stage pipeline





USJC55: United Semiconductor Japan CMOS 55nm


TSMC0.18μm
Power is slightly lower
Power(mW)
60
50
40
30
20
10
0
RV32Isingle
RV32Imulti
RV32Ipipe
R3Ksingle
R3Kmulti
R3Kpipe


TSMC0.18 μm
Area is larger but it is for enhancing the operational frequency.
area (μm²)
500000
450000
400000
350000
300000
250000
200000
150000
100000
50000
0
RV32Isingle
RV32Imulti
RV32Ipipe
R3Ksingle
R3Kmulti
R3Kpipe

RV32I vs. R3000

- Clock Frequency and Million Instructions Per Second: R3000 is slightly better.
  - bge and blt of RV32I stretch the critical path.
  - Delayed-branch of R3000 effectively works.
- Both can work at 650MHz clock when USJC55nm process is used.
  - Memory delay is not precisely cared.
- The area and power are similar.

Summary

- RV32I is a good model processor as R3000.
- The ISA and microarchitectures are mostly similar.
- The complicated bit-field slightly reduces the hardware, but it is confusing for students.
- The performance of R3000 is slightly better.
  - ‘bge’ and ‘blt’ stretch the critical path.
  - Delayed-branch of R3000 is effective.
- The benefit of RV32I is that it can be used as a base of many extensions.
  - Making understand why RV32I does not use delayed-branch is important.

- RV32I will be broadly used as a model processor for education.