国内顧客によるSiFive RISC-V 搭載チップ発表！

SiFiveの最新技術のご紹介

RISC-V Days Tokyo 2021 Spring
April 22, 2021

国内顧客によるSiFive RISC-V 搭載チップ発表！

SiFiveの最新動向・発表のご紹介

SiFiveユーザ動向：ArchiTek社がSiFive RISC-V 搭載チップ発表

2021年3月18日（木）

ArchiTekとSiFiveは、セキュリティやプライバシーを保ち柔軟にエッジAI処理を可能にするAiOnIc®プロセッサを開発

AiOnIc®
Edge AI Processor

Edge AI Processor "AiOnIc®"（アイオニック）

- Process: TSMC 12nm(N12FFC)
- Packadge: FCCSP(12mm×12mm), 484 pins, 0.5mmピッチ
- Die Size: 4.5mm×4.5mm
- Operating Voltage: 0.9V, 1.8V
- CPU: SiFive RISC-V(E34)
- SRAM: 8MB
- I/F: DDR4, Ethernet, UART, I2C, I2S, SPI, QSPI, GPIO
- Clock Freq: ～600MHz

- "aIPE" Engines
  - Digital signal processing
  - Conventional sort
  - Multi functional DMA
  - Inverse matrix operation
  - FFT
  - GPGPU
  - CV
  - Conventional multiplication addition

AiOnIc ®

独自アーキテクチャ『aIPE』を搭載した
初の自社チップ『AiOnIc ® 』のサンプルを開発

12nmプロセスの採用で小型・低消費電力を実現し
エッジAIプロセッサのデファクトを狙う

ArchiTek株式会社は、
独自アーキテクチャ『aIPE（ArchiTek Intelligence® Pixel Engine）』を搭載した
初の自社チップ『AiOnIc ® （アイオニック）』のサンプルを開発しました。
『aIPE』は世界で開発されているエッジAIプロセッサをリードする新しい構造です。
NEDO事業※１に於いて、自動運転に不可欠なSLAM※２では汎用CPUと比較して1/20の処理時間短縮、
骨格、姿勢推定を実行するOpenPose※３ではGPUと比べて約3.8倍の動作速度を実現しました。

エッジAIプロセッサ『AiOnIc』

AiOnIc ®

■アプリケーション

『AiOnIc ® 』はあらゆるセンサーのデータをエッジでリアルタイムに処理してメタデータ（言葉や数字などで表現できる小さな情報）に変換することで、セキュリティやプライバシーの問題を気にすることなく「Edge to Edge」をワンチップで実現します。

	店舗監視 AIカメラ	・監視、万引き防止 ・来客カウント ・動線解析
	見守り	・介護施設 ・託児所、保育園 ・家庭
	物流 ロボット	・搬送ロボット、AGV ・業務用車両
	ドローン	・農業など一次産業 ・計測、検査、点検
	ドラレコ 運転支援	・運転支援、危険予測 ・車内外の監視 ・運転者のモニタリング

	ＦＡ 検査装置	・検査装置 ・故障予測
	ヘルスケア	・運動量計 ・血糖モニター ・ウェアラブル端末
	医療	・病院 ・クリニック
	ＡＩ家電	・各種AI家電

SiFive collaborates with Intel Foundry Services

SiFive collaborates with new Intel Foundry Services (IFS) to enable innovative new RISC-V computing platforms

(March 25, 2021 : SiFive Blog by Patrick Little, President & CEO, SiFive)

I am excited to see Intel's new **Foundry services business** (IFS) ……We're pleased to see Intel recognize the utility and opportunity for the RISC-V instruction set architecture **in partnering to enable SiFive's industry-leading Core IP portfolio to enable a new wave of leading-edge technology. The advantages of SiFive Core IP and the newly added choice of IFS(Intel Foundry Services)'** new business services and leading-edge high-performance capabilities enable our customers to develop these next-generation computing platforms.

(March 23, 2021 : Intel CEO Pat Gelsinger Announces "IDM 2.0" Strategy for Manufacturing, Innovation and Product Leadership)

IDM 2.0 represents the combination of three components that will enable the company to drive sustained technology and product leadership:

1. **Intel's global, internal factory network for at-scale manufacturing**
2. **Expanded use of third-party foundry capacity**
3. **Building a world-class foundry business, Intel Foundry Services**

 Intel Foundry Services (IFS) will be differentiated from other foundry offerings with a world-class IP portfolio for customers, including **x86 cores as well as ARM and RISC-V ecosystem IPs.**

SiFive/OpenFive Tapes Out SoC on TSMC 5nm Technology

SiFive/OpenFive Tapes Out SoC for Advanced HPC/AI Solutions on TSMC 5nm Technology

(SAN MATEO, Calif., April 13, 2021) — OpenFive, a leading provider of customizable, silicon-focused solutions with differentiated IP, today announced the successful tape out of a high-performance SoC on TSMC's N5 process, with integrated IP solutions targeted for cutting edge High Performance Computing (HPC)/AI, networking, and storage solutions.

The SoC features an OpenFive High Bandwidth Memory (HBM3) IP subsystem and D2D I/Os, as well as a SiFive E76 32-bit CPU core. The HBM3 interface supports 7.2Gbps speeds allowing high throughput memories to feed domain-specific accelerators in compute-intensive applications including HPC, AI, Networking, and Storage. OpenFive's low-power, low-latency, and highly scalable D2D interface technology allows for expanding compute performance by connecting multiple dice together using an organic substrate or a silicon interposer in a 2.5D package.

The SiFive E7-Series is a high performance embedded 32-bit processor. The E76 configuration of the E7-Series includes SiFive Insight Trace and Debug technology, which enables core instruction trace streaming off-chip. This feature is a requirement for debugging complex real-time software stacks, as well as software verification and certification, providing software developers with deep insights into the performance and behavior of their applications.

NVIDIA、Armベースのデータセンター向けCPU「Grace」発表

（**2021年04月13日**）
米**NVIDIA**は、オンラインで開催の年次カンファレンス「**GTC 2021**」で、
同社としては初になるデータセンター向け**CPU**「**Grace**」
「複雑な**AI**と構成のコンピューティングワークロードで現在最速とされる
サーバの**10倍**の性能を提供する**Arm**ベースのプロセッサ」を発表した。

「**Arm**の技術を採用することで、**NVIDIA**は**Grace**を巨大規模の**AI**および**HPC**
専用の**CPU**として設計した。**GPU**および**DPU**（データ処理装置）と組み合わせ
ることで、**Grace**は、コンピューティングのための**3**番目の基盤テクノロジーと、
AIを進歩させるためにデータセンターを再構築する機能を提供する。**NVIDIA**は
今や、**3**つのプロセッサを提供する企業になった」と語った。
NVIDIAは昨年**9月**、英**Arm**をソフトバンクから買収することで合意した。
（まだ買収は完了していない。）

ルネサスとSiFive車載用次世代ハイエンドRISC-Vソリューションの共同開発で提携

RENESAS

SiFive

（2021年4月21日）

ルネサス エレクトロニクス株式会社とSiFive, Inc.は、このたび、車載アプリケーション向けに次世代のハイエンドRISC-Vソリューションの共同開発をするために戦略的パートナシップを締結したことを発表します。

本提携は、SiFiveがRISC-Vコア IPポートフォリオをルネサスに ライセンス供与することも含みます。

Partnership for Jointly Developing
Next-Gen Automotive RISC-V Solutions

RENESAS   SiFive

RISC-V

SiFive RISC-V Core IP Portfolio

2 Series	3/5 Series	7 Series	VI7 Series	8 Series
Power & area optimized	**Efficient performance**	**High performance**	**High performance vector**	**Maxium performance**
2– 3-stage single-issue pipeline	5– 6-stage single-issue pipeline	8-stage, dual-issue superscalar pipeline	8-stage, dual-issue with integrated vector unit	3-wide 12-stage out-of-order superscalar pipeline

U Cores

	U5 Series	U7 Series	VIU7 Series	U8 Series
64-bit application cores	Linux-capable application processors	High performance Linux-capable processors	Linux- capable vector processors	Highest performance application processors
Linux, datacenter, network baseband	› U54, U54-MC	› U74, U74-MC	› VIU75, VIU75-MC	› U84, U84-MC

S Cores

	S2 Series	S5 Series	S7 Series
64-bit embedded	Area-optimized 64-bit microcontrollers	Low-power 64-bit microcontrollers	High performance 64-bit embedded cores
Storage, AR/VR Machine learning	› S21	› S51, S54	› S76, S76-MC

E Cores

	E2 Series	E3 Series	E7 Series
32-bit embedded	Our smalles, most efficient cores	Balanced performance and efficiency	High performance 32-bit embedded cores
MCU, edge computing, AI, IOT	› E20, E21, E24	› E31, E34	› E76, E76-MC

SiFive & Renesas Joint Development Partnership

Renesas and SiFive Partner to Jointly-Develop Next-Generation High-End RISC-V Solutions for Automotive Applications

(TOKYO, Japan, and SAN MATEO, Calif., April 21, 2021)

Renesas Electronics Corporation and SiFive, Inc., today announced **a strategic partnership to jointly develop next-generation, high-end RISC-V solutions for automotive applications. The partnership will also include SiFive licensing the use of their RISC-V core IP portfolio to Renesas.**

"RISC-V is an important element in providing additional capabilities and options for new and existing customers," said Takeshi Kataoka, Senior Vice President, General Manager of Automotive Solution Business Unit at Renesas. "We are very excited to work with SiFive as their lead partner to develop next-generation semiconductor solutions through the collaboration of our accumulated expertise in the automotive field, and SiFive's high-end RISC-V technologies."

Renesas provides automotive solutions including ADAS, Autonomous Driving (AD), Electric Vehicles (EV), and Connected Gateway (CoGW) to customers all over the world by utilizing its diverse portfolio of industry-leading microcontrollers (MCUs) and system-on-chips (SoCs), as well as analog and power products. With a safe, comfortable, and environmentally-conscious society of future mobility in mind, Renesas is exploring the use of next-generation, high-performance RISC-V cores optimized for automotive applications to expand high-end SoC and MCU development capabilities to continue providing innovative and trusted automotive solutions to customers worldwide.

SiFive Intelligence : Machine Learning Solutions

SiFive Intelligence for Modern MachineLearning Architectures Presentation at Linley Spring Processor Conference on April 23

(Linley Spring Processor Conference 2021 : April 19 - 23, 2021 Virtual Event)

SiFive has gone a step further with the development of new AI-focused instructions specifically tuned for the acceleration of common machine learning processing. The presentation will demonstrate how these new instructions enable high-performance, low-power inference applications. SiFive Intelligence solutions incorporate multicore, Linux-capable, RISC-V microarchitecture processors with scalable RVV 1.0-specification vector lengths, and provide TensorFlow Lite support.

"SiFive's vision is to take a 'software-first' approach to its SiFive Intelligence products, delivering flexible acceleration strategies that scale with the evolving nature of AI," said Chris Lattner, President of Engineering and Product, SiFive. "RISC-V provides an open specification, making it easier for software to communicate with hardware and encouraging developer creativity. This is a transformative moment, as SiFive expands its presence in the AI space with SiFive Intelligence platforms for the next generation of automotive, mobile, IoT, 5G networking, and data center computing solutions."

SiFiveの最新技術のご紹介

SiFive IP Offerings

RISC-V Core IP

U Cores

64-bit Application Processors

S Cores

64-bit Embedded Processors

E Cores

32-bit Embedded Processors

SoC IP

Memory Interface IP Subsystems

HBM2
HBM2E

Connectivity IP

Interlaken
Ethernet
USB

System & Peripheral IP

DMA
SPI & more...

Trace and Debug

SiFive Insight

Security IP

SiFive Shield

SiFive IP Offerings

RISC-V Core IP

U Cores

64-bit Application Processors

S Cores

64-bit Embedded Processors

E Cores

32-bit Embedded Processors

SoC IP

Memory Interface IP Subsystems

HBM2
HBM2E

Connectivity IP

Interlaken
Ethernet
USB

System & Peripheral IP

DMA
SPI & more...

Trace and Debug

SiFive Insight

Security IP

SiFive Shield

SiFive RISC-V Core IP Portfolio

	2 Series	3/5 Series	7 Series	VI7 Series	8 Series
	Power & area optimized 2– 3-stage single-issue pipeline	**Efficient performance** 5– 6-stage single-issue pipeline	**High performance** 8-stage, dual-issue superscalar pipeline	**High performance vector** 8-stage, dual-issue with integrated vector unit	**Maxium performance** 3-wide 12-stage out-of-order superscalar pipeline

U Cores

64-bit application cores
Linux, datacenter, network baseband

U5 Series	U7 Series	VIU7 Series	U8 Series
Linux-capable application processors	High performance Linux-capable processors	Linux- capable vector processors	Highest performance application processors
> U54, U54-MC	> U74, U74-MC	> VIU75, VIU75-MC	> U84, U84-MC

S Cores

64-bit embedded
Storage, AR/VR
Machine learning

S2 Series	S5 Series	S7 Series
Area-optimized 64-bit microcontrollers	Low-power 64-bit microcontrollers	High performance 64-bit embedded cores
> S21	> S51, S54	> S76, S76-MC

E Cores

32-bit embedded
MCU, edge computing, AI, IOT

E2 Series	E3 Series	E7 Series
Our smalles, most efficient cores	Balanced performance and efficiency	High performance 32-bit embedded cores
> E20, E21, E24	> E31, E34	> E76, E76-MC

SiFive Core Designer

Optimize SiFive RISC-V Core IP for Your Application

- SiFive Core Designer enables configuration of SiFive RISC-V Core IP through an easy to use Web Portal

- **Variants** are generated with click of a button and are available from the Workspace

- **Variants** contain
  - RTL matching the configuration, including a testbench and other collateral needed to realize the design
  - Documentation specific to the design
  - Customized bare-metal BSP for easy integration into SiFive's SDKs
  - FPGA bitstreams for common FPGA development boards for easy software benchmarking of the RC

SiFive Core Designer: web-based, simple and easy

SiFive.com

Silicon at the speed of software.
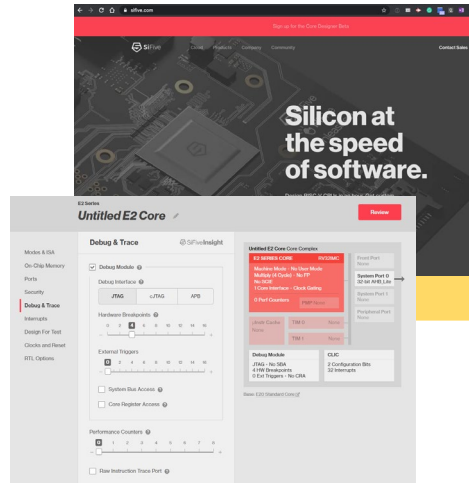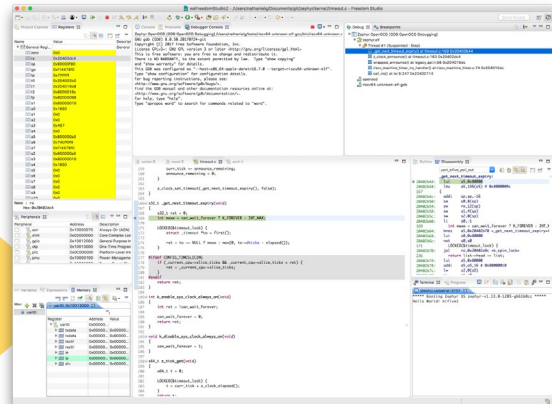
SiFive Core Designer
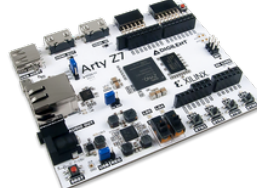
Core tarball built and generated for your SCD account within hours

Workspace

Freedom Studio
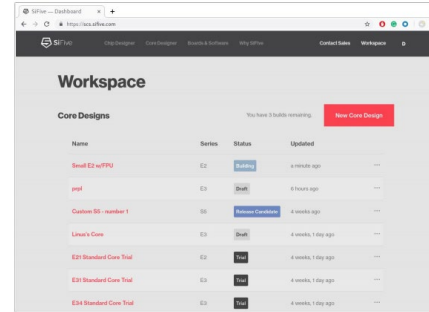
Freedom Tools

Freedom E SDK

SystemC Models

Instruction Set Simulator (ISS) - QEMU

RTL, FPGA Bit Streams

Previous Releases

Power Improvements	Performance Improvements	Area Improvements
up to *25%*	up to *2.8x*	up to *11%*

21G1 Release

- Up to 25% smaller code size
- 35% increase performance for Bit Processing
- Half Precision Floating Point for AI/IoT application
- Optimized SoC integration

U Cores

S Cores

E Cores

The New Generation of Processor

Flexibility in SoC Integration

SiFive Shield™ Security

SiFive Insight™ Accessibility

SiFive Freedom Studio, Software Development

Benefits of the 21G1 Release

Up to 25% Smaller Code size from Improved C-Library, Compiler, toolchain

- Smaller memory footprint, lower cost, lower power consumption
- Fewer cycles required for algorithm computation, lower energy consumption

Bit Manipulation package support (Zba, Zbb)

- AI, IoT, Sensor Fusion, Networking, Data compression, Encryption applications accelerated

## Half Precision data type support

- Acceleration, support for AI algorithms

SoC Integration / Memory SubSystem Greatly Improved

- Flexibility in memory map, to allow ease of integration of SiFive processors into pre-existing SoC / Memory maps
- Flexibility in reset schemes for wide range of SoCs
- Virtual addressing schemes to allow SiFive processors implementation in variety of systems
- Broader range of SRAM / Peripheral connectivity to processor allowing better trade offs in terms of software / hardware computation
- Larger number of Processor interfaces allowing more choices of SoC connectivity to balance bandwidth and computation capability

Migrating to RISC-V while maintaining TrustZone compatibility

Armv8 TrustZone architecture
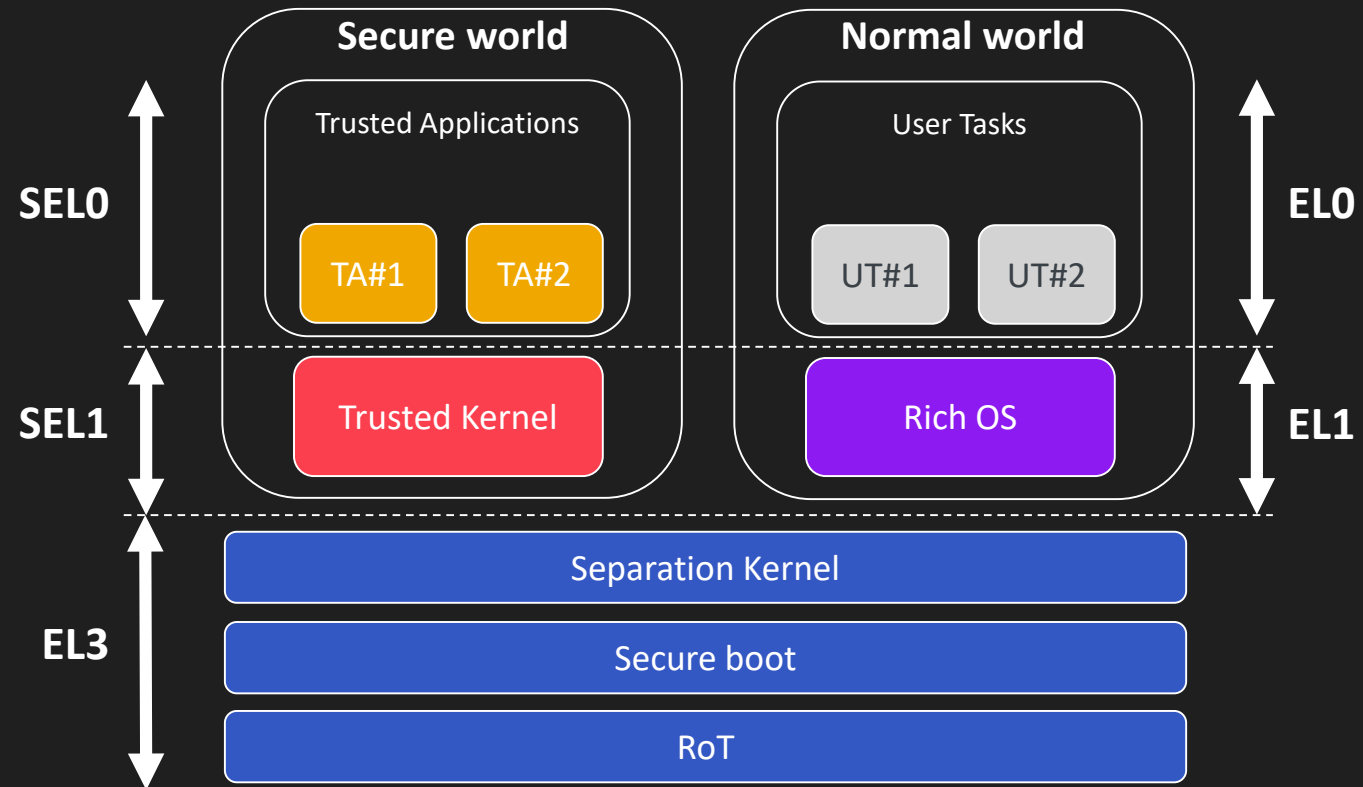
Emulating TrustZone on RISC-V

	Armv8 TrustZone		
	EL	**NS**	**Mode**
Untrusted App #2	EL0	Non Secure	User
Untrusted App #1		Non Secure	User
Rich OS	EL1	Non Secure	Supervisor
Trusted App #2	SEL0	Secure	User
Trusted App #1		Secure	User
Trusted Kernel	SEL1	Secure	Supervisor
Separation Kernel	EL3	Secure	Monitor
RoT/Secure Boot		Secure	Monitor

RISC-V®
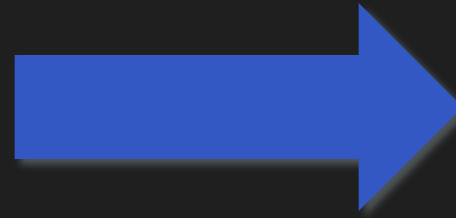
Name	Abbreviation
User	U
Supervisor	S
Hypervisor	H
Machine	M

SiFive WorldGuard

An Open Fine-Grain Security Model for Isolated Code & Data Protection

Multi-Domain Security Model with Fine Grain Control

SoC Level Information Control with Hardware Isolation

Data Protection For Cores, Caches, Interconnects, Peripherals and Memories

WorldGuard, a hardware enforced multi-domain architecture
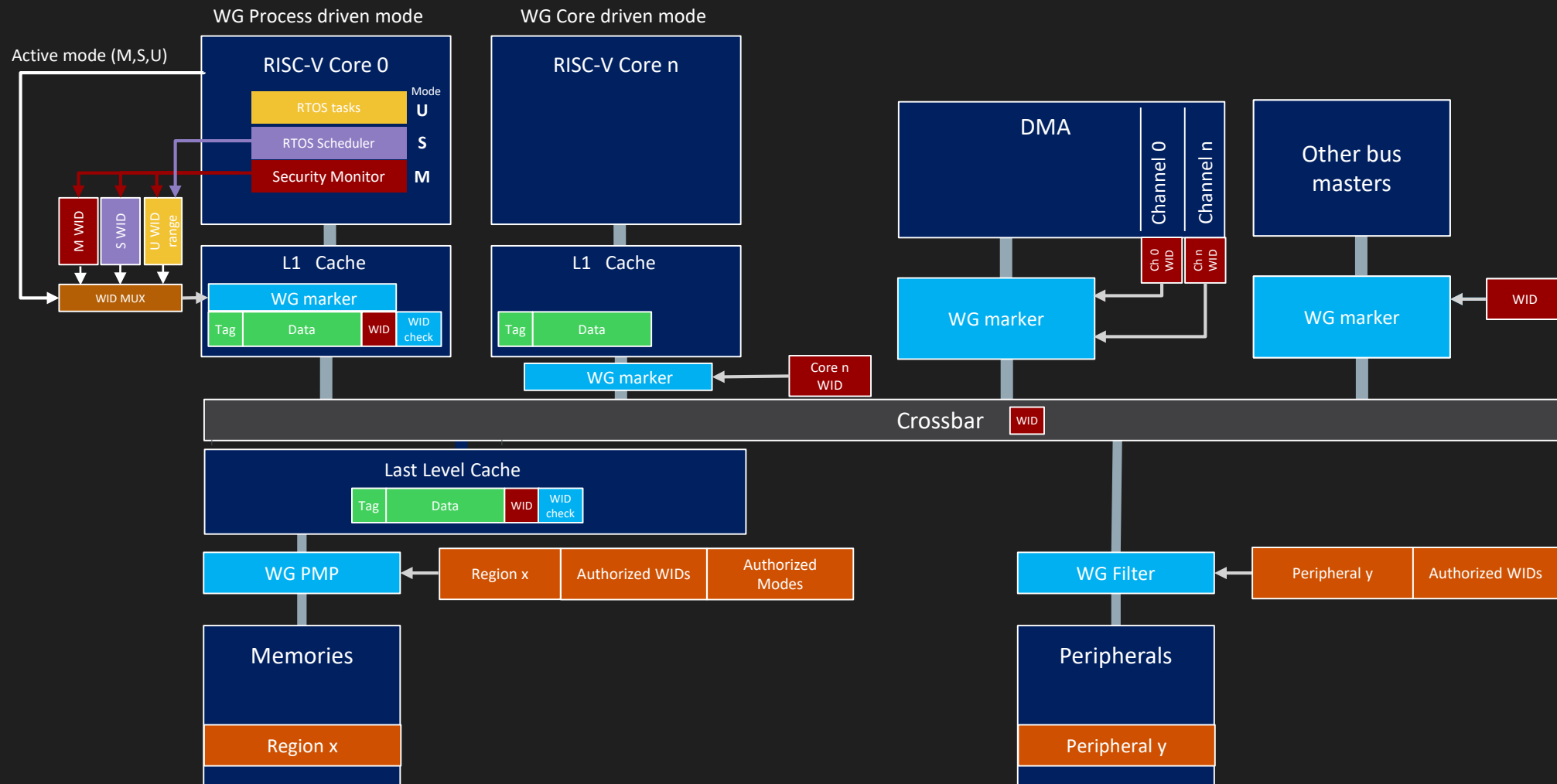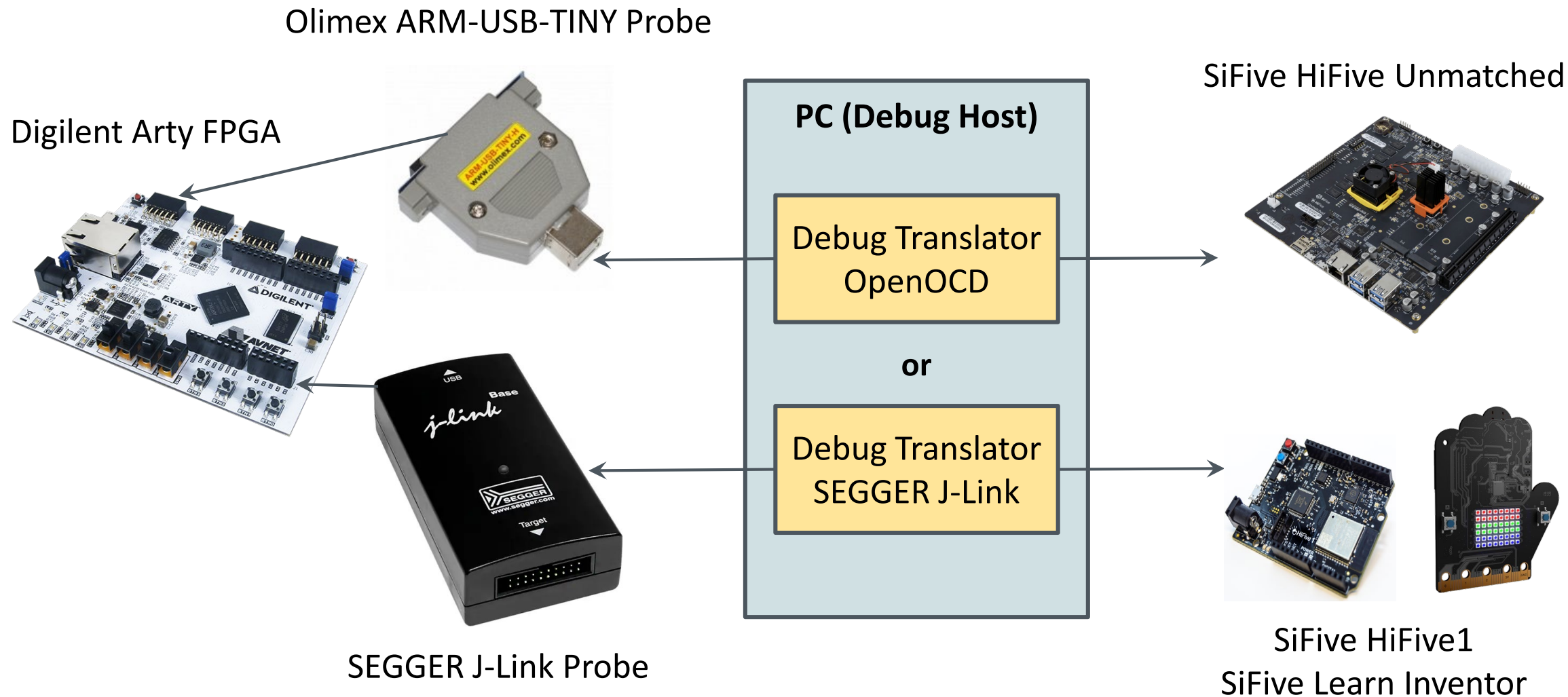
Emulating TrustZone with WorldGuard

	Armv8 TrustZone			WorldGuard	
	EL	NS	Mode	WID	Mode
Untrusted App #2	EL0	Non Secure	User	7	U
Untrusted App #1		Non Secure	User	6	U
Rich OS	EL1	Non Secure	Supervisor	5	S
Trusted App #2	SEL0	Secure	User	4	U
Trusted App #1		Secure	User	3	U
Trusted Kernel	SEL1	Secure	Supervisor	2	S
Separation Kernel	EL3	Secure	Monitor	1	M
RoT/Secure Boot		Secure	Monitor	0	M

SiFive Silicon and Development Platforms

Olimex ARM-USB-TINY Probe

Digilent Arty FPGA

SiFive HiFive Unmatched

PC (Debug Host)

Debug Translator OpenOCD

or

Debug Translator SEGGER J-Link

SEGGER J-Link Probe

SiFive HiFive1
SiFive Learn Inventor

HiFive Unmatched

## The World's Fastest Native RISC-V Development Platform
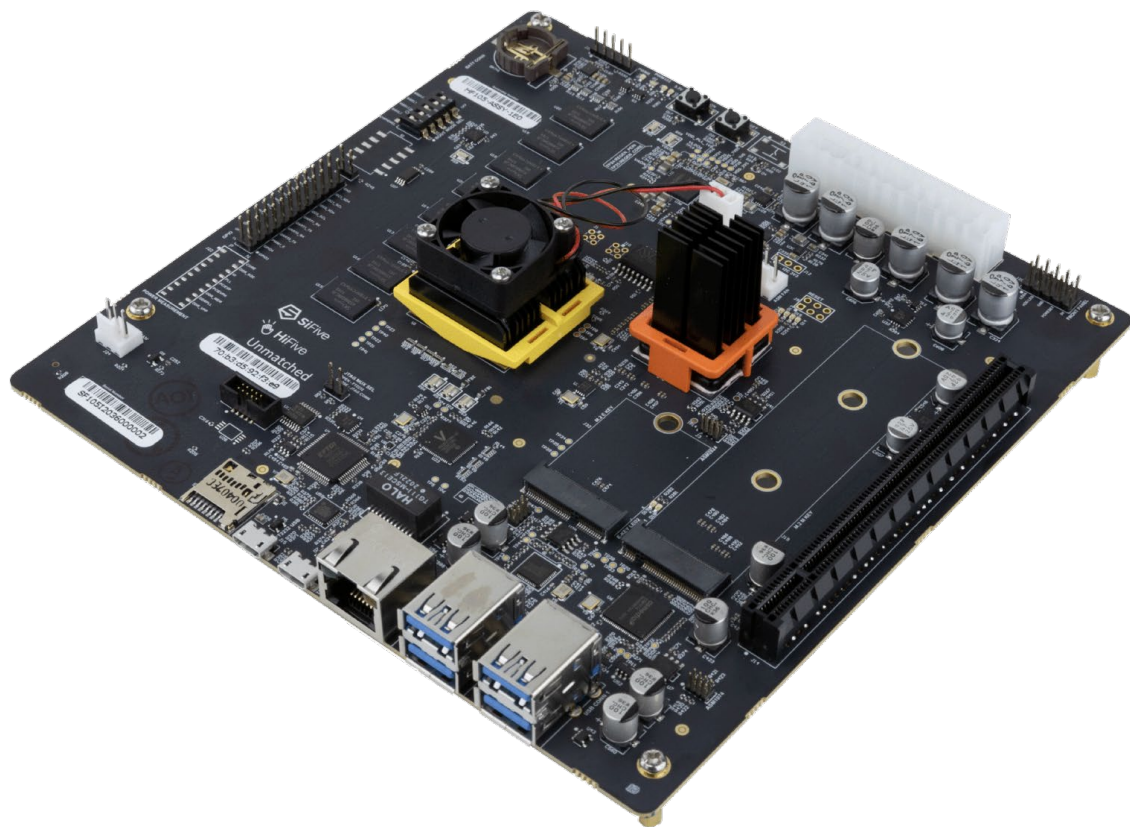
- SiFive FU740 Processor
  - SiFive 7-Series 64-bit RISC-V Core Complex
  - 4x U74-MC & 1 S7 Core
  - 2MB L2 Cache
- 16GB DDR4 Memory
- 32 MB SPI FLASH
- 4x USB 3.2 Gen 1 Ports
- MicroUSB Console Connection
- Mini-ITX PC Form Factor with ATX 24-pin Power Supply Connector
- X16 PCIe® Expansion Slot
- (PCIe Gen 3 x8)
- NVME M.2 2280 (PCIe® Gen 3 x4)
- MicroSD Card Slot
- Gigabit Ethernet
- M.2 Key E Wi-Fi/Bluetooth

SiFive

Freedom Studio

Eclipse C/C++ Development Environment

- SiFive RISC-V Cross Compiler
- SiFive OpenOCD Debugger
- SEGGER J-LINK Debugger
- SiFive QEMU emulator
- SiFive Freedom E SDK software
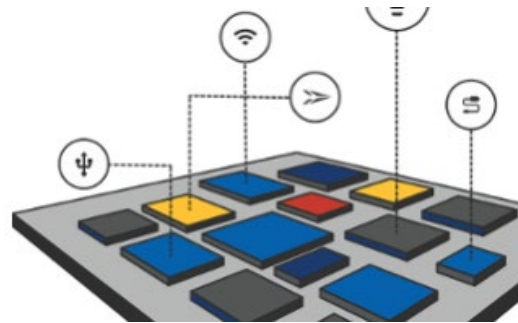
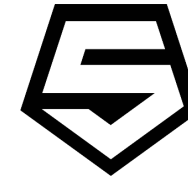## Freedom Tools

RISC-V development tools

- GNU Newlib Toolchain
- OpenOCD
- QEMU
- SDK Utilities
- Trace Decoder
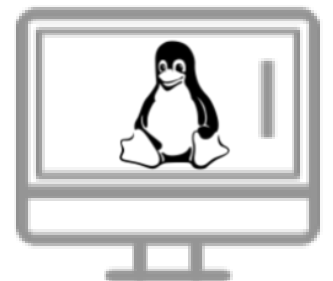- XC3SPROG

Freedom E SDK

Bare metal software development

- Example programs
- Industry standard benchmarks
- Board support
- Metal library

> make

Freedom U SDK

Embedded Linux software development

- Yocto / OpenEmbedded
- Board support
- Bootloaders
- Device tree binary
- Linux kernel images
- Disk images

Build and Run the Software

- File - Import - DevKit Examples - Browse

- Select the zip that matches your core

- Select the desired examples and click Finish

- Control-B will build the entire workspace

- Run - Debug - OpenOCD starts a JTAG Debug Session and Loads the program
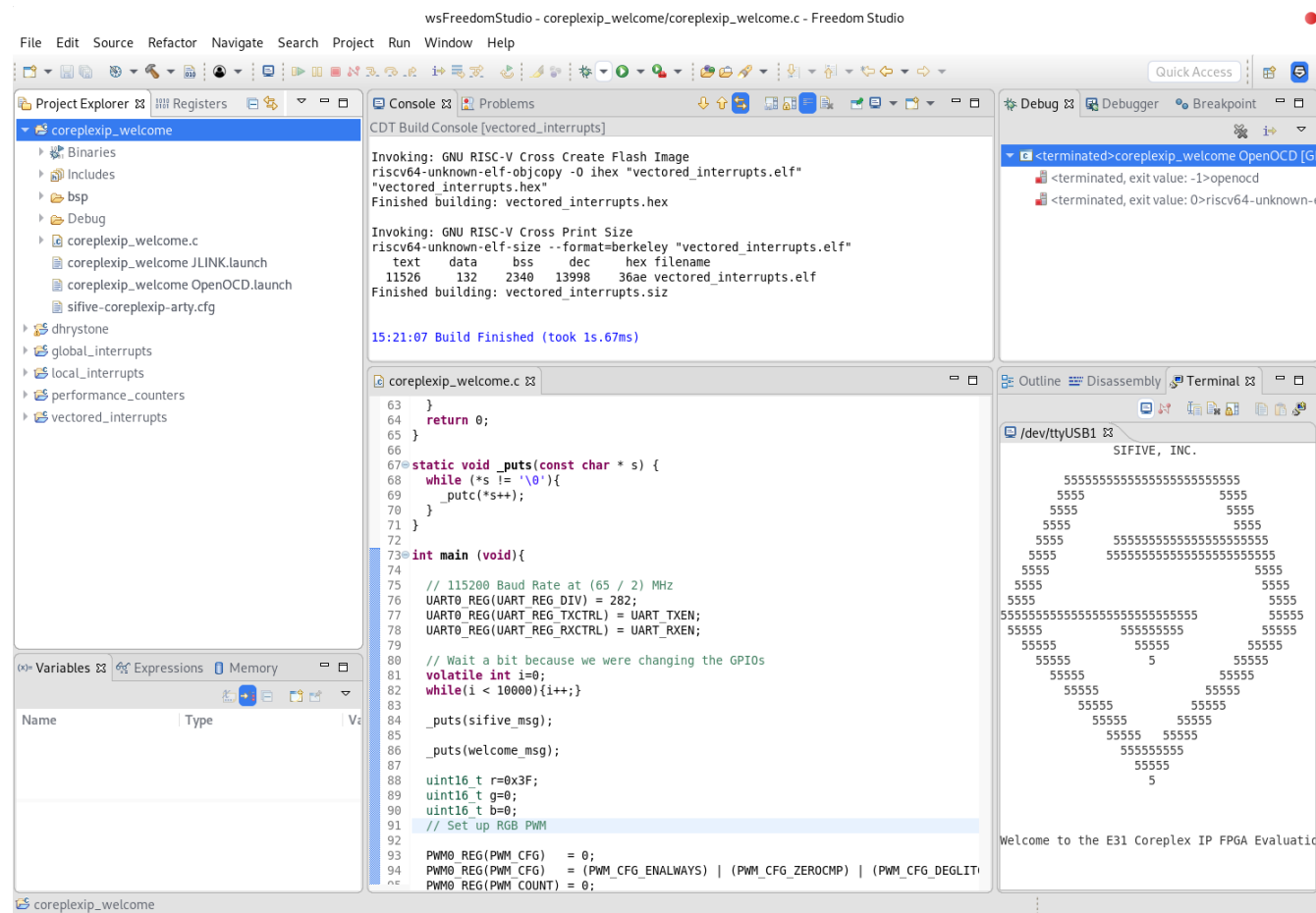
SiFive RISC-V Embedded Software Ecosystem
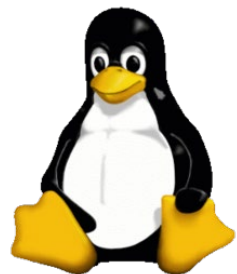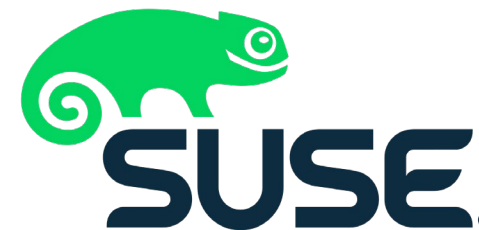
Open source solutions

Commercial solutions

さいごに

弊社バーチャルブースに是非お立ち寄りください

SiFive社各プロダクトに関する
　お問い合わせ、および、サポートは以下の窓口にて承ります
ご連絡をお待ちしております

DTS インサイト

株式会社ＤＴＳインサイト LSI Design Service部

お問い合わせ窓口： **info-sifive@dts-insight.co.jp**
サポート窓口： **support-sifive@dts-insight.co.jp**