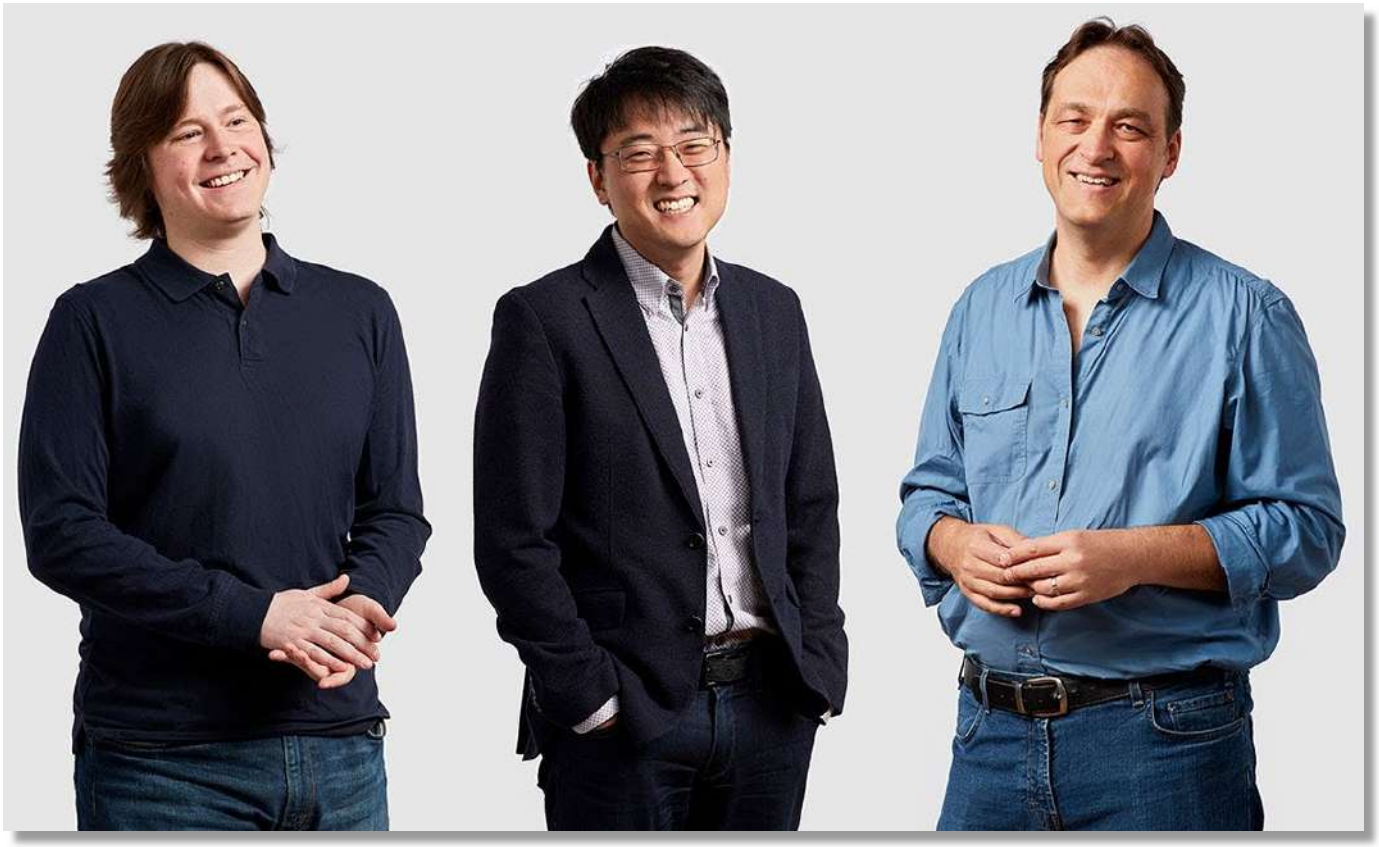
SiFive Overview

17th Nov, 2021

Leading the RISC-V Revolution



We invented RISC-V

SiFive's founders are the same
UC Berkeley professor and PhDs
who invented and have been leading the
commercialization of the RISC-V Instruction Set
Architecture (ISA) since 2010

2018, 2019, 2020: SiFive Recognized as
Most Respected Private Semiconductor Company

RISC-V International now > more than 700 members.

RISC-V

Free, open, extensible ISA for all computing devices

RISC-V International Japan members

SiFive

CPSEC
Cyber Physical Security Research Center

DTS INSIGHT

UNO Lab., Ltd.

NSI-TEXE

SONY

TechanaLye

SHC
SH CONSULTING

HITACHI
Inspire the Next

PEZY Computing

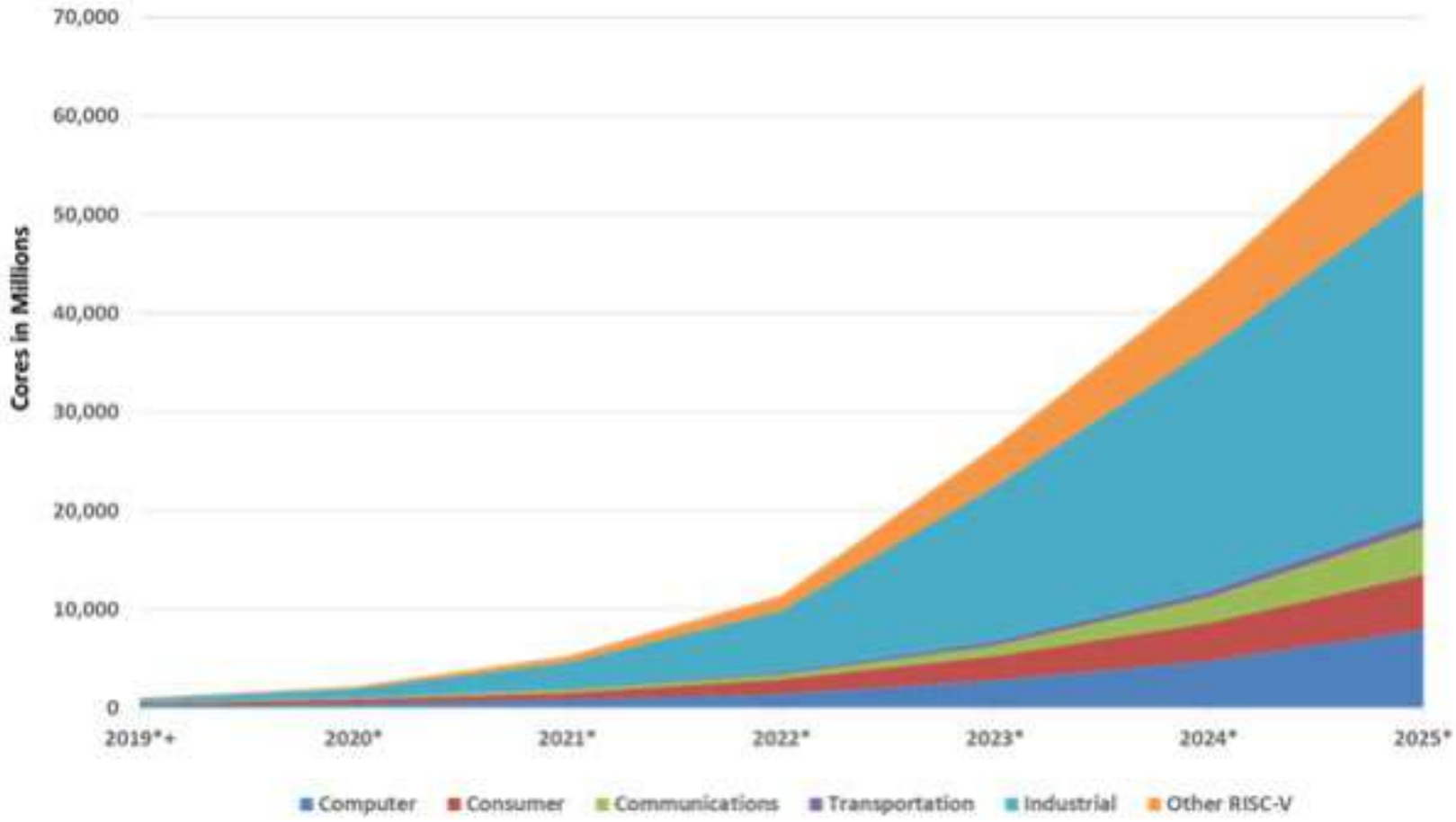
東京大学
THE UNIVERSITY OF TOKYO

UEC TOKYO

University of Electro-Communications

RISC-V Market Forecast

"Based on the already sizeable adoption of RISC-V, we forecast that the market will consume a total of 62.4 billion RISC-V cores by 2025," Semico Research



Projected CAGR 146.2%

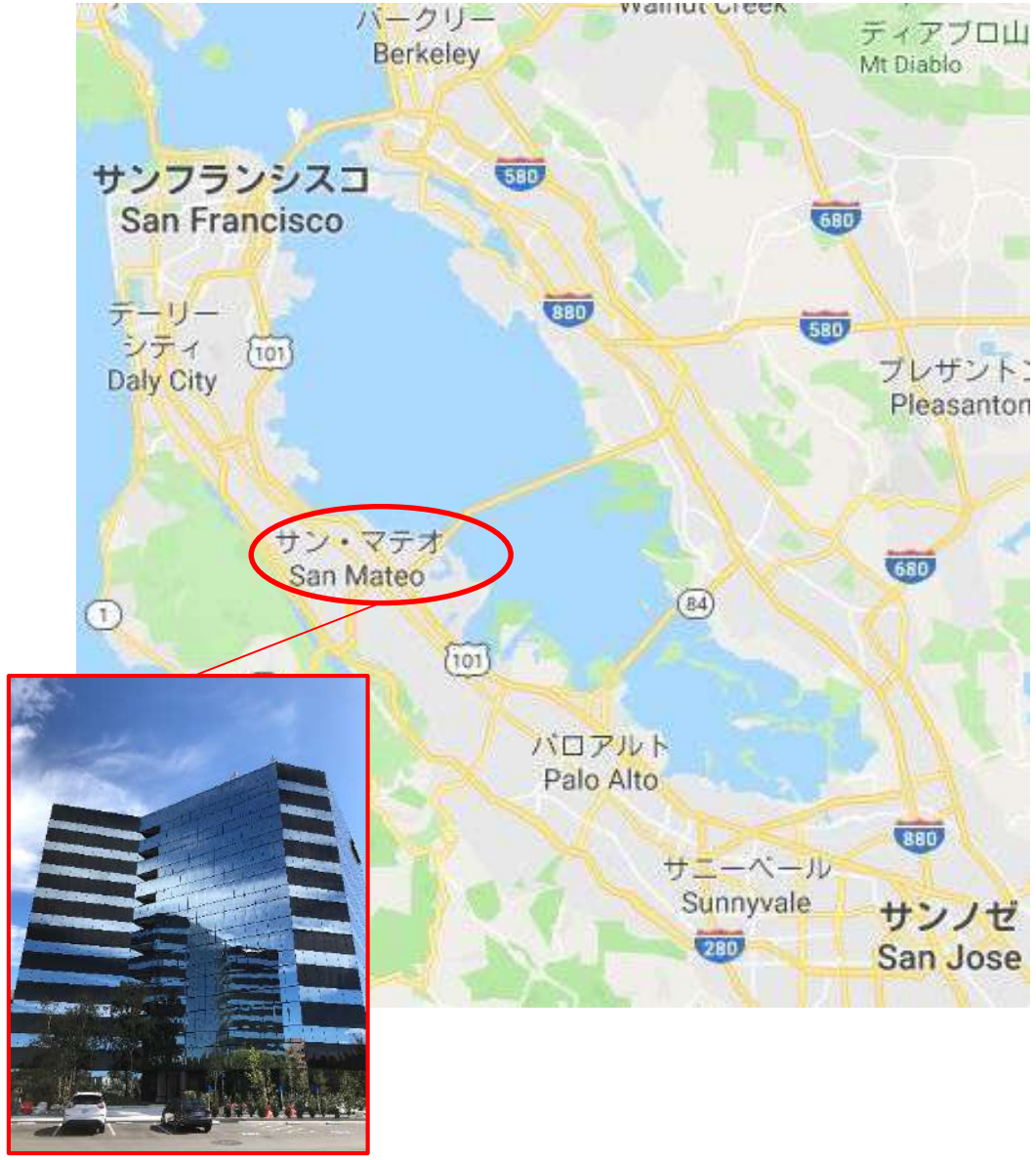
Source: Semico Research Corp.

RISC-V growing exponentially

"Based on the already sizeable adoption of RISC-V, we forecast that the market will consume a total of 62.4 billion RISC-V cores by 2025"

- Semico Research

SiFive社概要



会社概要

- 創業：2015年
- 本社所在地：San Mateo, California, USA

特徴

- RISC-V生みの親が設立
- RISC-V業界団体（RISC-V Foundation）の牽引会社
- 業界で最初にRISC-V ASICチップと評価ボードをリリース

投資状況

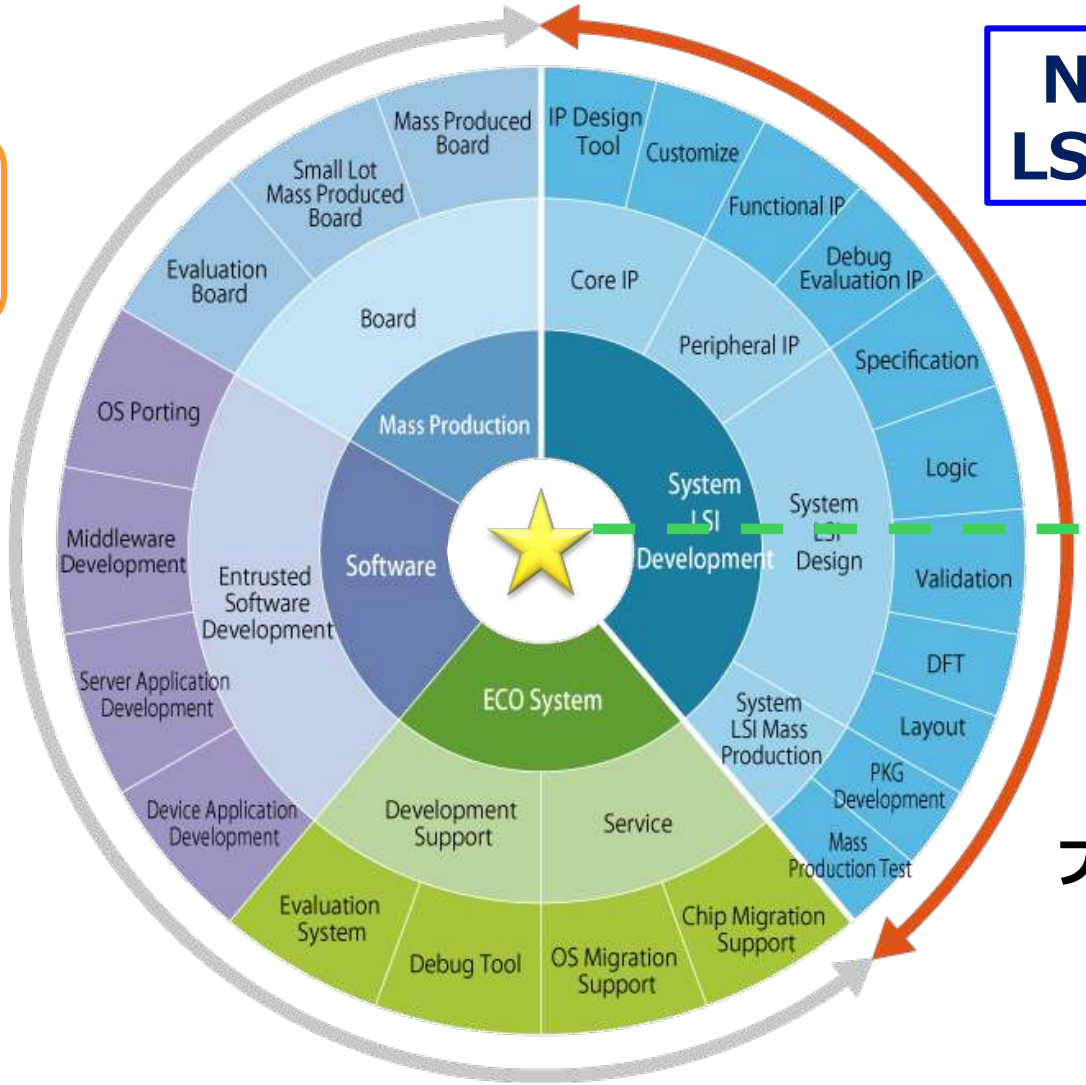
- 投資ステージ： シリーズE(2020/8), 約205億円
- 主な投資会社
  - 半導体会社
    - Intel, Qualcomm, Western Digital, SK telecom
  - ベンチャーキャピタル
    - Spark Capital, Sutter Hill Ventures
    - Osage University partners
    - Chengwei Capital

SiFive社日本国内代理店 DTSインサイトが目指すビジネス領域

ハードウェア/ファームウェア組込などの得意領域を活かし、
お客様のあらゆるニーズにお応えする**One Stop Solution**をご提案いたします

Mainstream
組込みSW開発

- 組込みソフトウェア開発
- ハードウェア開発
  - （回路設計、PCB設計、機構・筐体設計から試作製造、量産）
- デバッガ(ICEなど)
- データモニターツール
- 動的テスト/解析ツール
- ソフトウェア構造分析ツール
- トレーサビリティ管理ツール



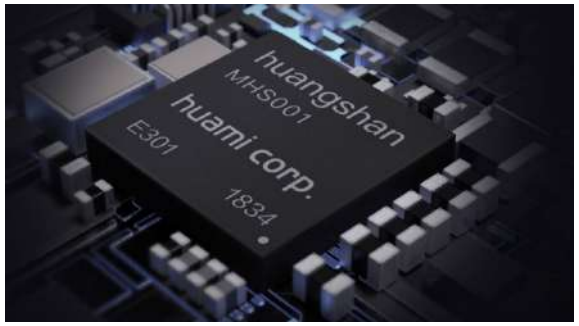
New Business
LSIデザインサービス

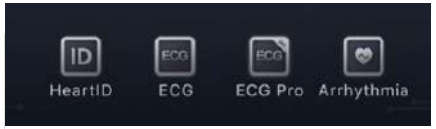
- **LSIデザインサービス**
  - **株式会社SSC様と協業**
- **RISC-V開発ボード環境**
- **RISC-Vデバッガ**
- **FW移行サービス**

プロセッサIP（RISC-V）
を題材にスタート

Products Powered by SiFive Cores (Few Examples)

Wearable SoC Huangshan-1





huami

NVMe SSD Controller FC3081

FADU

PolarFire SoC Icicle Kit

MICROCHIP

Rapid adoption of SiFive Core IP from the Edge to the Core

Products Powered by SiFive Cores (Few Examples)

Cayenne family USB-C video interface

Synaptics®

TERALYNX Ethernet Switch Silicon

Innovium®

Acquired by MARVELL™

HyperX memory network processor

Coherent Logix™

Products Powered by SiFive Cores (Few Examples)

AiOnIc®
Edge AI Processor

ArchiTek

Edge AI Processor “AiOnIc®”

- Process: TSMC 12nm(N12FFC)
- Packadge: FCCSP(12mm×12mm), 484 pins, 0.5mmピッチ
- Die Size: 4.5mm×4.5mm
- Operating Voltage: 0.9V, 1.8V
- CPU: SiFive RISC-V(E34)
- SRAM: 8MB
- I/F: DDR4, Ethernet, UART, I2C, I2S, SPI, QSPI, GPIO
- Clock Freq: ～600MHz

- “aIPE” Engines
  - Digital signal processing
  - Conventional sort
  - Multi functional DMA
  - Inverse matrix operation
  - FFT
  - GPGPU
  - CV
  - Conventional multiplication addition

RISC-V Momentum

ANANDTECH

Home > CPUs

Samsung to Use SiFive RISC-V Cores for SoCs, Automotive, 5G Applications

by Anton Shilov on December 12, 2019 11:00 AM EST

18 Comments | Add A Comment

golem.de
IT-NEWS FÜR PROFIS

SMARTPHONES

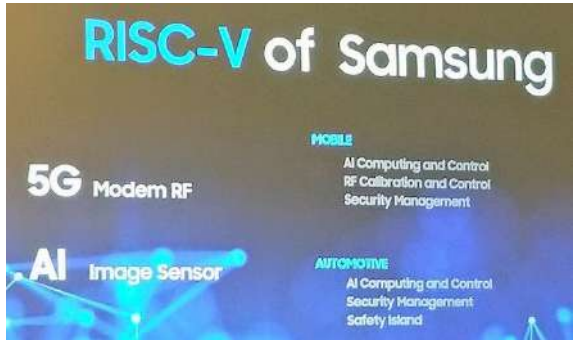
Qualcomm uses RISC-V in Snapdragon chips

One of the largest SoC developers is now relying on RISC-V : Qualcomm integrates cores with the open instruction set architecture for embedded use in current and future Snapdragon chips.

January 24, 2020, 3:12 p.m., Marc Sauter

腾讯网

New H3C Semiconductor successfully adopts RISC-V U7 multi-core processor from Saifang Technology



Leaders adopting SiFive Processors

"We're excited to partner with SiFive because of their ability to deliver CPUs and software for the modern RISC-V ecosystem."

- **Jim Keller**, President and CTO, Tenstorrent

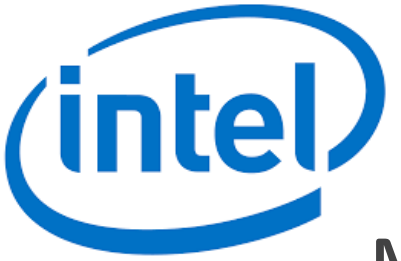
"We are very excited to work with SiFive as their lead partner to develop next-generation semiconductor solutions through the collaboration of our accumulated expertise in the automotive field, and SiFive's high-end RISC-V technologies."

- **Takeshi Kataoka**, Senior Vice President, General Manager,
Automotive Solution Business Unit, Renesas

"We are pleased to work with SiFive to accelerate our customers' AI / ML custom SoC design, illustrating the innovation potential we can achieve together."

- **Mijung Noh**, VP, Foundry Design Service Team
Samsung Electronics

Foundry collaboration



March 23, 2021

SiFive collaborates with new Intel Foundry Services to enable innovative new RISC-V computing platforms

Intel would include P550 cores on its 7nm Horse Creek chip set which is something intel will make available for RISC-V software development to show to developers and manufacturers.

April 29, 2021

SiFive and Samsung Foundry Extend Partnership to Accelerate AI SoC Development, resulting in an AI accelerator SoC tape out on Samsung 2nd generation 14LPP FinFET technology(Microsoft Zipline)

ルネサスとSiFive車載用次世代ハイエンドRISC-Vソリューションの共同開発で提携

（2021年4月21日）

ルネサス エレクトロニクス株式会社とSiFive, Inc.は、このたび、車載アプリケーション向けに次世代のハイエンドRISC-Vソリューションの共同開発をするために戦略的パートナシップを締結したことを発表します。

本提携は、SiFiveがRISC-VコアIPポートフォリオをルネサスにライセンス供与することも含みます。

SiFive

RISC-V at Scale:
An Architecture for the Future of Computing

Shubu Mukherjee
Vice President of Architecture, SiFive

shubu.mukherjee@sifive.com
@ssmukh

The Linley Group

SiFive RISC-V Processor IP Portfolio

SiFive Essential

	2-Series	3/5-Series	7-Series
	Power & area optimized 2-3 stage single-issue	Efficient performance 5-6 stage single-issue	High performance 8 stage superscalar
U Cores 64-bit application Linux, datacenter, network baseband		**U5-Series** Linux-capable application processors > U54, U54-MC	**U7-Series** High performance Linux-capable > U74, U74-MC
S Cores 64-bit embedded Storage, AR/VR, Realtime	**S2-Series** Area-optimized 64-bit microcontrollers > S21	**S5-Series** Low-power 64-bit microcontrollers > S51, S54	**S7-Series** High performance 64-bit embedded > S76, S76-MC
E Cores 32-bit embedded MCU, edge computing, AI, IOT	**E2-Series** Our smallest, most efficient cores > E20, E21, E24	**E3-Series** Balanced performance and efficiency > E31, E34	**E7-Series** High performance 32-bit embedded > E76, E76-MC

SiFive Performance

P200-Series	P500-Series
Efficient performance Integrated Vectors	Maximum performance 3-wide OoO Superscalar
P270 Efficient Performance Vector Application Core	**P550** Highest Performance Application Core

SiFive Intelligence

X200-Series
AI Accelerated Processor
SW + HW Solutions

X280
Scalable, Programmable Edge Training AI/ML
> X280-VLEN 512b

Scalable from Microcontrollers to HPC

Scaling RISC-V to the Application Processor Domain

- The next wave of RISC-V adoption will occur at the bleeding edge, where raw performance is paramount
  - This is already happening today
- Recent advancements in microarchitecture, including multi-core and multi-cluster topologies will accelerate RISC-V adoption in diverse application areas such as mobile, autonomous vehicles, and the datacenter
- SiFive has 3+ years R&D investment in high performance, scalable RISC-V micro-architectures
  - First results seen in the release of the SiFive Performance P550 in Q2 2021
    - SiFive's first out-of-order production-ready processor
  - Multiple customer tape-outs in Q1 2022
  - The SiFive Performance P550 is the first step and only the beginning

SiFive Performance P550 Application Processor

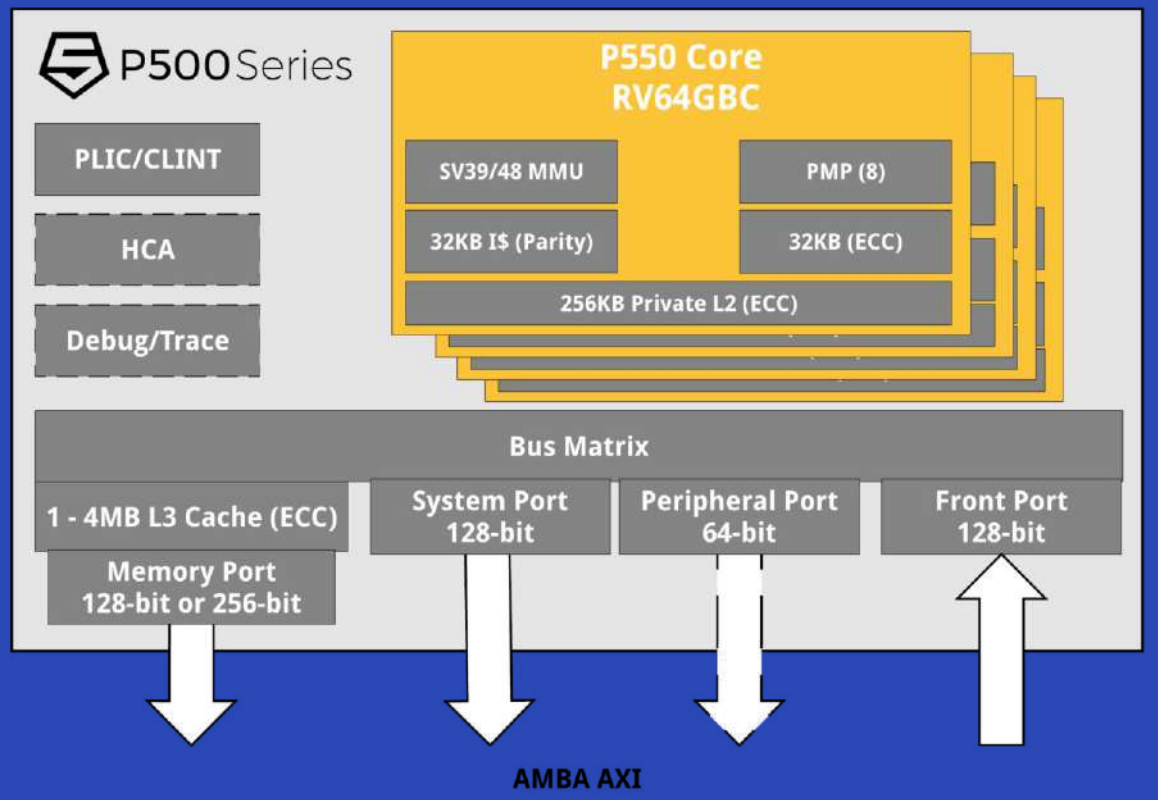
High-Performance Out-of-Order RISC-V Application Processor

The P550 Series is a 13-Stage, Triple-Issue, Out of Order processor making high-performance RISC-V processors reality while maintaining class leading area and performance density. The P550 processor supports multicore coherence with up to 4 cores in a core complex.

64-bit ISA includes with Double-Precision FPU and Bit Manipulation Extensions

Coherent Multicore with up to 4 Cores in Core Complex

Private L1 and L2 Caches for improved memory performance

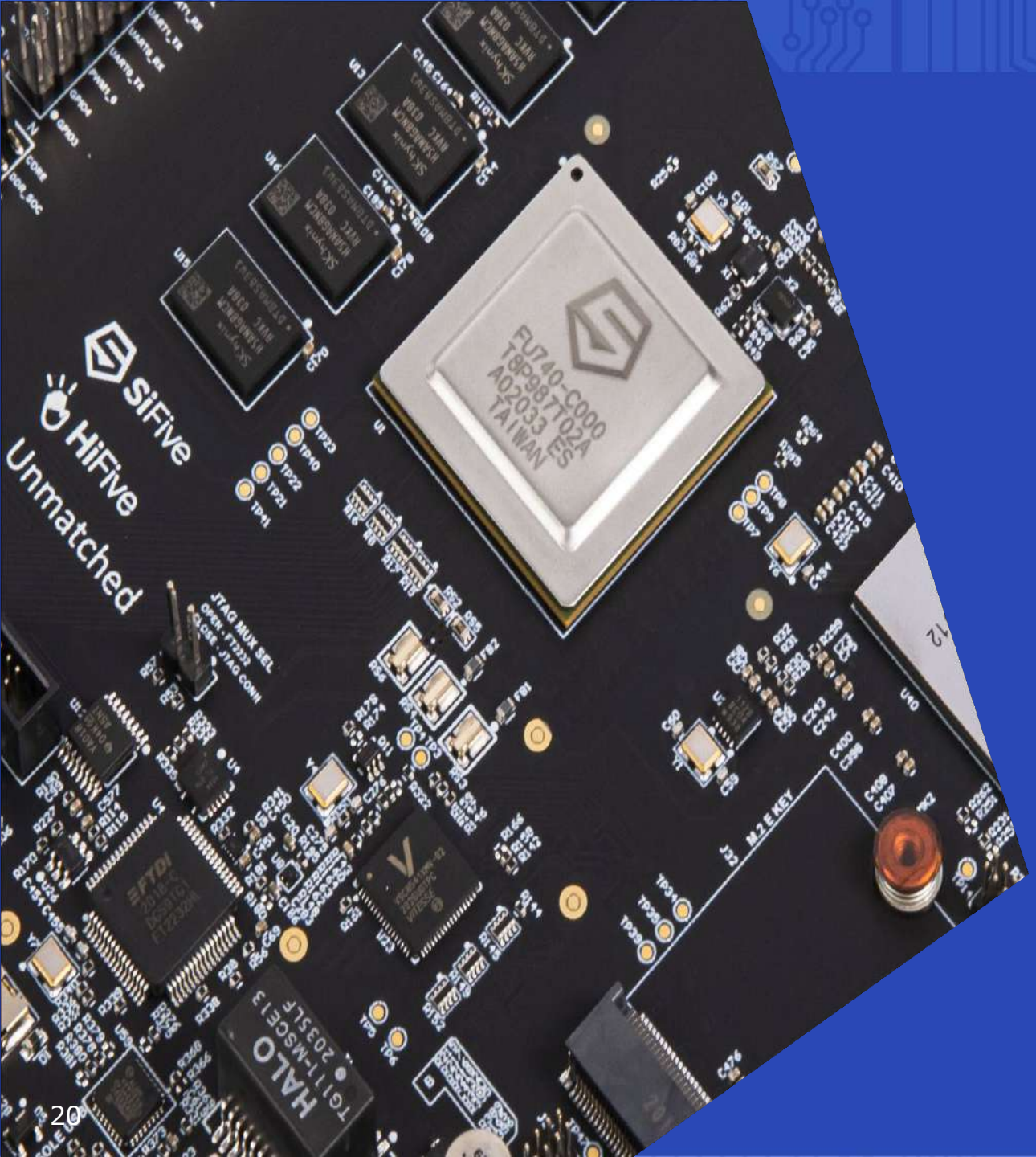


8.7 SPECInt2k6/GHz
2.4GHz in 7nm
0.23mm2

Sophisticated Trace and Debug capabilities

Advanced Security Capabilities and Crypto Accelerators

Pre-Integrated and Verified Verilog RTL Deliverable



Beyond SiFive Performance P550

The future of SiFive high performance processors

SiFive Application Processor – Next Generation

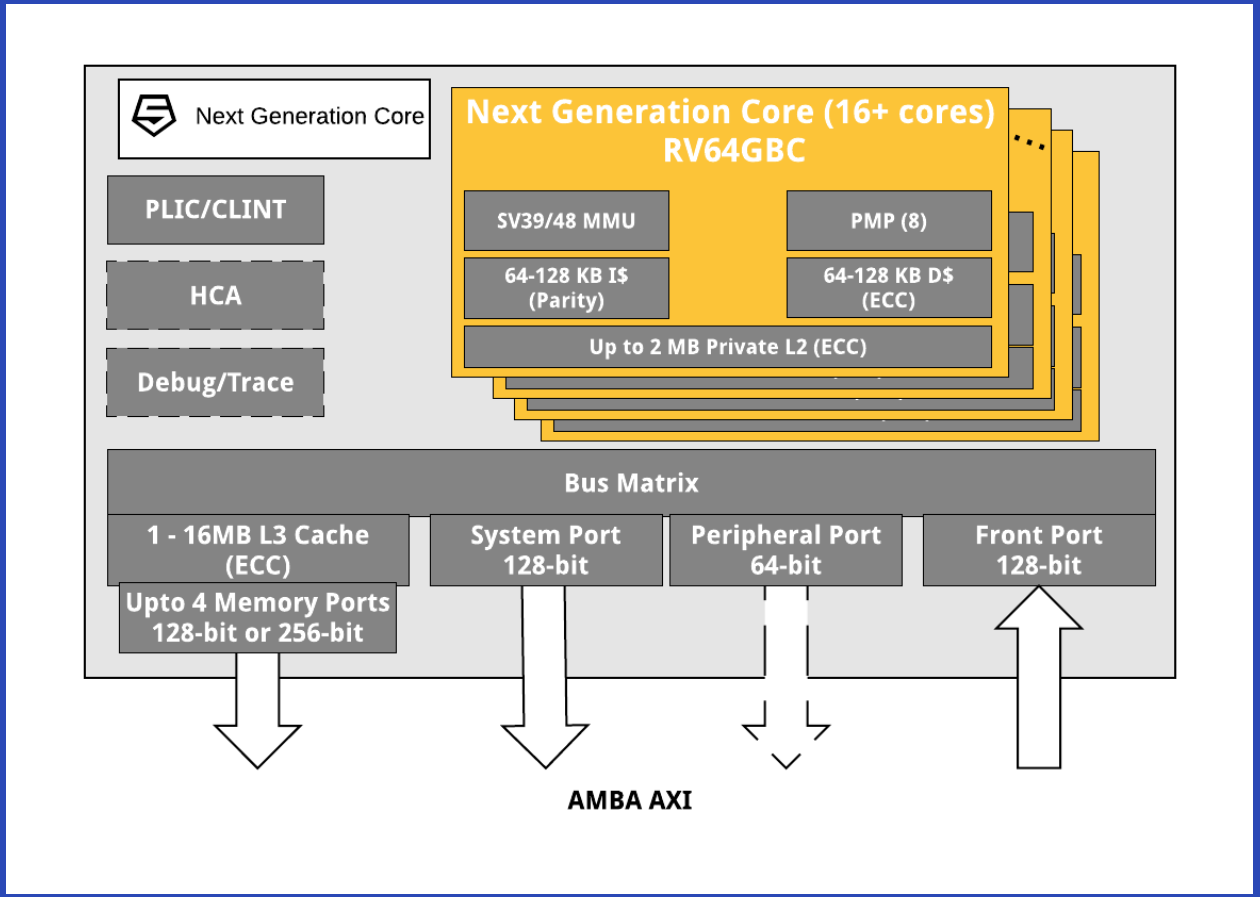
High-Performance Out-of-Order RISC-V Application Processor

A Quad-Issue, Out of Order processor making high-performance RISC-V processors a reality while maintaining class leading area and performance density. Supports multicore coherence with up to 16 cores in a core complex.

64-bit ISA with Double-Precision FPU and Bit Manipulation Extensions

Coherent Multi-cluster with up to 16 Cores in Core Complex

Private L1 and L2 Caches for improved memory performance



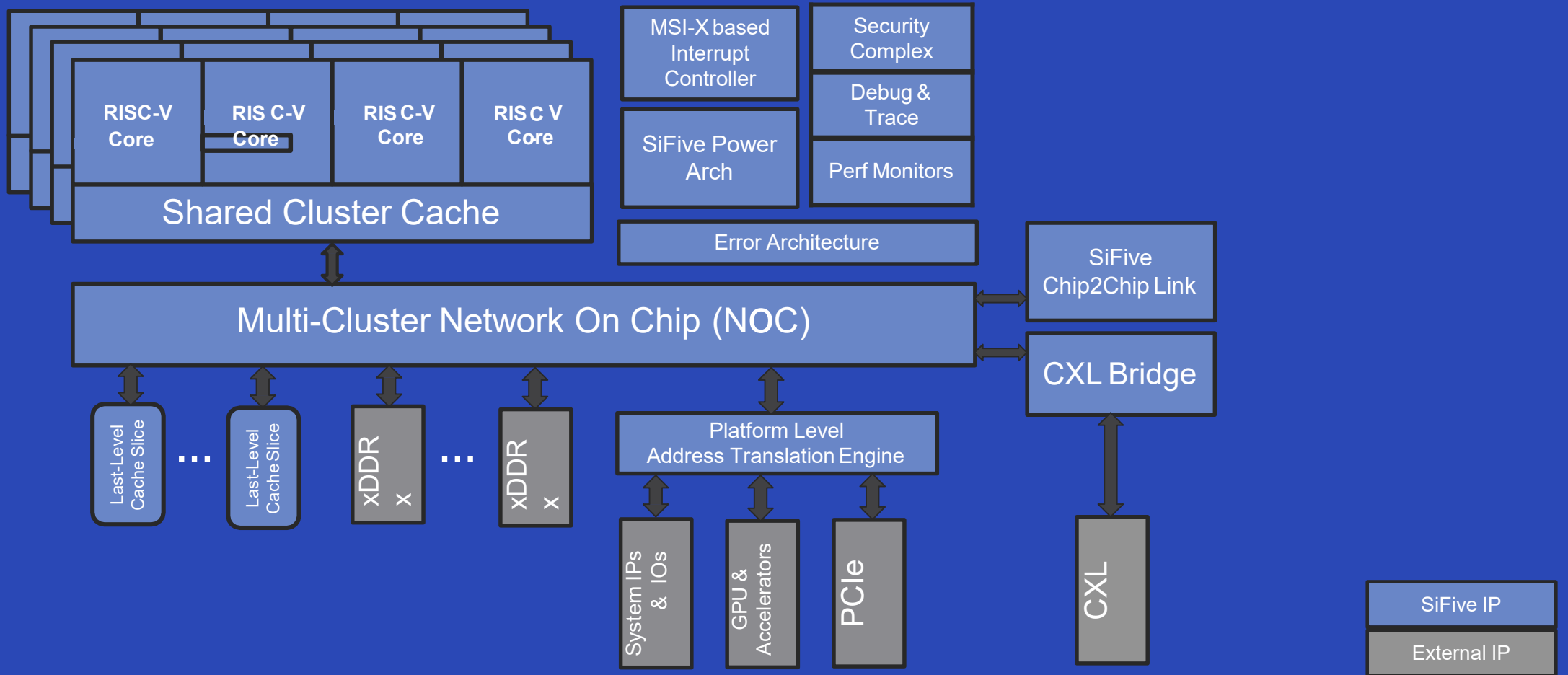
~50% higher performance over Performance P550

Sophisticated Trace and Debug capabilities

Advanced Security Capabilities and Crypto Accelerators

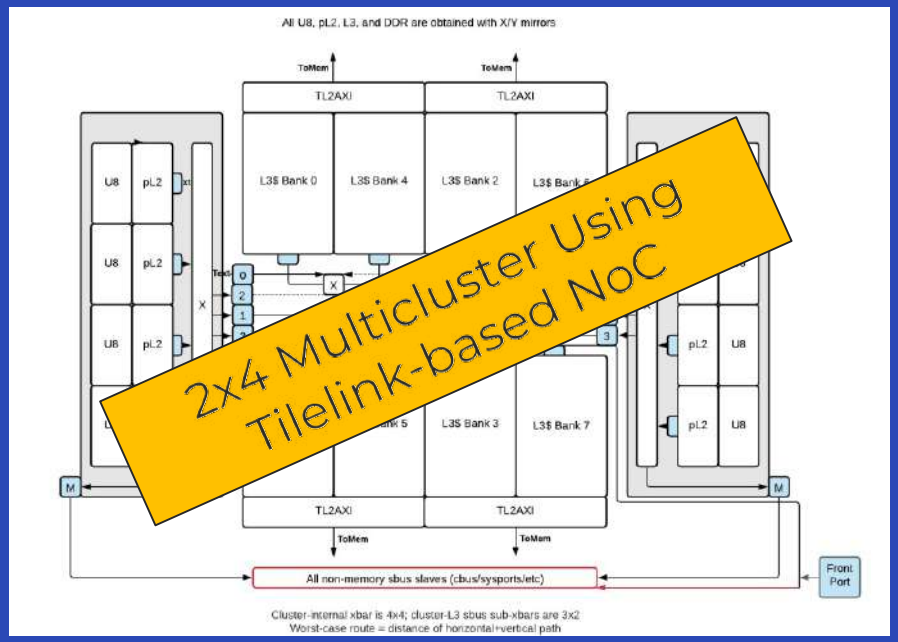
Towards The Freedom Revolution Platform

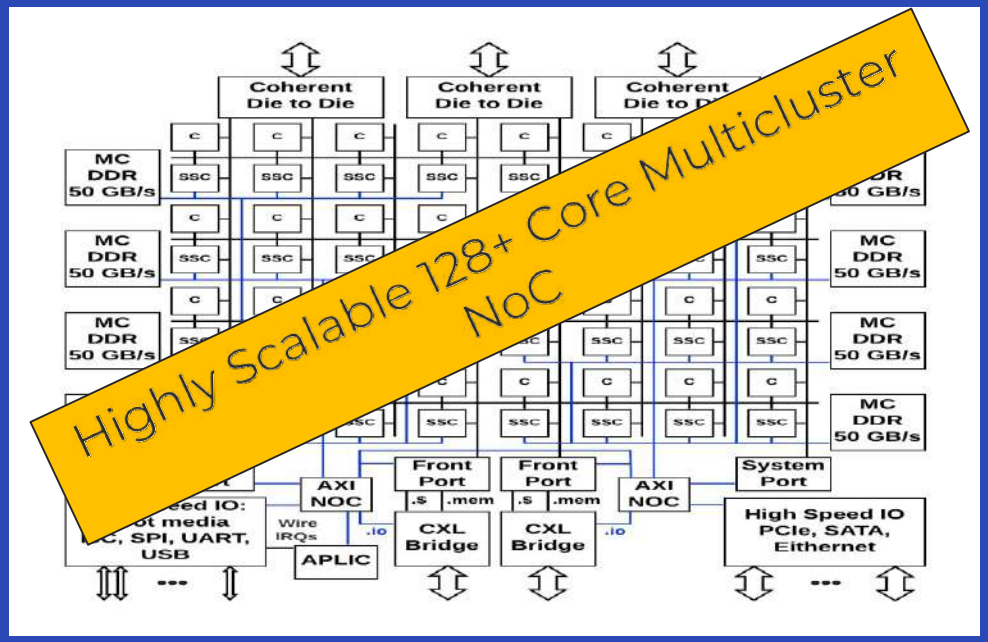
(vision of a complete solution)



SiFive Freedom Revolution is a concept platform built with SiFive & Third-Party IPs

Multicore Scalability to 128 cores & beyond





TileLink to Other Interface Converters

TileLink2 Upgrade

Non-inclusive Cache Hierarchy

Higher Frequency

Advanced Interrupts

Advanced Interrupt Architecture
(RISC-V International work in progress)

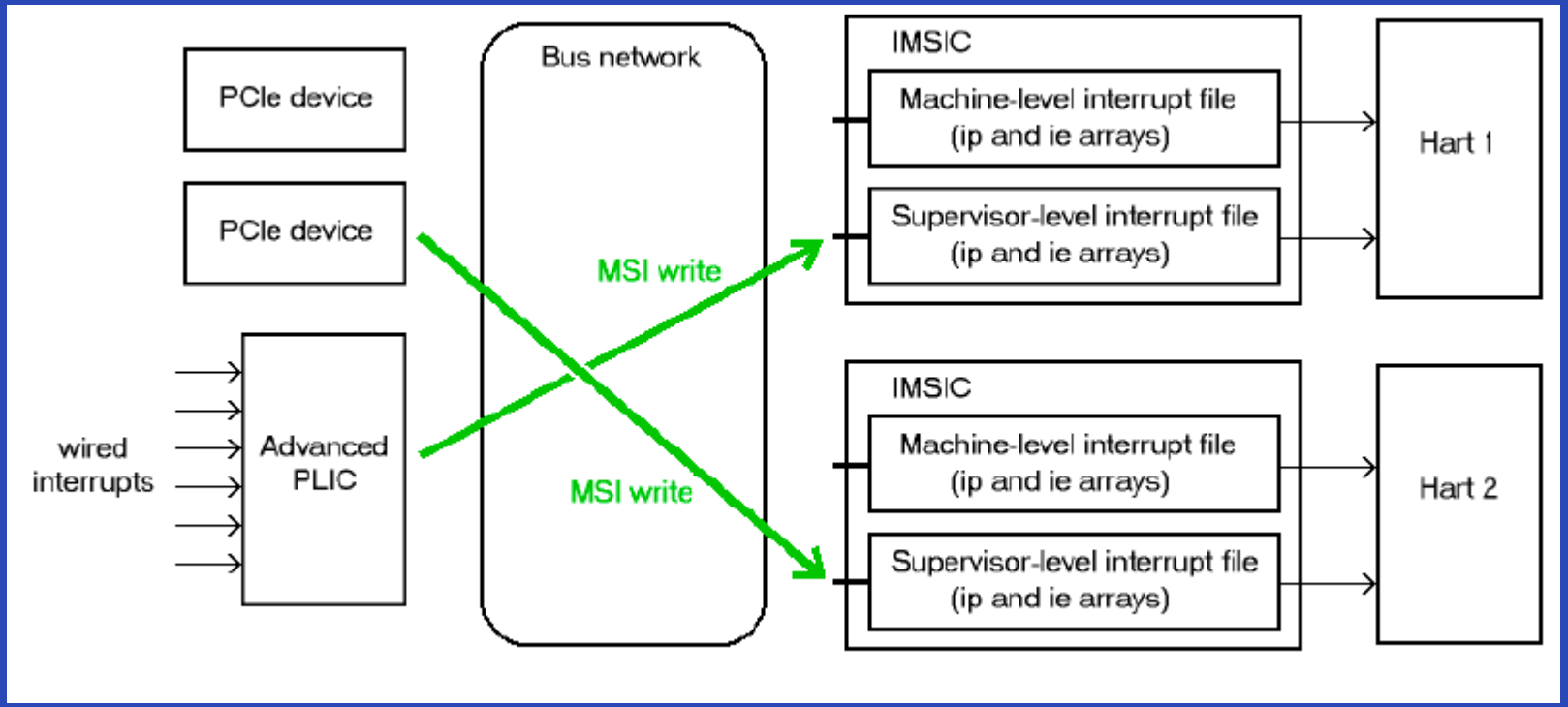
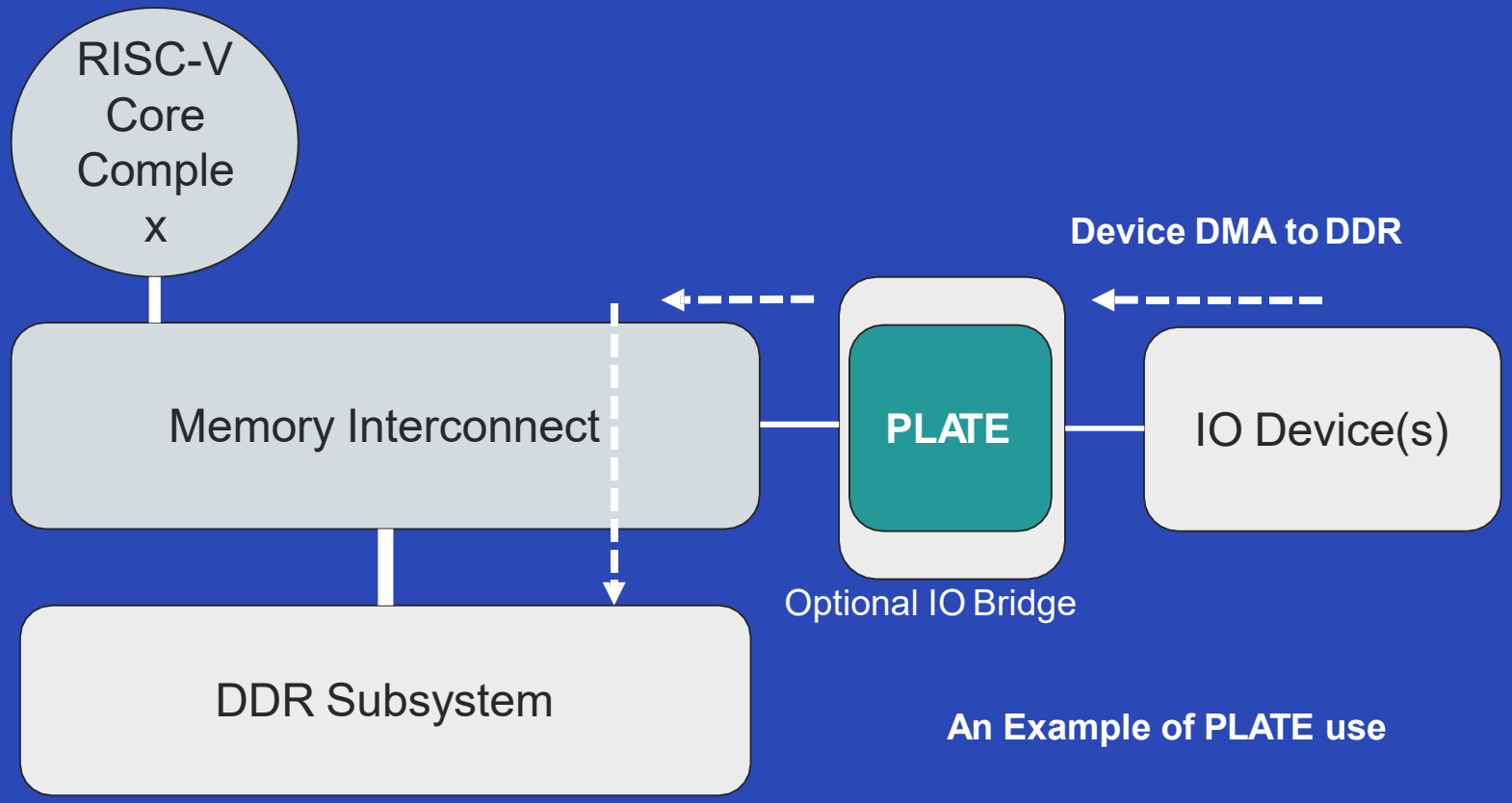


Figure from spec

MSI-X interrupts delivered directly from device to a hart
SiFive will support Advanced Interrupts

PLATE: Platform-Level Address Translation Engine

For system level memory management



SiFive-specific IP enables fast yet protected DMA

Power Management

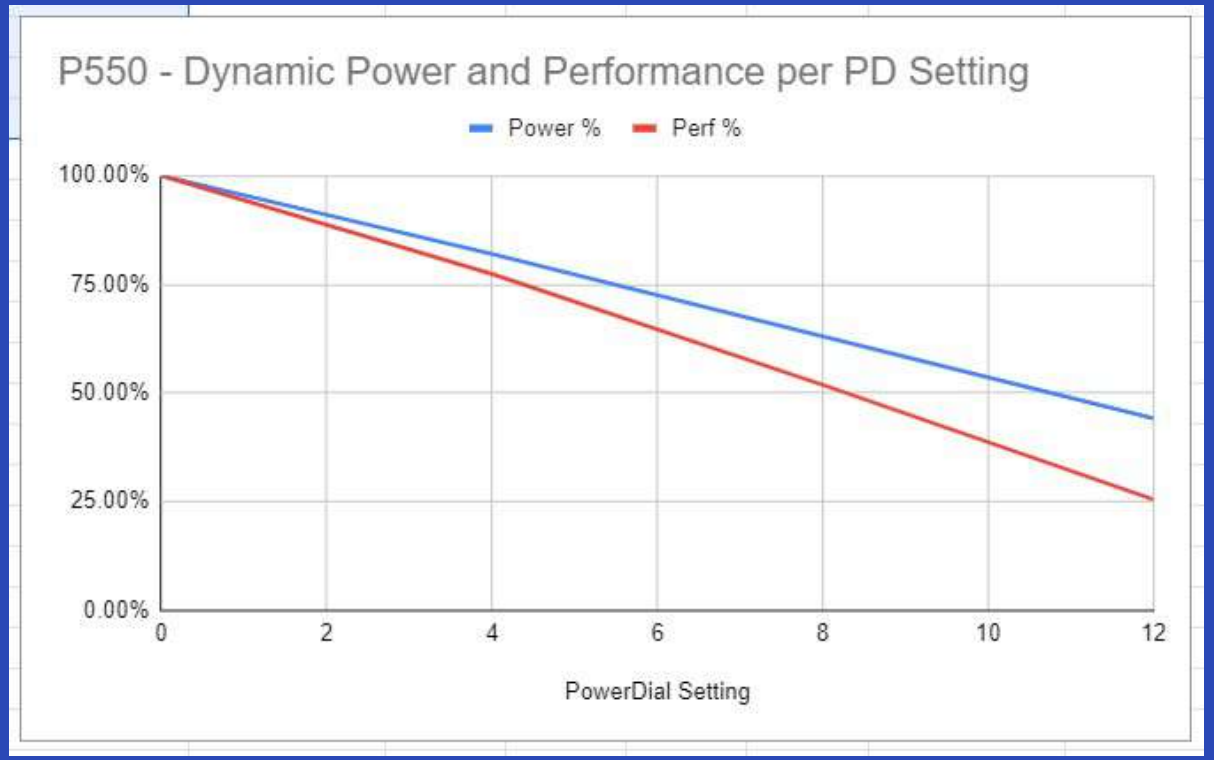
Idle Power Management

- WFI Clock Gating
- Power Down
- Retention States

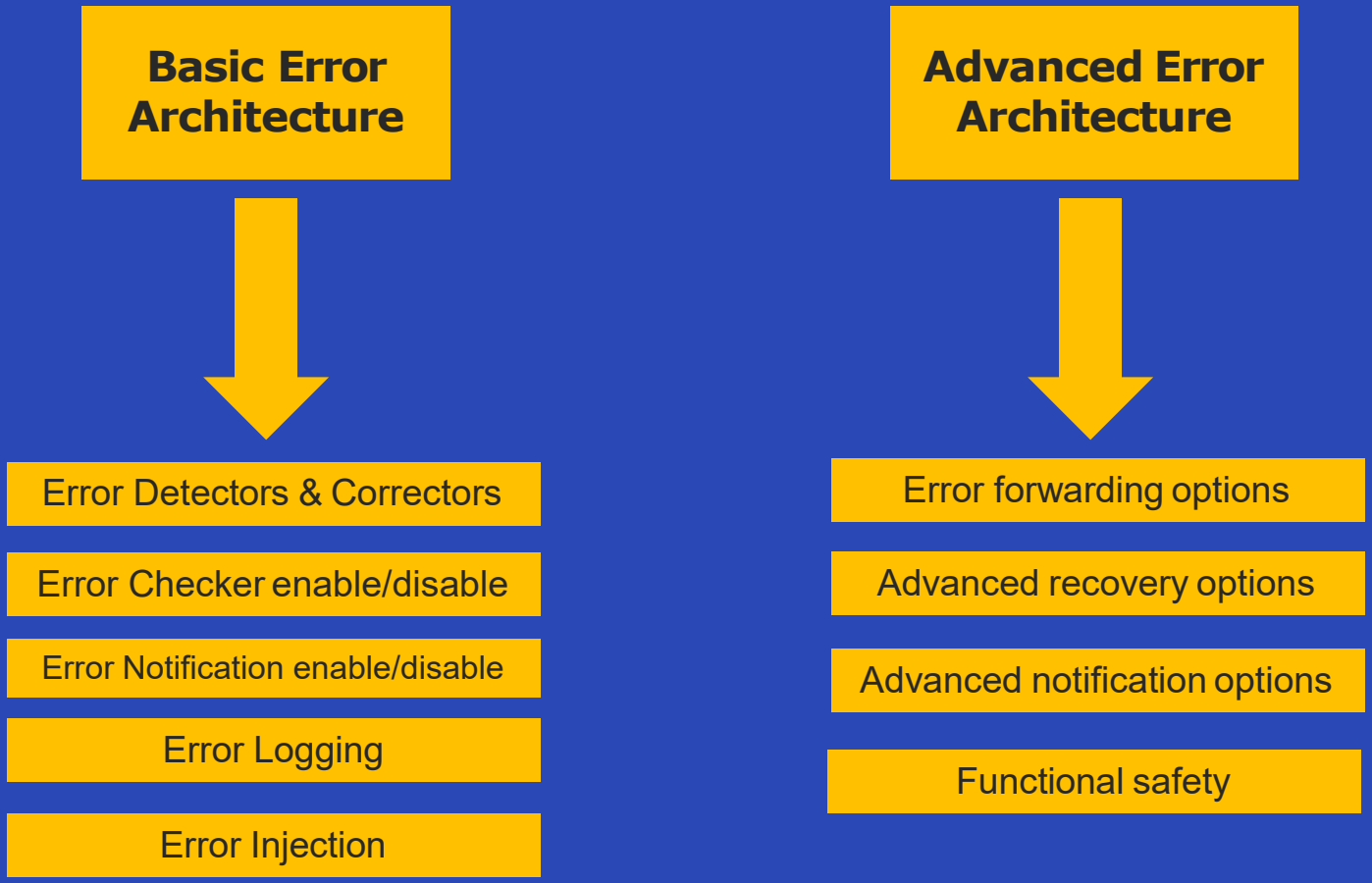
Dynamic Power Management

- Power Dial
- DVFS
- Power control & measurement

SiFive Power Dial: Digital Throttle to Reduce Power Performance vs. Power



Advanced Error Architecture



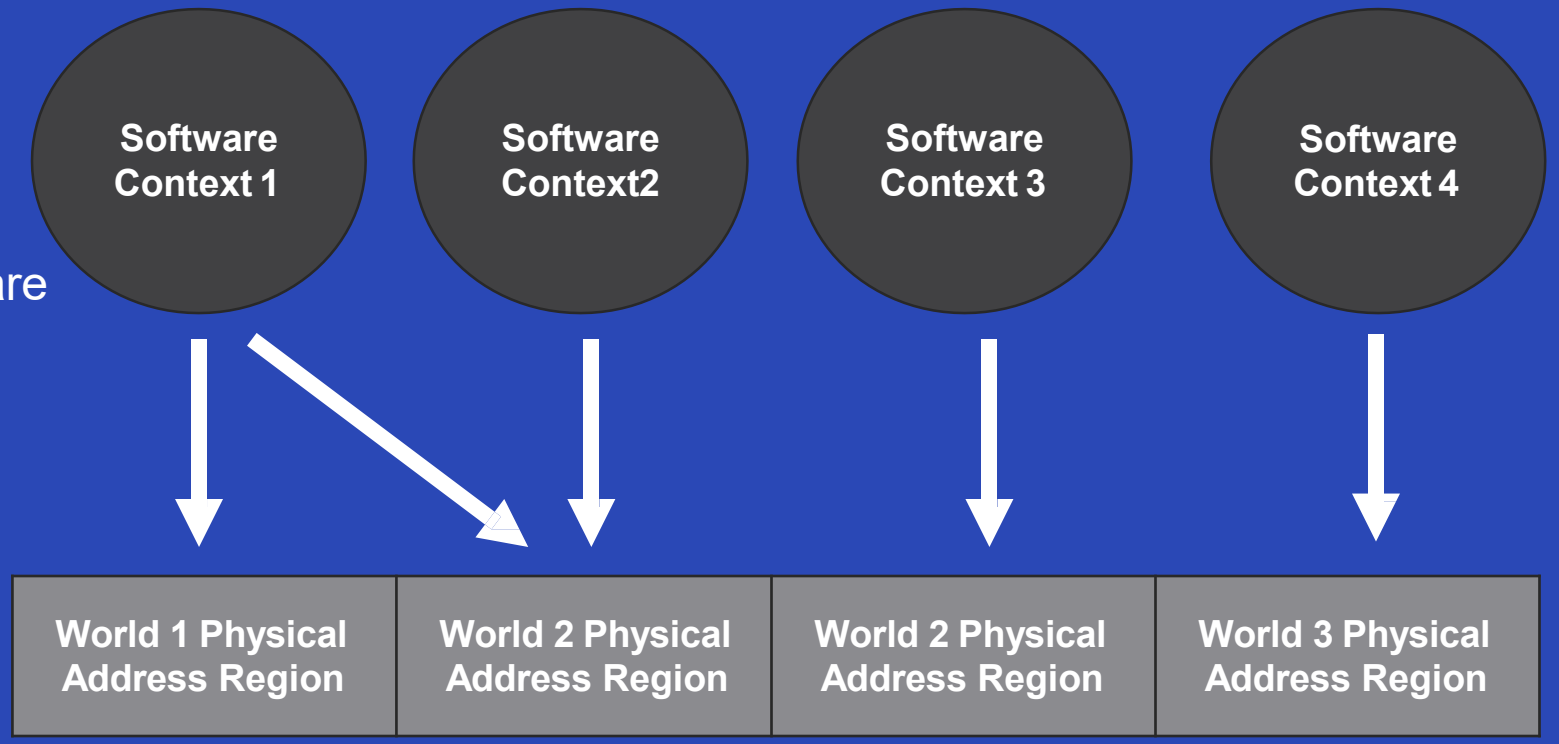
Delivering advanced error architecture for safety-critical applications

Security: SiFive WorldGuard-Based Isolation

SiFive WorldGuard isolates software contexts using world identifiers

Trusted agent (e.g., RISC-V M-mode) assigns world identifiers

Example SiFive WorldGuard Configuration

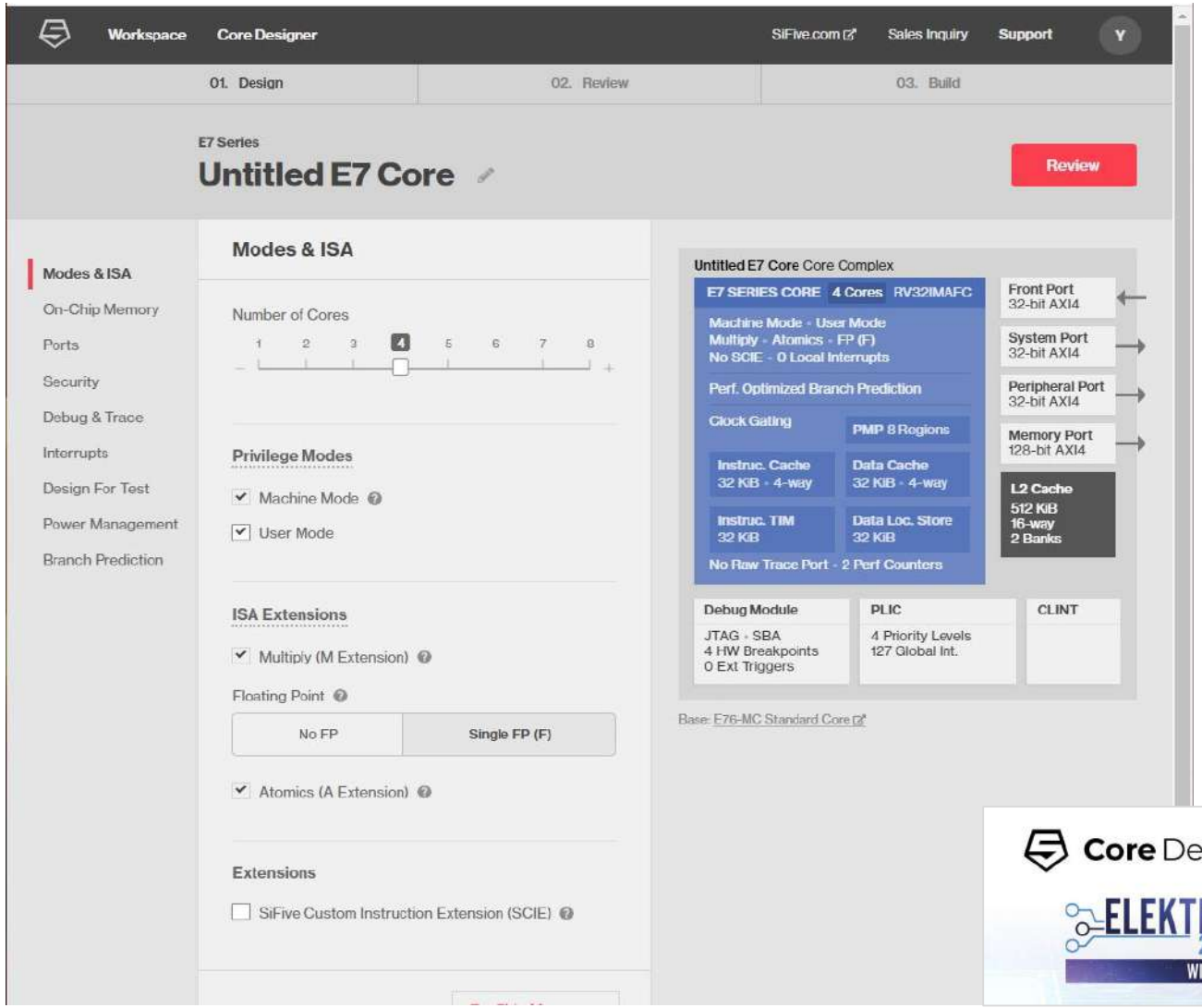


(World 2 is shared between Software Context 1 & 2)

WorldGuard Provides Isolation of Physical Address Regions among software contexts

SiFive Core Designer

Optimize SiFive RISC-V Core IP for Your Application



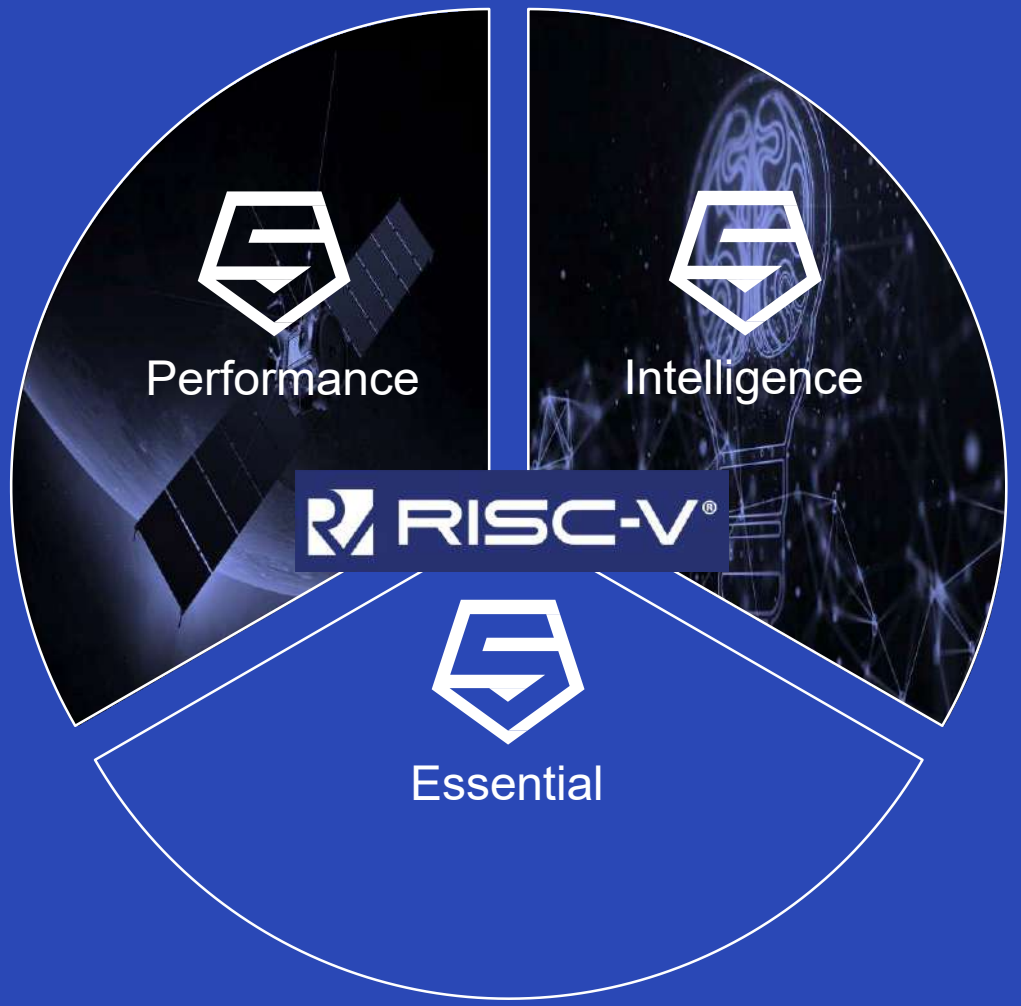
- SiFive Core Designer enables configuration of SiFive RISC-V Core IP through an easy to use Web Portal
- **Variants** are generated with click of a button and are available from the Workspace
- **Variants** contain
  - RTL matching the configuration, including a testbench and other collateral needed to realize the design
  - Documentation specific to the design
  - Customized bare-metal BSP for easy integration into SiFive's SDKs
  - FPGA bitstreams for common FPGA development boards for easy software benchmarking of the RC

The Future of RISC-V Has No Limits

The Highest Performance, Most Advanced RISC-V Processor Available

Very High Performance & Efficiency for AI & ML Acceleration

The Industry's Broadest Family of Scalable, Configurable Control & Embedded Cores



SiFive Performance Next-Gen:

- +50% Perf
- Scalable to 16 coherent cores
- Class-Leading Area Density

EndPoint向けAI SoC「AiOnIc®」

小型、低消費電力アーキテクチャと
ホストプロセッサとしてのRISC-Vとの融合

ArchiTek

2021年11月17日

会社概要

2011年	創業（3名でスタート）
2017年	NEDO SUI(Startup Innovator)に採択
2018年 （第2の創業）	VCより出資 （シリーズA） 5億円調達 SPARX Asset Management Co., Ltd. Mirai Creation Fund TechAccel NTT docomo 株式会社NTTドコモ・ベンチャーズ MUFG 三菱UFJキャピタル株式会社 池田泉州キャピタル株式会社 経済産業省企画のJ-Startup(第1期)に選定 J-Startup NEDO「革新的AIエッジコンピューティング技術の開発」に採択
2020年	シリーズAと同一VCより出資（シリーズB）約5億円調達(累計10億円） 1月にNEDOプロジェクトでの試作LSIが完成  開発コード：**arima** 11月に自己資金による独自LSIの試作が完成  開発コード：**beppu**

「AiOnIc®」の特長

✓「AI推論」と「画像/音声処理」に特化

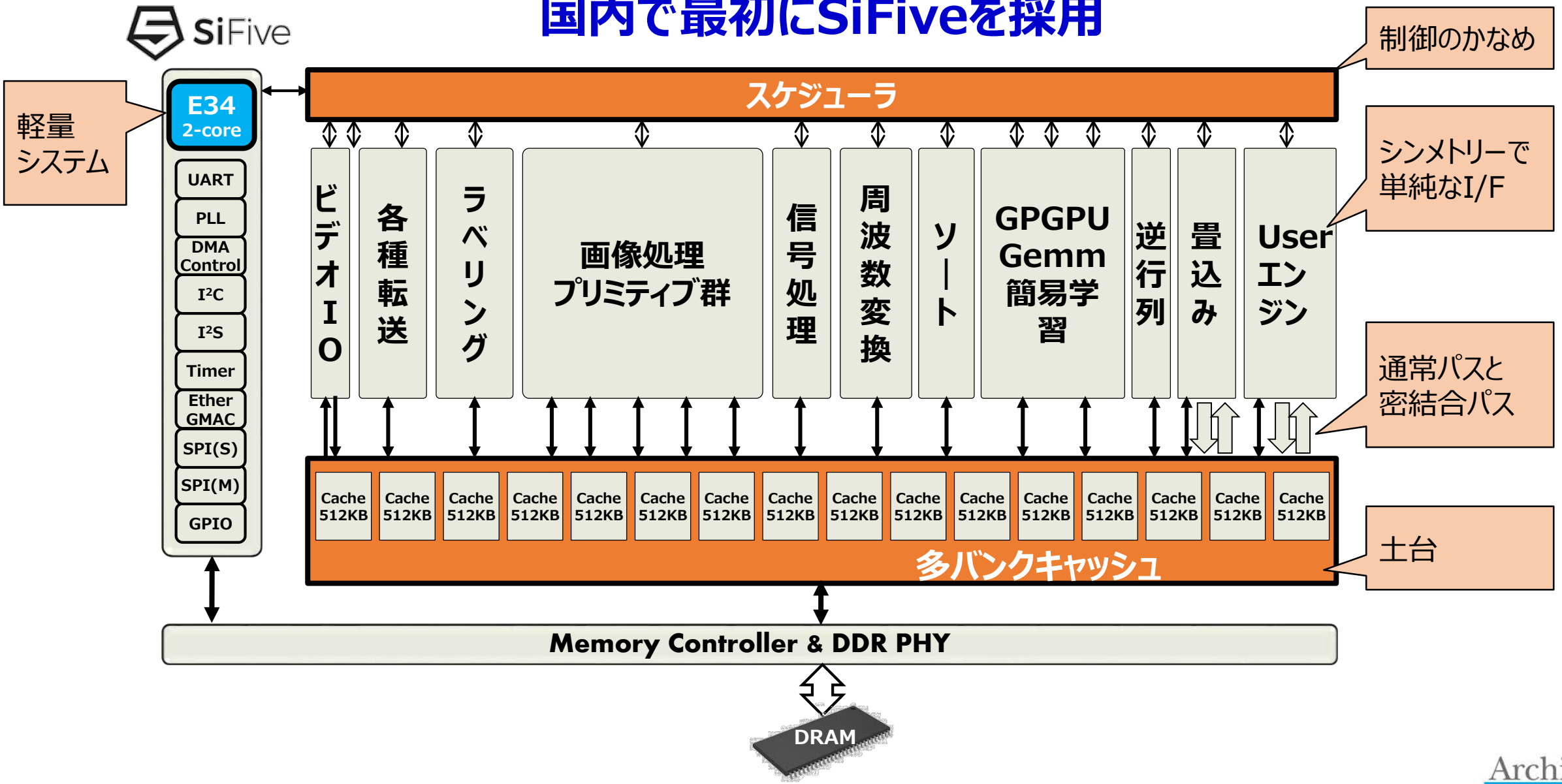
✓ 高い電力性能（低燃費）

✓ 低レイテンシでストレスなく並列実行

身の周りで使える組み込み用SoC

SoC(beppu)の内部構成

国内で最初にSiFiveを採用



『 AiOnIc® AIカメラ・キット』

「電池駆動」および「ファンレス」を実現！

エッジAIプロセッサ　AiOnIc®

System Processor (600MHz):
SiFive E34 x2

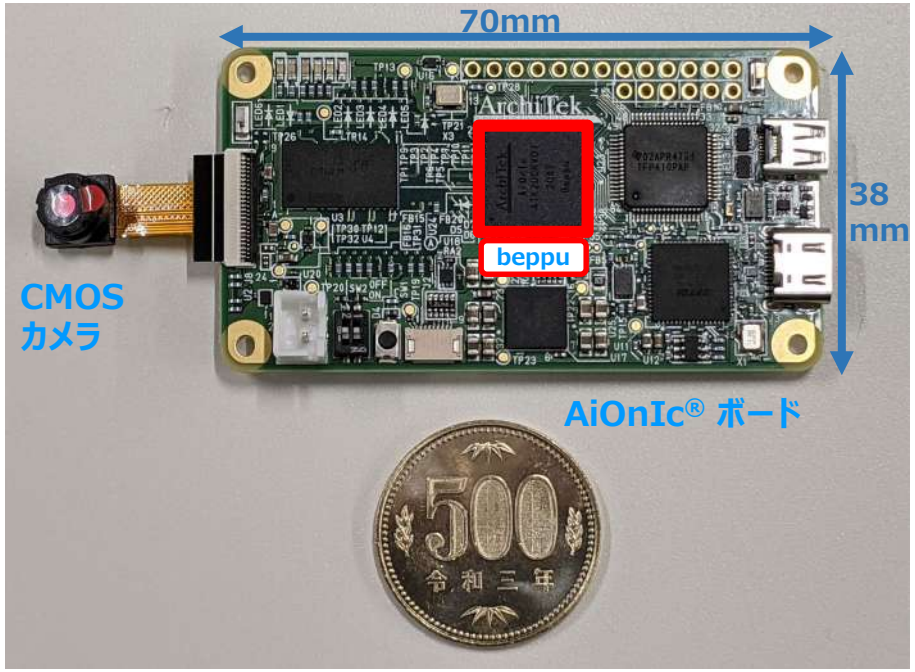
CV Engine (600MHz):
各種CV, FFT/IFFT, Labeling, Bitblt, Sort, 逆行列, デジタル信号処理

AI Processor (600MHz/375GOPS):
GPU x4,
GeMM x4（Float型ディープラーニング）

メモリ:
内蔵8MBキャッシュ, 内蔵512KBレジスタファイル, 外部SDRAM DDR4 2.4GBps

IO:
UART x4, I2C x4, I2S, SPI x2, QSPI, GPIO

AiOnIc® AI カメラ・キット



SoC：
AiOnIc “beppu“
メモリ：
DDR4 8Gbit, SPI Flash 128Mbit
基板サイズ：
70 × 38mm
電源電圧：
5V (USB Type-Cコネクタ)

インターフェース：
USB Type-C(5V, USB, UART, HSPI)
microHDMI(画像出力)
microSDカード
Ethernet(EJ45コネクタは非実装)
パラレルI/Fカメラ(OV2640)

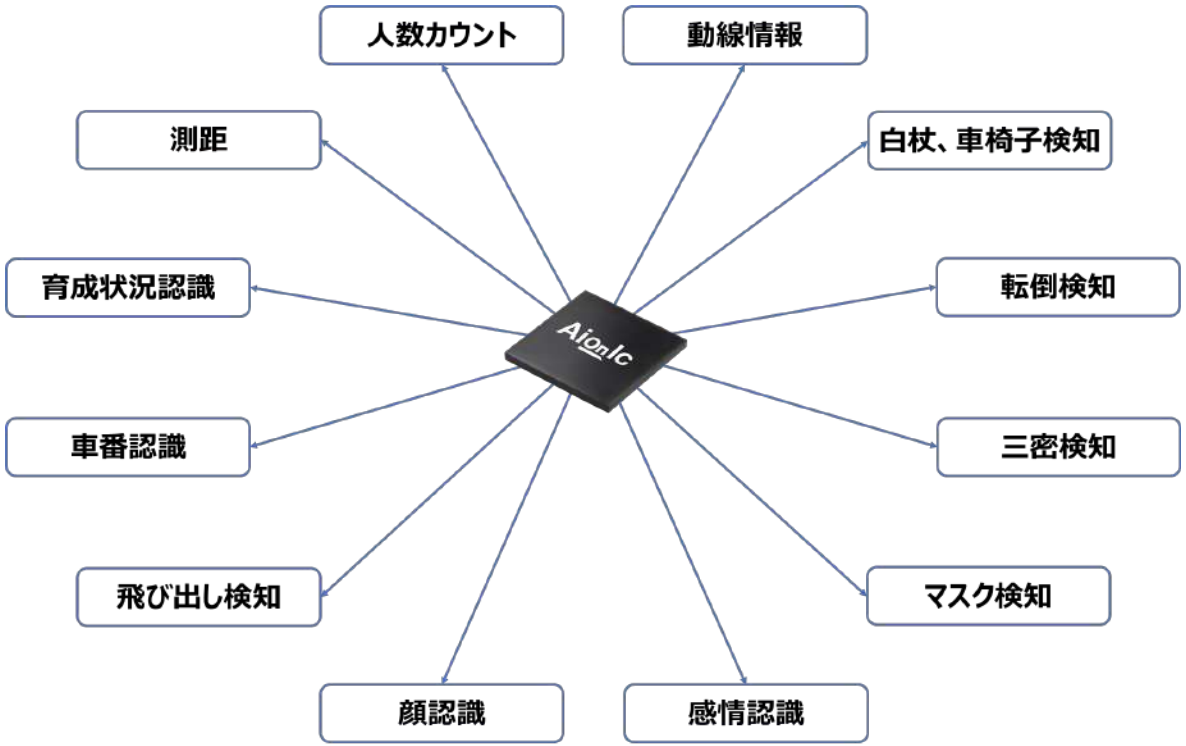
ArchiTek

『録画しないカメラ』で社会問題を解決

「画像データ」を「メタデータ」に変換

プライバシー含む
サイズ大

プライバシー含まず
サイズ極小



SDGsへの貢献

ArchiTek

当社CEOが14:35から登壇

次期量産チップ “chichibu” のエッセンスをご紹介いたします。

13:50-14:35	日	RISC-V RTOS セキュア IoT #day1_06_shc	河崎 俊平 | SHコンサルティング株式会社
14:35-15:05	日	仮想エンジンアーキテクチャとRISC-Vの融合 #day1_07_architek	高田 周一 | ArchiTek株式会社 | 代表取締役
15:05-15:15		休憩	
15:15-16:00	日	ルネサスのRISC-Vへの取り組み #day1_08_renesas	江藤 公治 | ルネサスエレクトロニクス株式会社, IoT・インフラ事業本部, MCU製品開発統括部統括部長/ 武蔵事業所長
16:00-16:30	日	組込み向けSoCを支えるRISC-VとAI技術・その実例 #day1_09_nsi	杉本 英樹 | 株式会社エヌエスアイテクス（NSITEXE,Inc.） | CTO

デモ

AIアルゴリズムのデモをご覧ください

- ✓ 姿勢推定と人数カウント
- ✓ 物体検知（Yolo v3）

お問い合わせ

SiFive社各プロダクトに関する
　お問い合わせ、および、サポートは以下の窓口にて承ります

ご連絡をお待ちしております

株式会社ＤＴＳインサイト LSI Design Service部

お問い合わせ窓口：　**info-sifive@dts-insight.co.jp**
サポート窓口：　**support-sifive@dts-insight.co.jp**