チップの民主化とVDEC, d.lab およびAI拠点

Chip democratization and VDEC, d.lab and AI Chip Design Center

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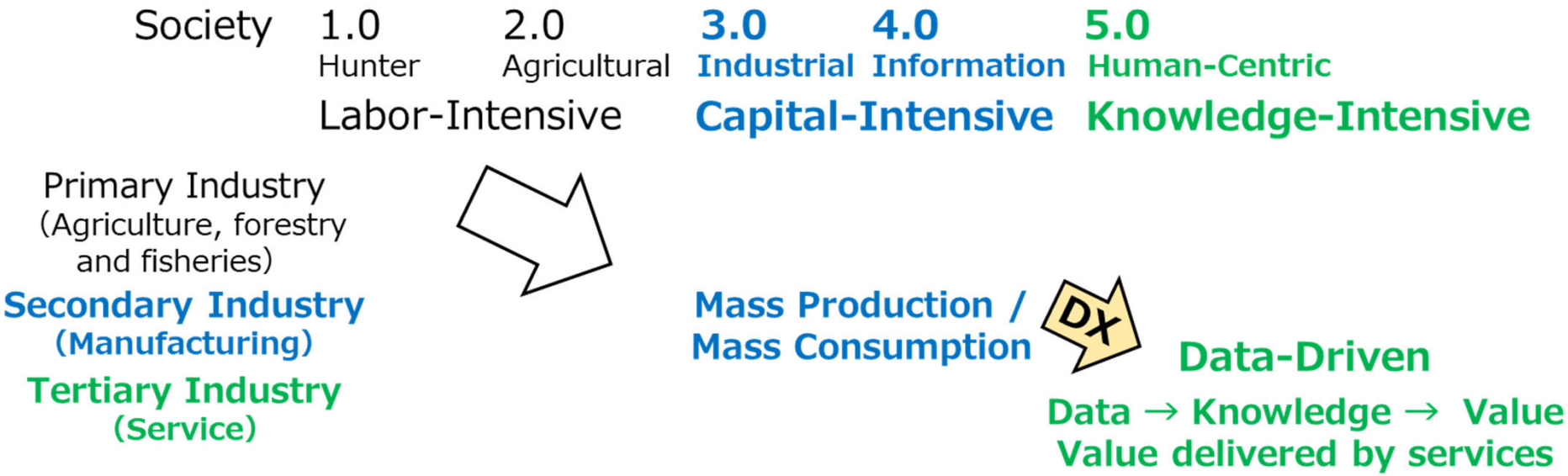
Activities toward chip democratization

- 1st Gen: MOSIS/CMP/…/VDEC
  - Centers for (Fab. Access / design environment support)
- 2nd Gen: CRAFT(2015)/IDEA(2017)/AIDC(2018)
  - Rapid prototyping, higher performance by Custom IC in the Advance Process
- 3rd Gen: Google/Skywater
  - Open source PDK , Open source EDA, Free shuttle

CRAFT: Circuit Realization At Faster Timescales
IDEA: Intelligent Design of Electronic Assets

Society's Paradigm Shift

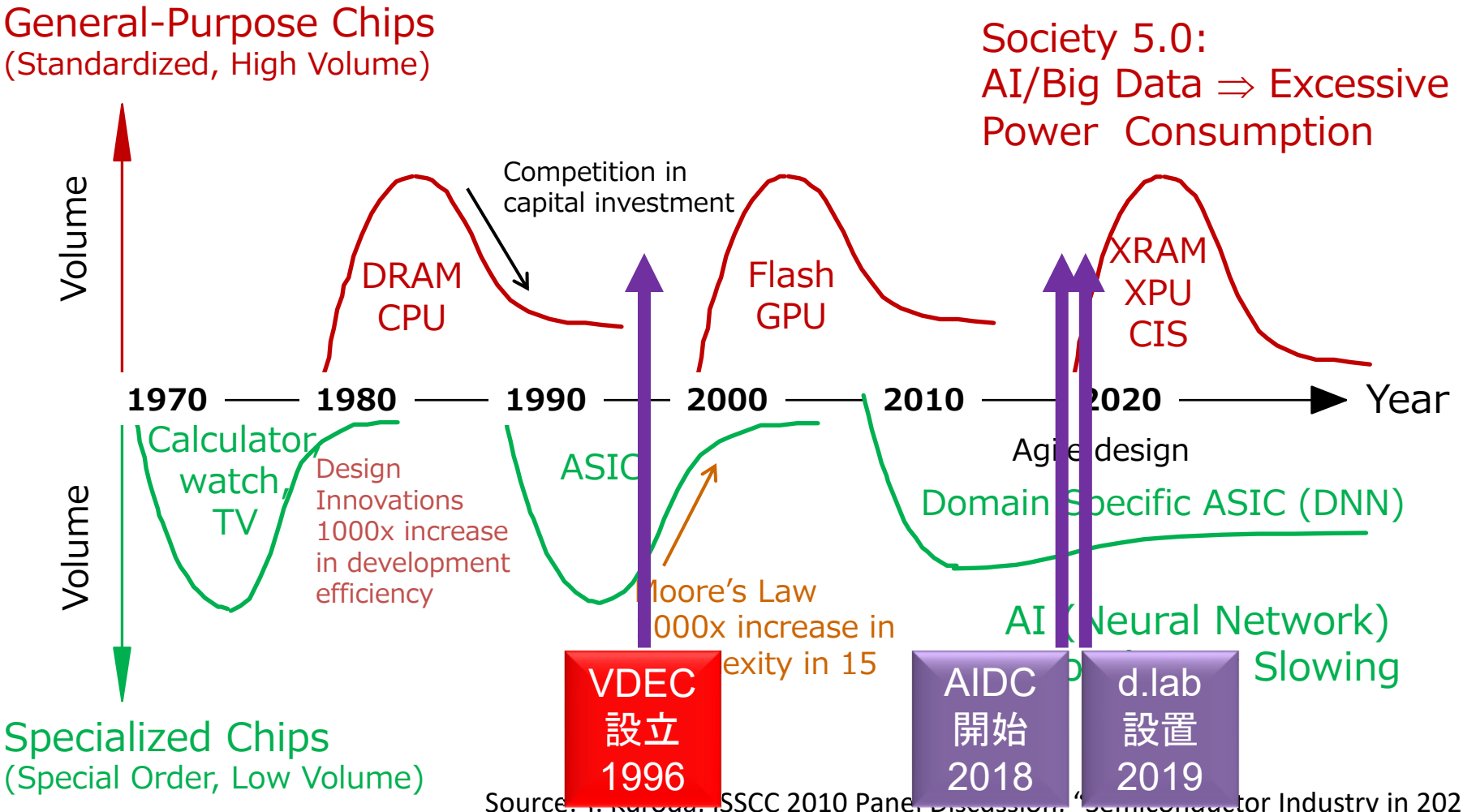


Alan Kay's talk at Creative Think seminar, July 20, 1982

Remember, it's all software, it just depends on when you crystallize it.

People who are really serious about software should make their own hardware.

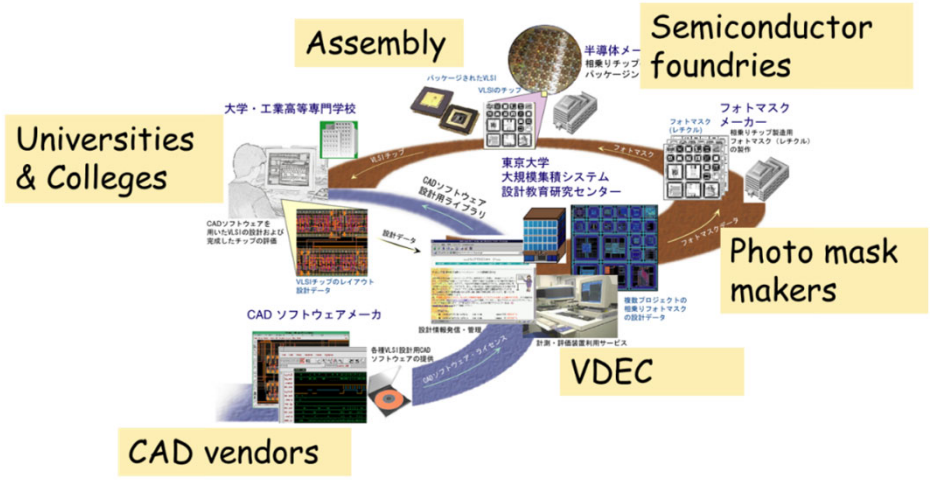
From General-Purpose to Specialized Chips



Source: T. Kuroda, ISSCC 2010 Panel Discussion, "Semiconductor Industry in 2025".

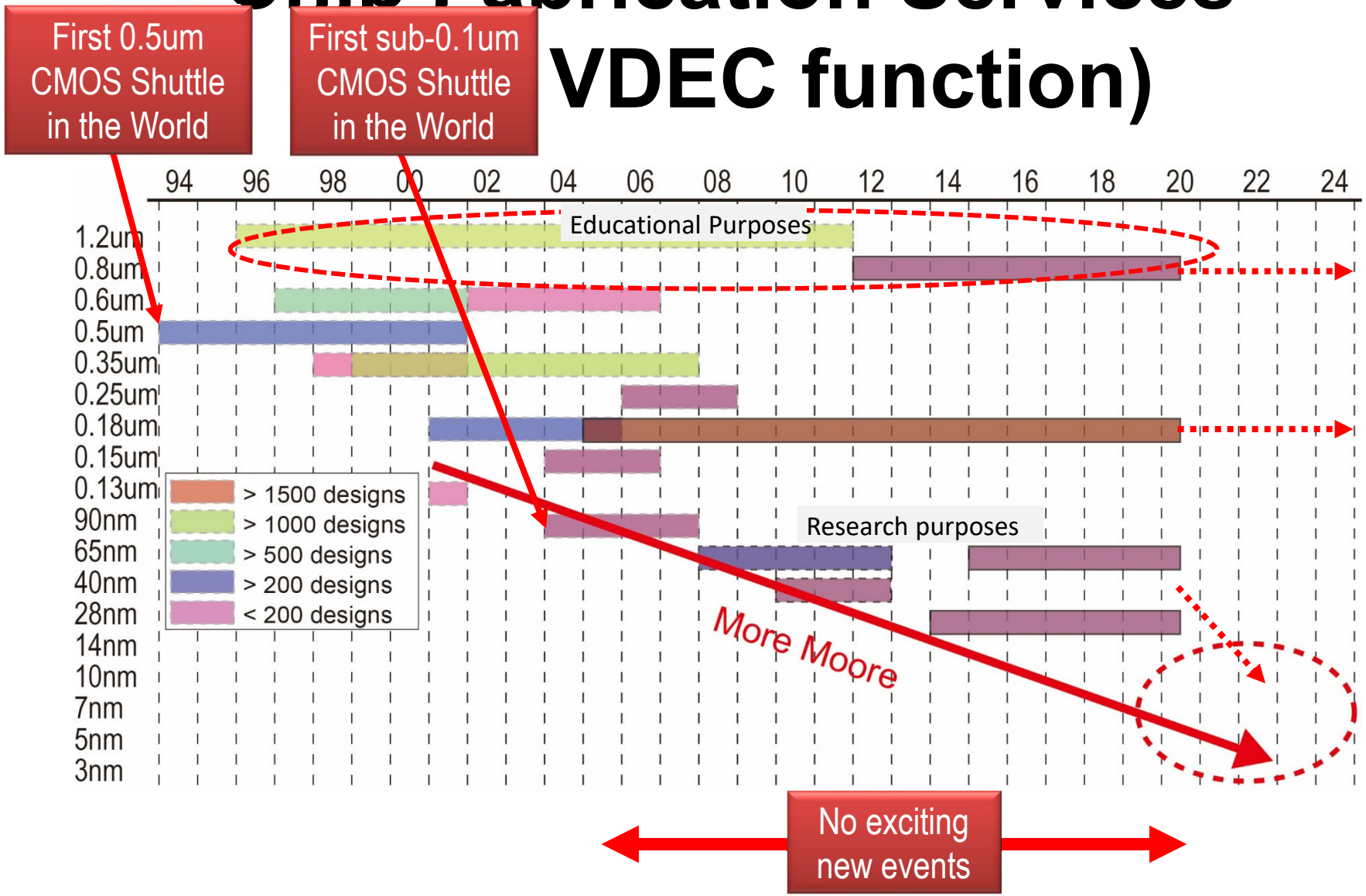
VDEC, as 1st Gen Activity

- Provide platform for chip fabrication
  - Provide chip fabrication services
  - Provide CAD tools
  - Provide up-to-date design methodologies/seminar

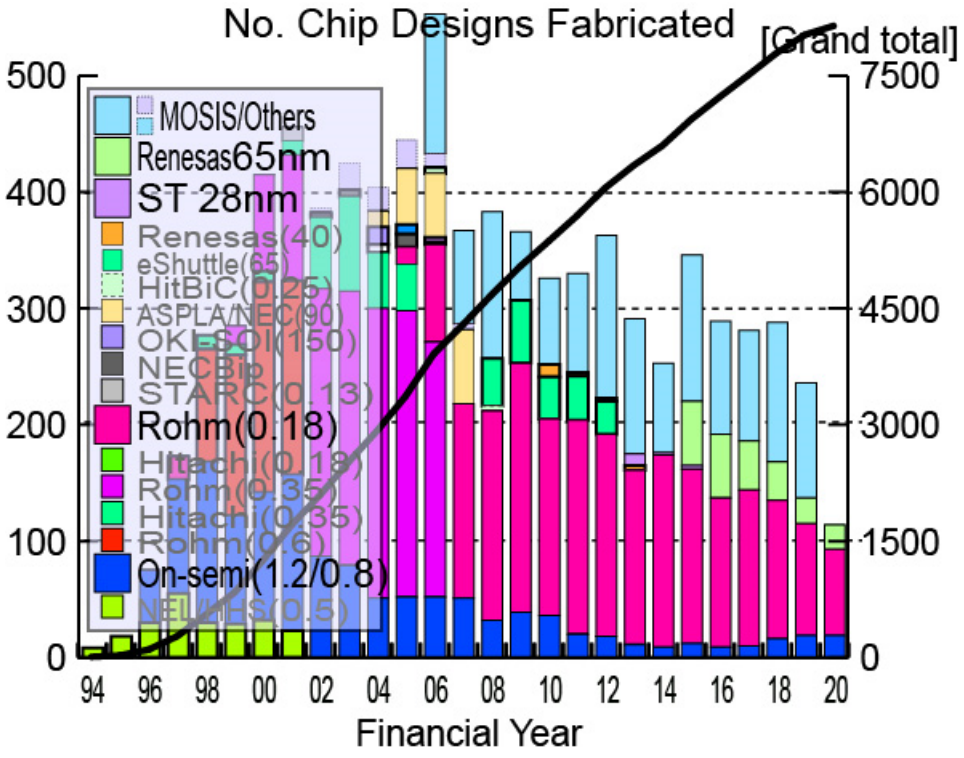


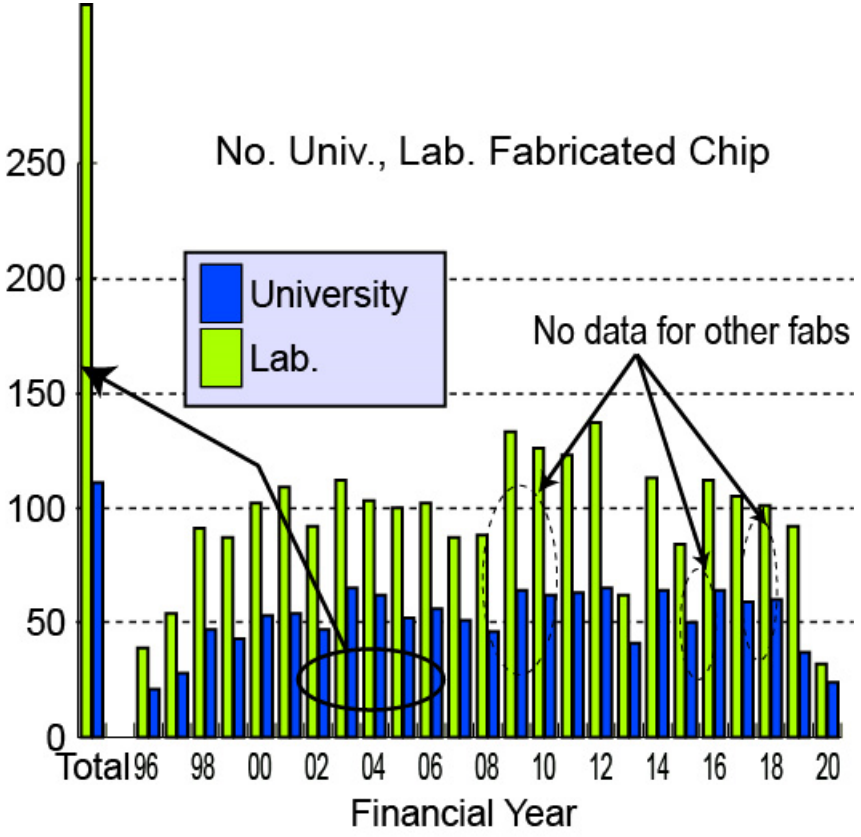
For chip democratization among Japanese Academia

Chip Fabrication Services (VDEC function)

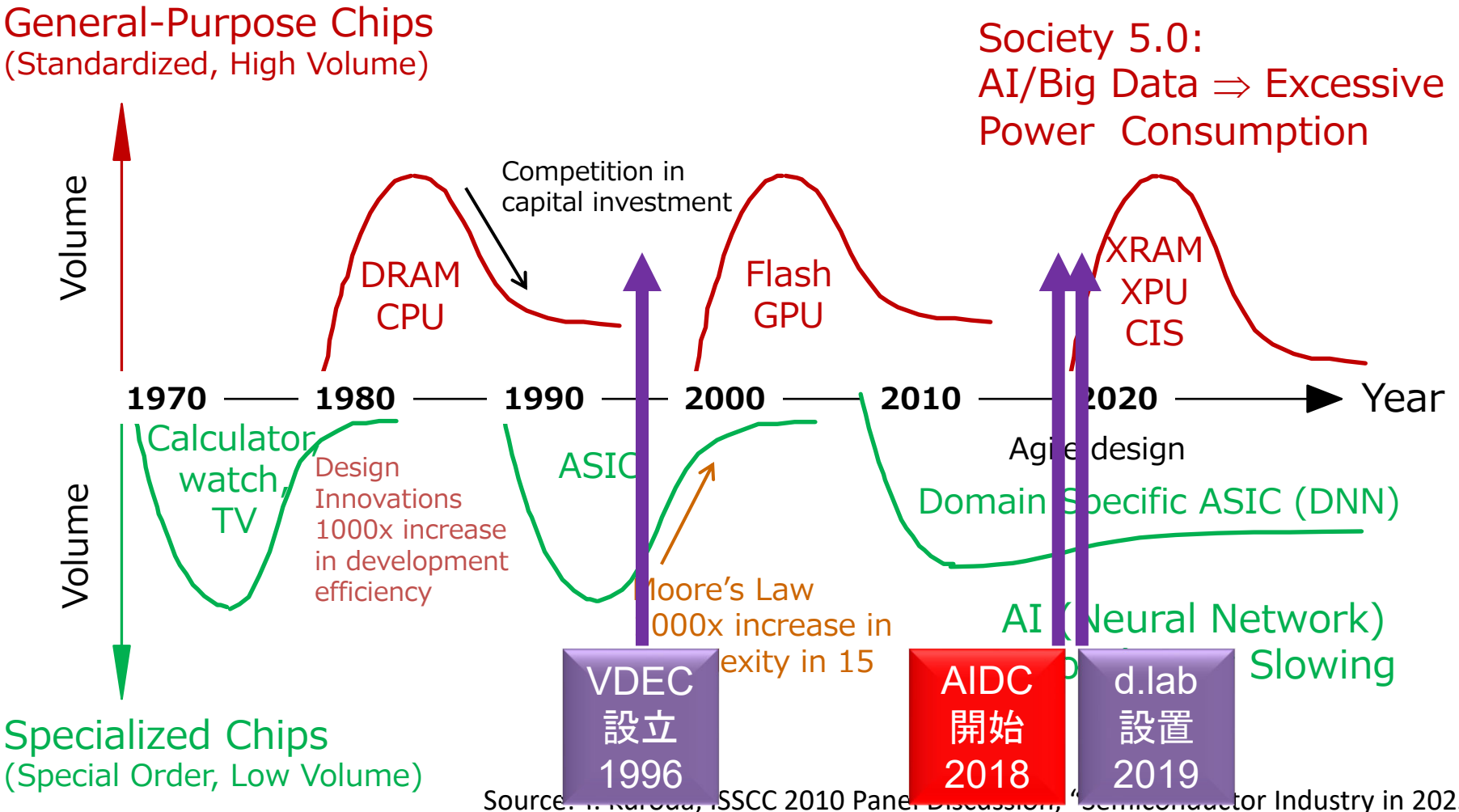


Trends of Chip fabrication



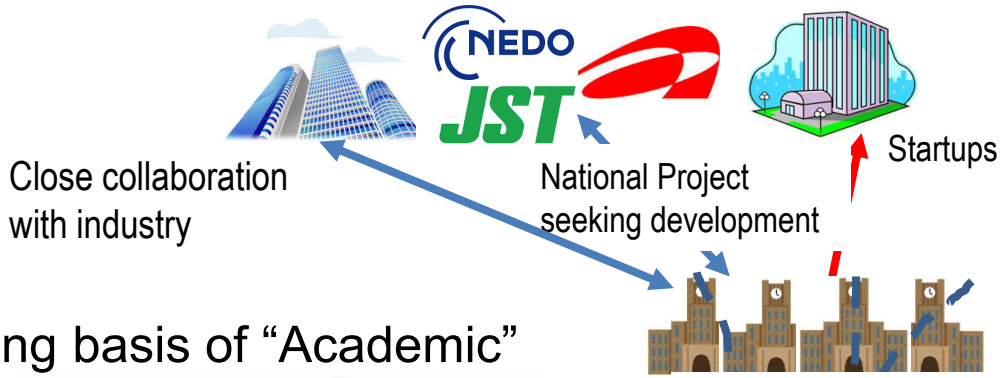


From General-Purpose to Specialized Chips



Source: T. Kuroda, ISSCC 2010 Panel Discussion, "Semiconductor Industry in 2025".

Step Toward VDEC 2.0
Platform for Advanced Chip design

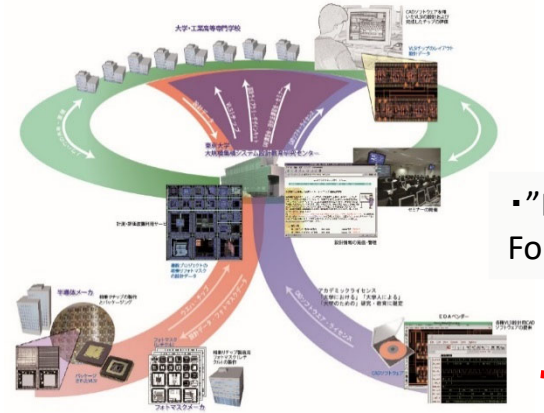


VDEC 2.0

AIDC: 2018~

d.lab: 2019~

- Maintaining basis of “Academic”



VDEC.EDU

VDEC 1.1

・”Extended Academic License”
For NEDO research project on “Across IoT”

2016~

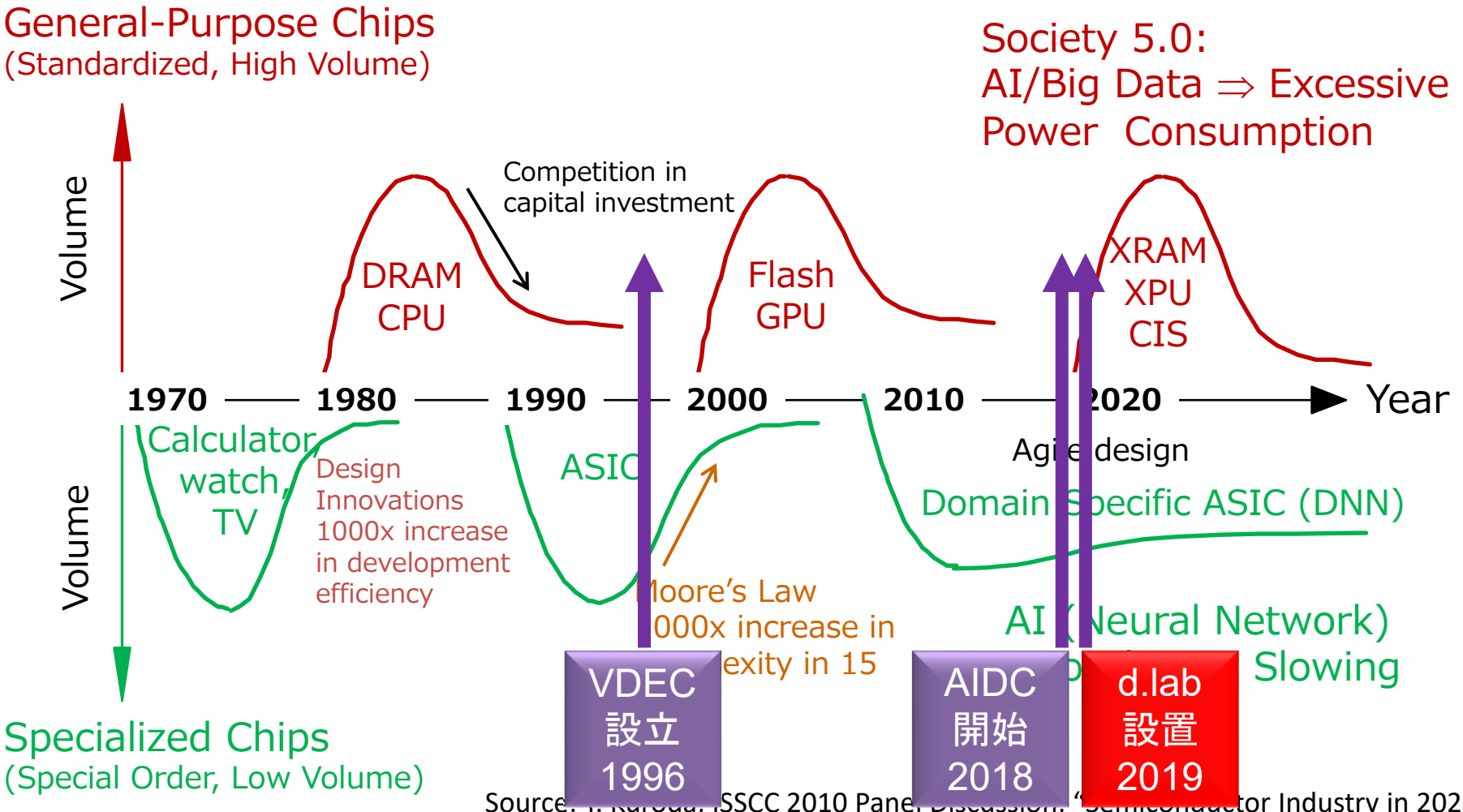
For chip democratization among Japanese Society

AI Chip Design Center

- Activity funded by METI and NEDO from 2018, at VDEC(now d.lab) & AIST
  - Platform for AI chip design in small company and startups
  - EDA tools for engineering samples
  - Verification platform by logic emulator
  - LSI-IP for AI chip design
  - Forum, seminars & materials for AI chip design
  - Chip fabrication gateway for the Advanced process for AI chip

Talk on SoC Design Platform.. By Dr. Uchiyama @ 9:45
Talk on RISC-V emulation.. By Dr. Arakawa @ 9:15 tomorrow

From General-Purpose to Specialized Chips



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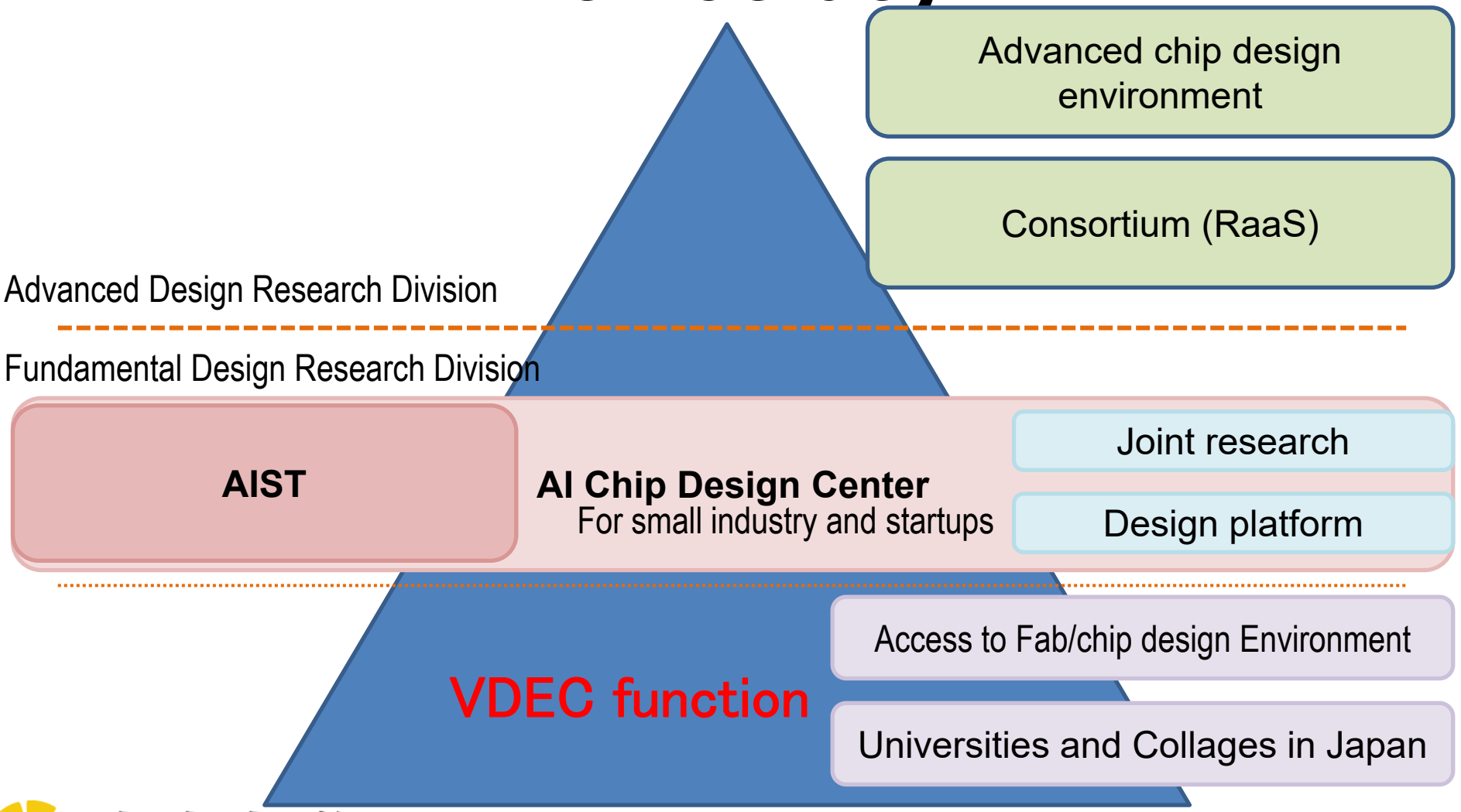
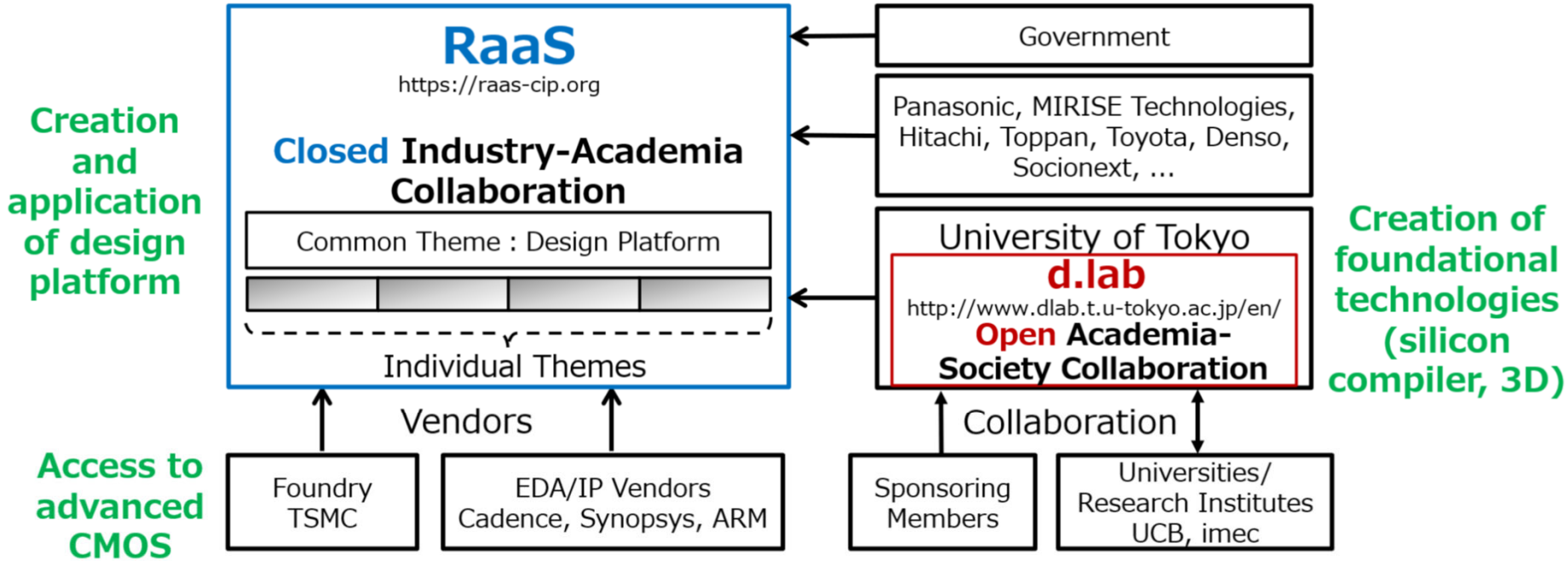
d.lab as the Center of Chip Democracy



Role of d.lab and RaaS

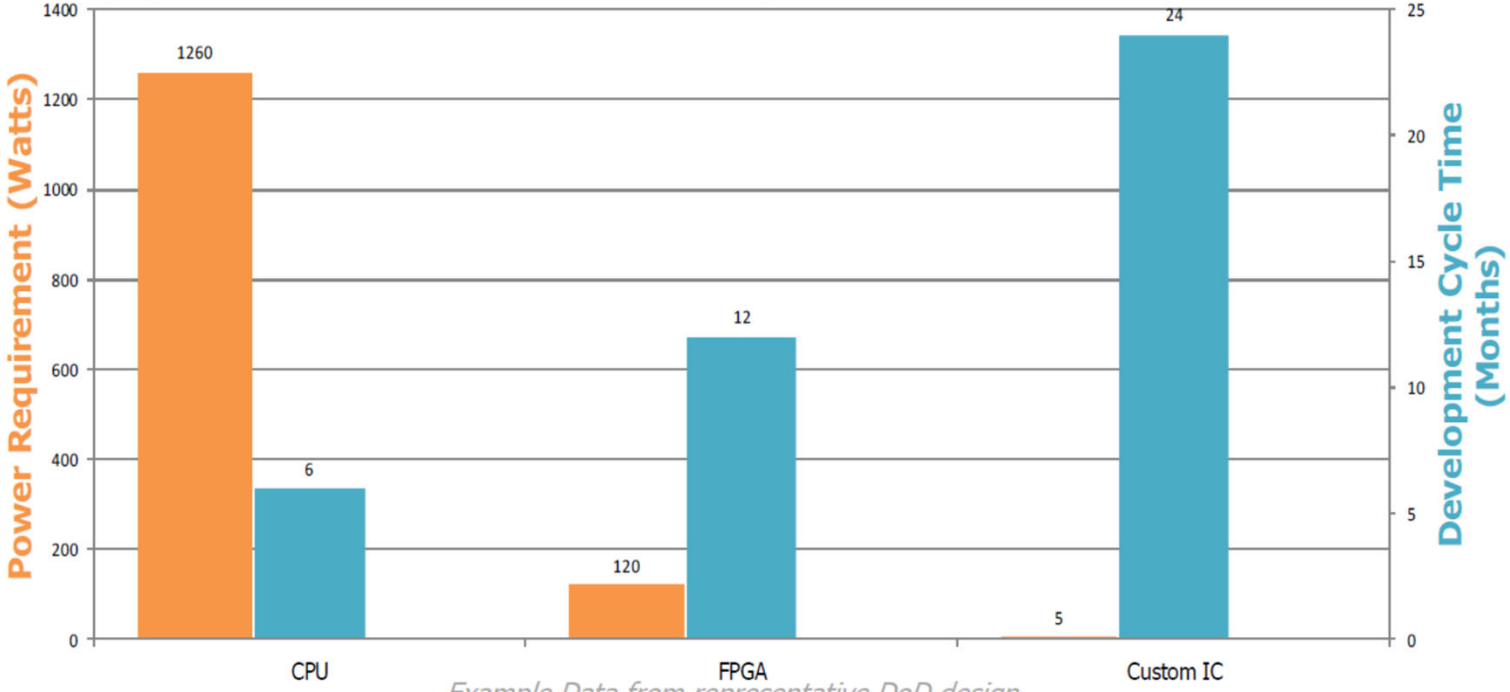
- University of Tokyo founded d.lab and RaaS to
  - Create an agile design platform and 3D integration technology
  - Enable development of specialized chips with 10-fold increase in both development efficiency (time) and energy efficiency (performance)



Courtesy by Prof. T. Kuroda

Performance versus development cycle times

Today you have to choose between performance and schedule/cost.



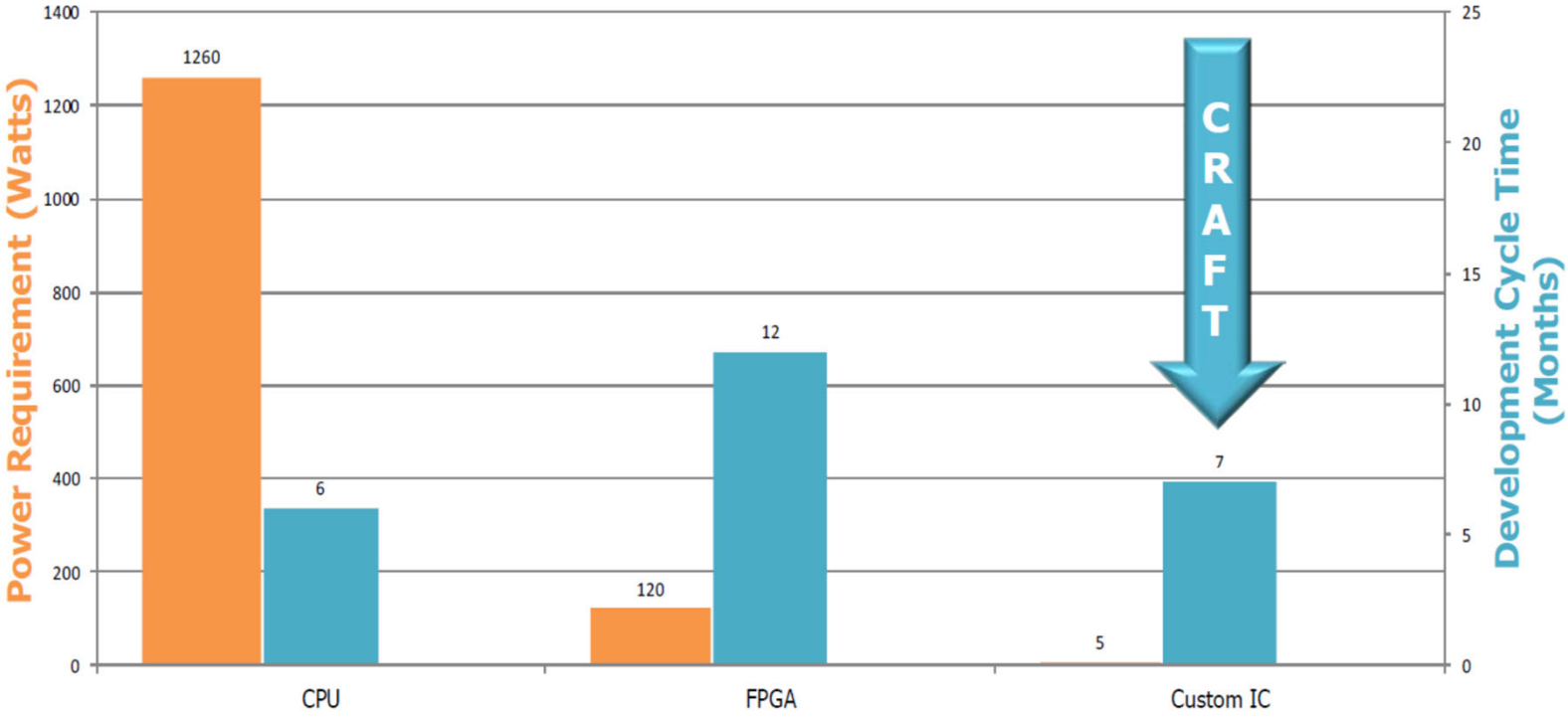
Example Data from representative DoD design

	Qty	Power Req.	Dev. Cycle Time	Current Character
General Purpose Central Processor **(CPU)**	28	**1260W**	**~6 months**	Low performance at power Flexible Quick to implement
Field Programmable Gate Array **(FPGA)**	4	**120W**	**~12 months**	Low performance at power Flexible Moderately quick to implement
Custom Integrated Circuit **(Custom IC)**	1	**5W**	**~24 months**	High performance at power Relatively inflexible Slow to implement

Performance versus development cycle times

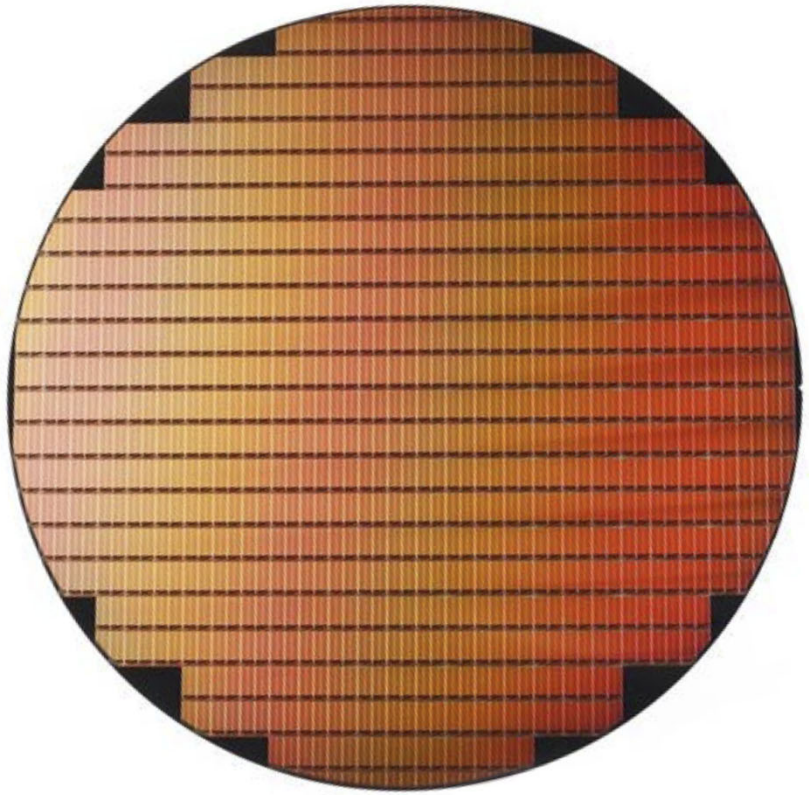
CRAFT Vision

To sharply reduce the barriers to DoD use of custom integrated circuits built using leading-edge CMOS technology while maintaining the high level of performance at power promised by this technology.



DARPA multi-project run (MPW) shuttle details

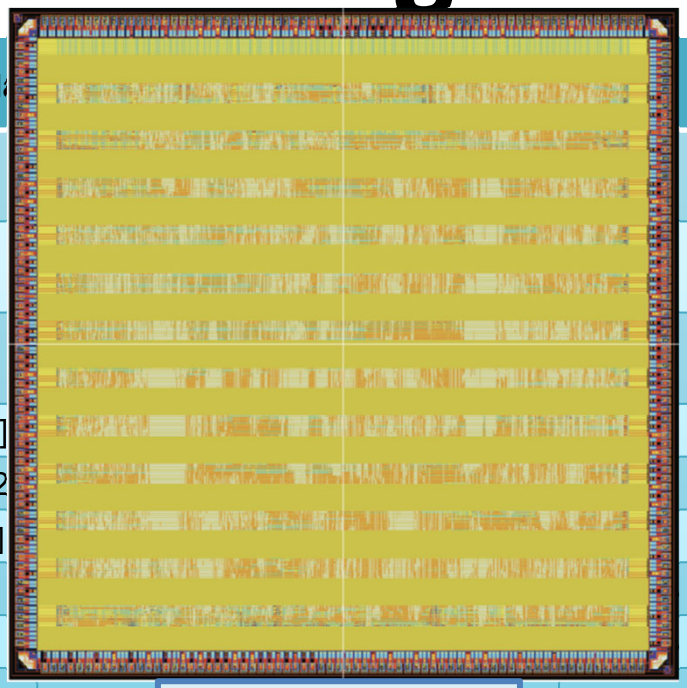
- **ALL runs available to ALL Defense Contractors**
- Wafer diameter: 300mm
- Single exposure area: 26mmX33mm
- Exposures (shots)/wafer: ~80
- Project area unit: 2.5mmX2.5mm
- Projects/shot: ~100



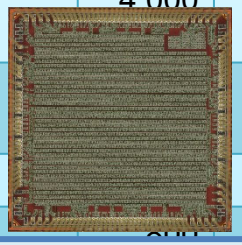
- A single FinFET process flow (TSMC 16FFC)
  - Bulk FinFET transistors with dual gate oxide
  - BEOL stack: 9 levels of Cu wiring
  - Standard passive components (no deep trench capacitor)
  - Standard eFuse blocks
  - HD and HP SRAM bit cell
- Schedule
  - PDK available: January, 2016
  - Training: May-June 2016
  - Firm shuttle commitment from users required: June, 2016
  - Design submission (GDS-In): July, 2016
  - Follow on runs 4/2017, 1/2018, 1/2019
  - Die back to users: (GDS-In + 6 months)
- Aggregator/interface/training organization
  - All questions for the foundry will go through MOSIS
  - All GDS will be sent to MOSIS
- User cost planned to be ~ $50K/project (2.5mmX2.5mm)

Design Examples

Pl				#Clk	Vdd [V]	Freq [MHz]	Tsg [us]	Pow. [mW]	E [uJ]
Mobile Device [SAC 2012]				9,909,000		1,000	9,905		
Highend PC [SCIS 2017]				840,000		4,000	210	91,000	19,110
Highend FPGA [SCIS 2017]				18,151			107		
ASIC* [CHES 2009]				5,340,400			15,800		
ASIC [A-SSCC 2012				512,541			640	255	163
ASIC* [T VLSI 2015]				330,053			521		
ASIC* [SCIS 2018]				9,270		147	202		
ASIC Ours V1+				38,911	1.4	192	203	1,200	243
ASIC Ours V2+	65		12.8	(8,			33	2,850	94.0
ASIC Ours V3+	65nm CMOS	11,726	29.7						
ASIC Ours V4++	12nm CMOS FinFET	2,300							



65nm (6mm□)



12nm (2mm□)

Area limitation

PAD & M
area limitation

Further acceleration by advance process

* Includes clock cycles for parameter / data IO

+Supporte by the New Energy and Industrial Technology Development Organization (NEDO).

++Supported by SECOM Science and Technology Foundation

東京大学 THE UNIVERSITY OF TOKYO

Systems Design Lab

Requirements on Chip design

- Increasingly higher energy efficiency
  - Customized chip
  - Advanced process
  - Advanced integration (Packaging and 3D)
- Increasingly faster design
  - HLS
  - Sophisticated IP cores

→ **Strong requirements for easy access to all of them**

Large SoC → Chiplets in PKG…

- High-speed I/O → Separated and closely integrated
- Memories → 3D integrated over processor
- Sensors → 3D integrated
- SoC will be "**Core**" + other pieces of chiplets and peripheries
  - Core: Processors + Accelerators

RISC-V as the Open Source Processor Core

高校生がebアプリをつくるかのようにSoCをさっと設計・試作してWebで販売する世界 by Philip Wong (TSMC)