RISC-V®

Instruction Sets Want to be Free

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Chairman, RISC-V Foundation;
Co-Founder and Chief Architect,
SiFive Inc.

@risc_v

Why Instruction Set Architecture matters

- **Why can't Intel sell mobile chips?**
  - 99%+ of mobile phones/tablets based on ARM v7/v8 ISA
- **Why can't ARM partners sell servers?**
  - 99%+ of laptops/desktops/servers based on AMD64 ISA (over 95%+ built by Intel)
- **How can IBM still sell mainframes?**
  - IBM 360, oldest surviving ISA (50+ years)

ISA is most important interface in computer system

where software meets hardware

Open Interfaces Work for Software!

Field	*Open Standard*	*Free, Open Implement.*	*Proprietary Implement.*
Networking	Ethernet, TCP/IP	Many	Many
OS	Posix	Linux, FreeBSD	M/S Windows
Compilers	C	gcc, LLVM	Intel icc, ARMcc
Databases	SQL	MySQL, PostgresSQL	Oracle 12C, M/S DB2
Graphics	OpenGL	Mesa3D	M/S DirectX
ISA	??????	----------	x86, ARM, IBM360

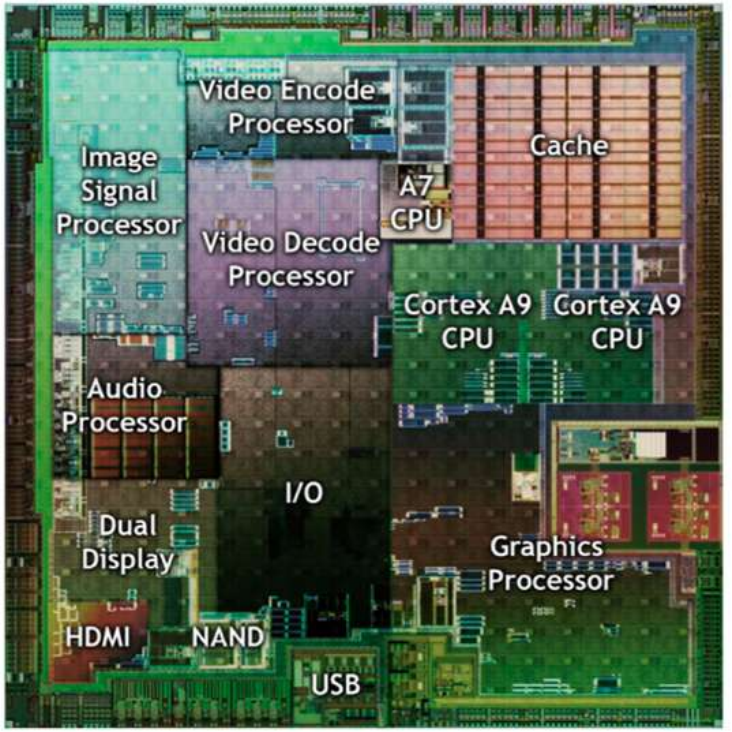
- Why not successful free & open standards and free & open implementations, like other fields?

Companies and their ISAs Come and Go

- Digital Equipment Corporation, RIP! (**PDP-11**, **VAX**, **Alpha**)
- Intel's dead ISAs (**i960**, **i860**, **Itanium, …**)
- **SPARC**
  - Sun opened v8 as IEEE 1754-1994, acquired by Oracle, all closed down
- **MIPS**
  - Sold to Imagination, bought by Wave
  - Opened up MIPS R6 ISA in 2018, then made not open in 2019
- **IBM POWER**
  - Initially proprietary, now ISA opened as OpenPower
- **ARM**
  - Sold to Softbank at >40% premium in 2016
  - Nvidia now acquiring ARM

Today, many ISAs on one SoC

- Applications processor (usually ARM)
- Graphics processors
- Image processors
- Radio DSPs
- Audio DSPs
- Security processors
- Power-management processor
- *> dozen ISAs on some SoCs – each with unique software stack*



NVIDIA Tegra SoC

Why?

- Apps processor ISA too big, inflexible for accelerators
- IP bought from different places, each proprietary ISA
- Engineers build home-grown ISA cores

Do we need all these different ISAs?

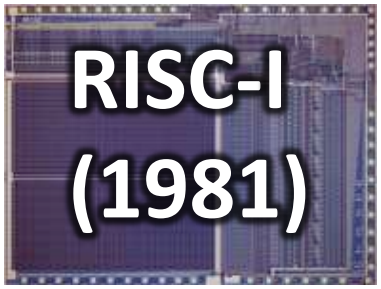
Must they be proprietary?

Must they keep disappearing?

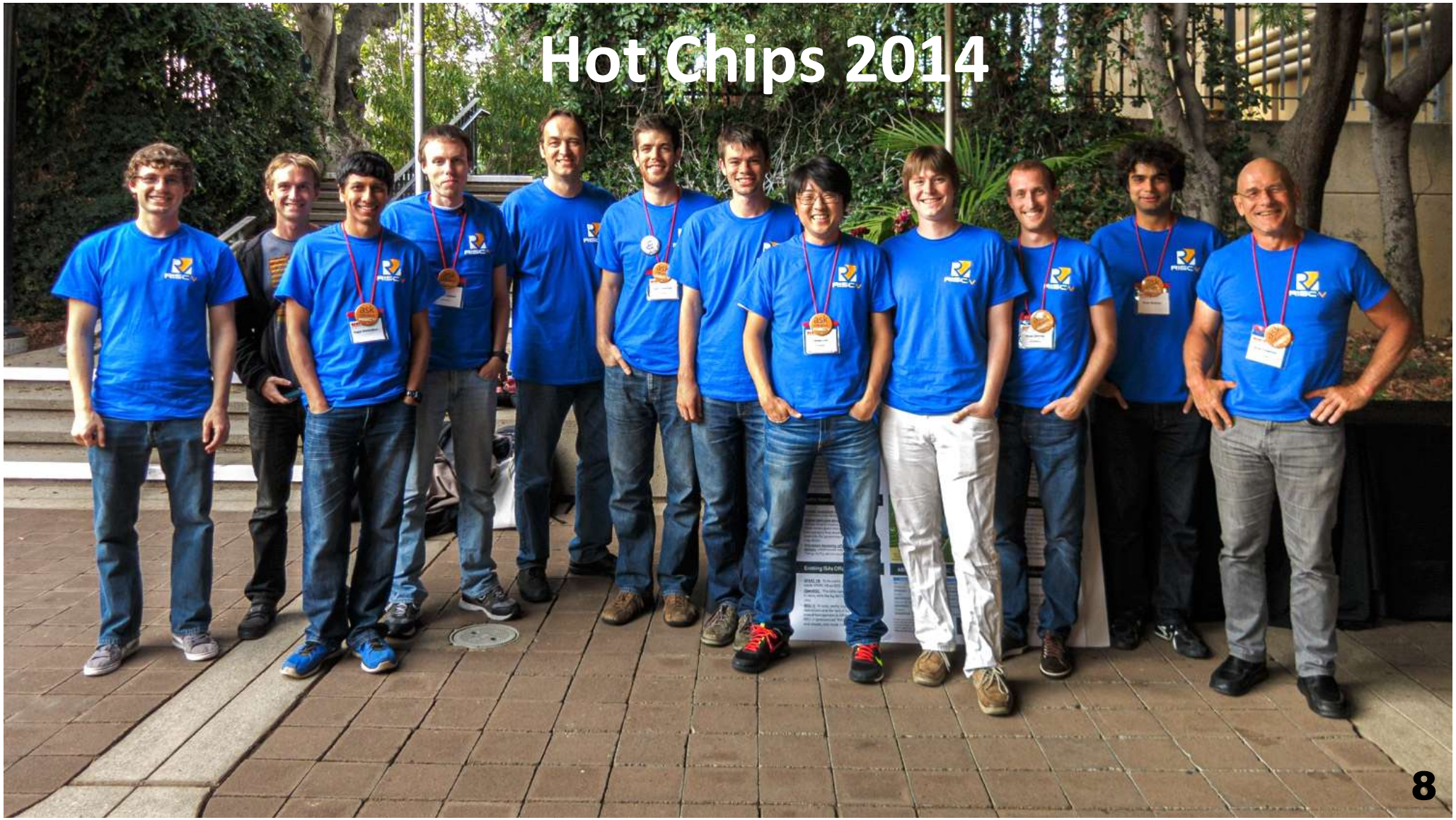
What if there was one stable free and open ISA everyone could use for everything?

RISC-V Background

- In 2010, after many years and many research projects using MIPS, SPARC, and x86, time for architecture group at UC Berkeley to choose ISA for next set of projects
- Obvious choices: x86 and ARM
  - x86 impossible – too complex, IP issues
  - ARM mostly impossible – complex, no 64-bit in 2010, IP issues
- So we started "3-month project" during summer 2010 to develop clean-slate ISA
  - Principal designers: Andrew Waterman, Yunsup Lee, David Patterson, Krste Asanovic
- Four years later, May 2014, released frozen base user spec
  - many tapeouts and several research publications along the way
- Name RISC-V (pronounced "risk-five") represents fifth major Berkeley RISC ISA



Hot Chips 2014



RISC-V International

- **RISC-V** is the open-source hardware Instruction Set Architecture (ISA)
- Frozen base user spec released in 2014, contributed, ratified, and openly published by RISC-V International

RISC-V International is a non-profit entity serving members and the industry

Our mission is to accelerate RISC-V adoption with shared benefit to the entire community of stakeholders.

- ✓ Drive progression of **ratified specs, compliance suite, and other technical deliverables**
- ✓ **Grow the overall ecosystem / membership**, promoting diversity while preventing fragmentation
- ✓ Deepen **community engagement and visibility**

CHINA

MORE THAN 200 MEMBERS HAVE JOINED THE CRVA AND CRVIC ASSOCIATIONS AS WELL AS 33 MEMBERS IN THE GLOBAL RISC-V FOUNDATION. ACROSS 2019 WE'VE LED DISCUSSIONS IN 6 CITIES AS WELL AS HOSTED A DAY OF TALKS AT THE WORLD INTERNET CONFERENCE. IN NOVEMBER, WE HOSTED 500 ATTENDEES AT THE CHINA RISC-V FORUM.

EUROPE

THE EUROPEAN PROCESSOR INITIATIVE HAS DECLARED RISC-V AS A KEY ARCHITECTURE FOR THE NEXT GENERATION OF HPC PROCESSORS AND SYSTEMS, FOCUSED ON ACCELERATION.

INDIA

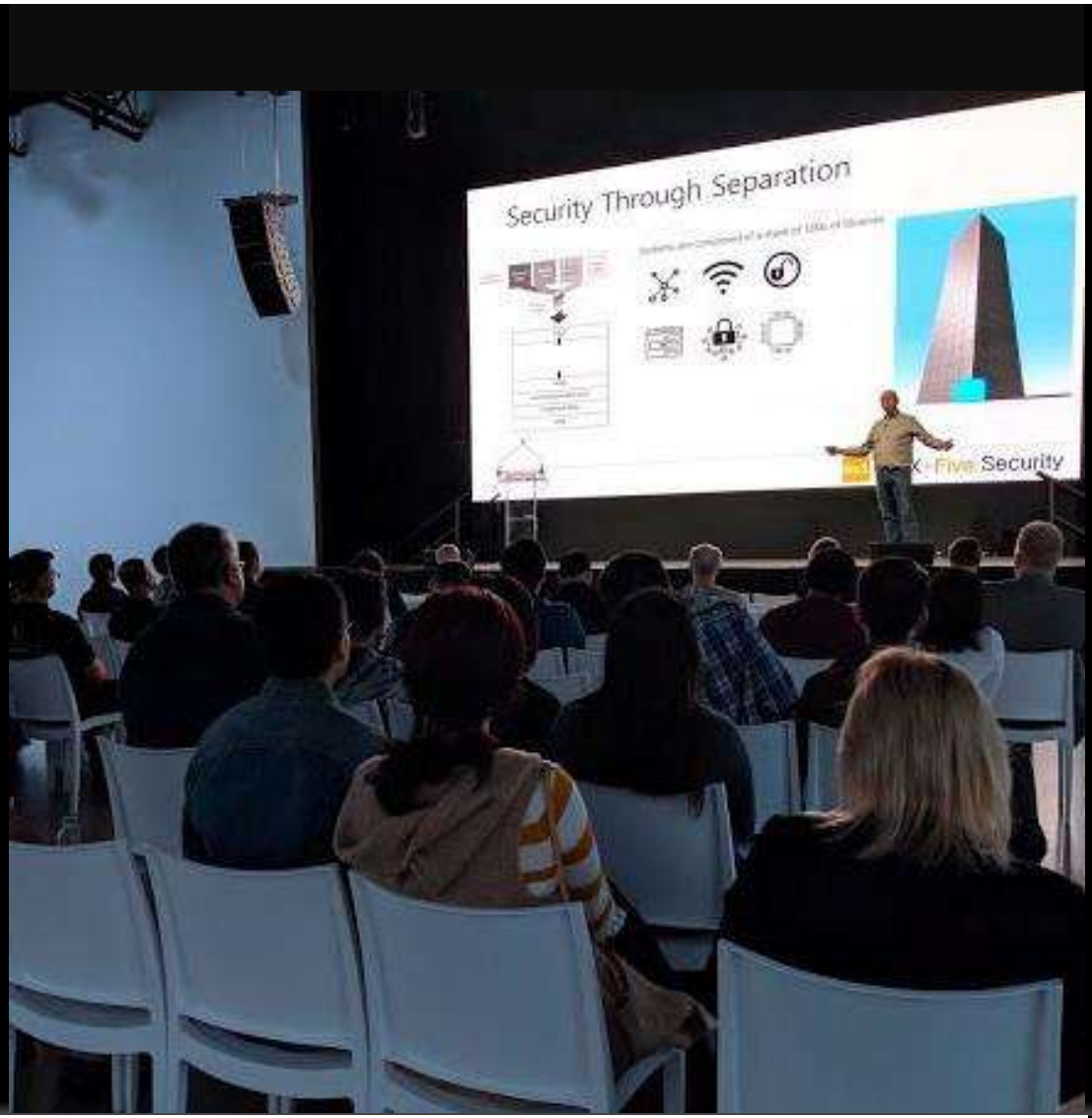
2014 WITH THE FUNDING OF 6 RISC-V PROCESSORS THROUGH THE SHAKTI PROJECT, RISC-V HAS BEEN WIDELY DECLARED THE NATIONAL ARCHITECTURE OF INDIA.

JAPAN

MOMENTUM IS CONTINUING TO GROW IN OUR ENGAGEMENT AND EVENTS WITH A 50% JUMP AT OUR 2019 TOKYO DAY TO 360 REGISTERED ATTENDEES.

NORTH AMERICA

NORTH AMERICA. INDUSTRY ADOPTION HAS TAKEN OFF WITH MILLIONS OF CORES SHIPPING FROM NVIDIA, WESTERN DIGITAL, SIFIVE, AND OTHERS.



PAKISTAN

ON THE ROAD TO DECLARING RISC-V THEIR NATIONAL ARCHITECTURE, TWO OF THE BIGGEST GATHERINGS EVER OF 3000+ IN PAKISTAN FOR TWO SIFIVE TECH SYMPOSIUMS – OCT 2019


Arilinc
astc
antmicro
aselsan
Allwinner
Alibaba.com
AdaCore
adafruit
Airavath Foundation
APEXMIC
GRADIENT
ASHLING
AIST
Baylibre
Berkeley Architecture Research
BITMAIN
bluespec
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BOSTON UNIVERSITY
BAE SYSTEMS
सी डैक CDAC
cadence
Cortus
सी डैक CDAC अॅक्टस acts
cea
Centipede
CEVA
CLEMSON
CloudBEAR
COBHAM
DATA 61
csem
codasip
Collins Aerospace
CRYPTAPE
CPSEC
DOVER MICROSYSTEMS
RISC-V
DRAPER
dxcorr
EMBECOSM
EMBALO TECHNOLOGIES
Esperanto TECHNOLOGIES
ESPRESSIF
ETH zürich
expresslogic
oculus
FORTH
galois
GENESYS
GHELIA
GigaDevice
GOLDEN GATE UNIVERSITY
Google
GOWIN
GREENWAVES
TU Graz
HENSOLDT
Hewlett Packard Enterprise
HEX-Five Security
HIGO 海阔
HITACHI Inspire the Next
Honeywell
HORTONWORKS
HUAWEI
huami
IAR SYSTEMS
IBM
ICT
IDT Integrated Device Technology
Imagination
imperas
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君正 Ingenic
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ISCAS
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KU LEUVEN
LATTICE
LAUTERBACH DEVELOPMENT TOOLS
lowRISC
MEDIATEK
Mellanox
Mentor A Siemens Business
MICROCHIP
MIT CSAIL
Microsemi Power Matters.
MOSIS
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ORION 猎户星空
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PerfXLab 湃峰科技
Pacific Northwest NATIONAL LABORATORY
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SANECHIPS 中兴微电子
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SHC SH CONSULTING
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Syntronix
Semiconductor Investment
SYZEXION
Tactical Computing Labs
TechaneLye
Technolution
Telink
KTrustKernel 上海瓶钵信息科技有限公司
THALES
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ultraSoC
云知声 Unisound
東京大学 THE UNIVERSITY OF TOKYO
University of BRISTOL
UPPSALA UNIVERSITET
KU
VectorBlox
VeriSilicon
创景科技
Western Digital
WIND RIVER
WIT
XILINX
XtremeEDA
ZeroPoint
信大捷安

More than 435 RISC-V Members

across 33 Countries Around the World

44 Chip
SoC, IP, FPGA

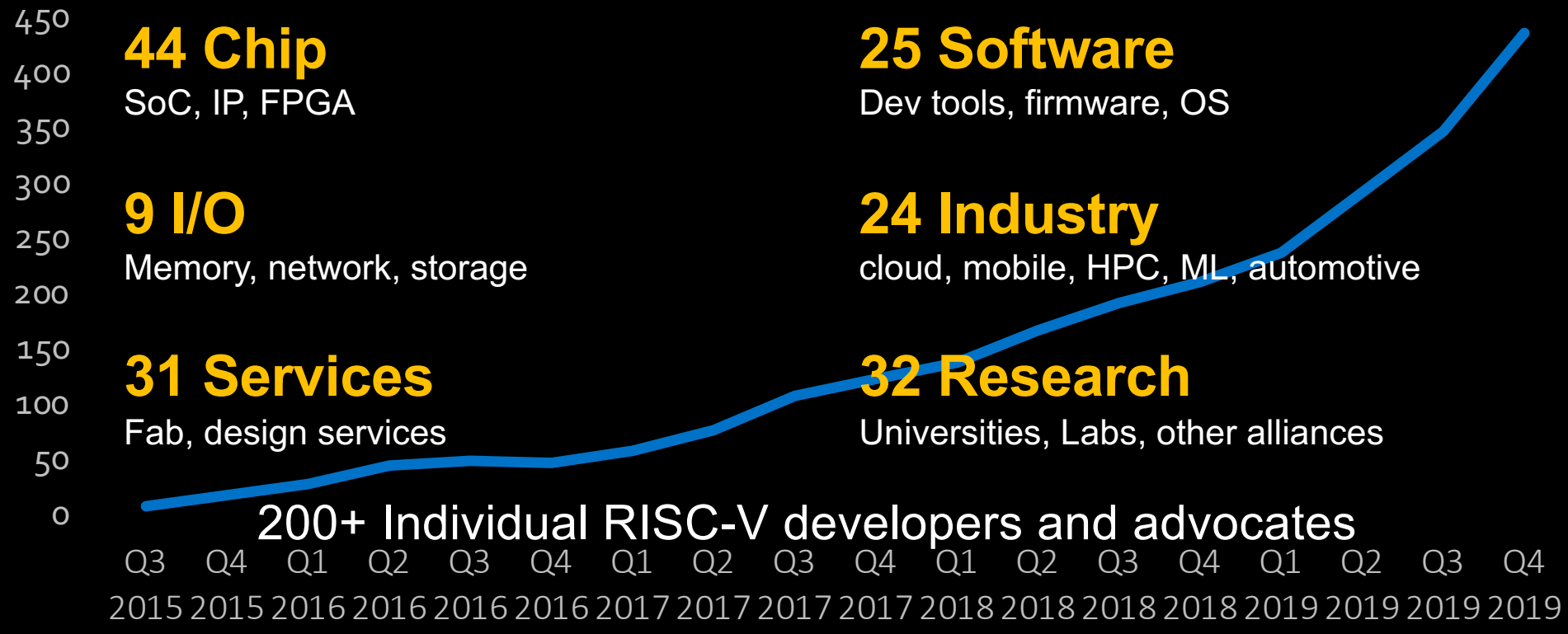
25 Software
Dev tools, firmware, OS

9 I/O
Memory, network, storage

24 Industry
cloud, mobile, HPC, ML, automotive

31 Services
Fab, design services

32 Research
Universities, Labs, other alliances



RISC-V Ecosystem

Software

Open-source software:
Gcc, binutils, glibc, Linux, BSD, LLVM, QEMU, FreeRTOS, ZephyrOS, LiteOS, SylixOS, …

Proprietary software:
Lauterbach, Segger, IAR, Micrium, ExpressLogic, Ashling, Imperas, AntMicro, …

RISC-V International

ISA specification | Golden Model | Compliance

Hardware

Open-source cores:
Rocket, BOOM, RI5CY, Ariane, PicoRV32, Piccolo, SCR1, Swerv, Hummingbird, …

Proprietary core providers:
Alibaba, Andes, Bluespec, Cloudbear, Codasip, Cortus, InCore, Nuclei, SiFive, Syntacore, …

Inhouse cores:
Nvidia, WDC, Alibaba, +others

What's Different about RISC-V?

- *Simple*
  - Far smaller than other commercial ISAs
- *Clean-slate design*
  - Clear separation between user and privileged ISA
  - Avoids µarchitecture or technology-dependent features
- *Modular* ISA designed for *extensibility/specialization*
  - Small standard base ISA, with multiple standard extensions
  - Sparse &variable-length instruction encoding for vast opcode space
- *Stable*
  - Base and first standard extensions are frozen
  - Additions via optional extensions, not new versions
- *Community designed*
  - Developed with leading industry/academic experts and software developers

Engaged engineers are domain experts

Drive technical priorities in 20+ focus areas

Compliance

Technical Deliverables

Opcode Space Mgmt Standing Committee

Software Standing Committee

Base ISA Ratification Task Group

Privileged ISA Spec Task Group

UNIX-Class Platform Spec Task Group

Formal Specification Task Group

Trusted Execution Env Spec Task Group

B Extension (Bit Manipulation) Task Group

J Extension (Dynam. Translated Lang) Task Group

P Extension (Packed-SIMD Inst) Task Group

V Extension (Vector Ops) Task Group

Cryptographic Extension Task Group

Debug Specification Task Group

Fast Interrupts Spec Task Group

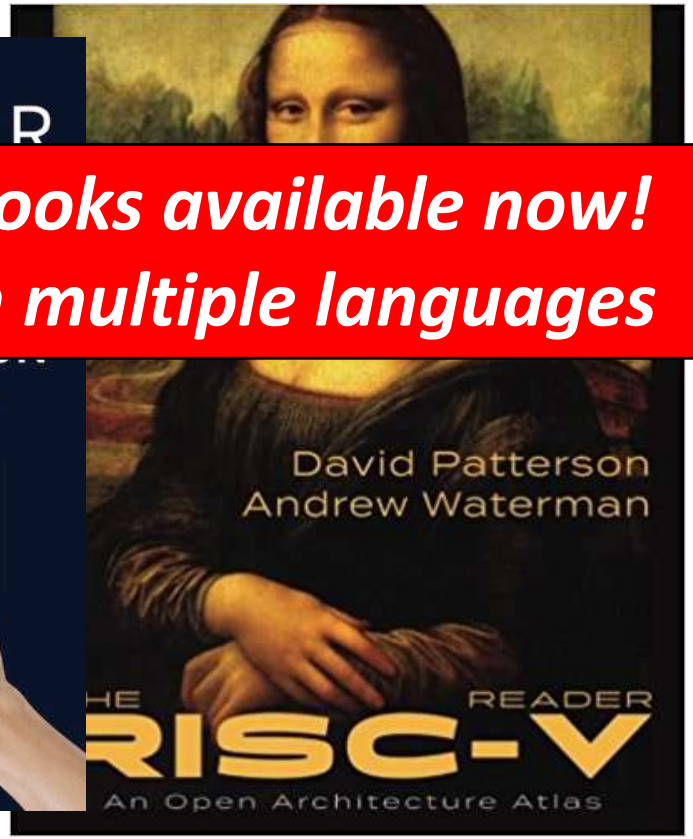
Memory Model Spec Task Group

Processor Trace Spec Task Group

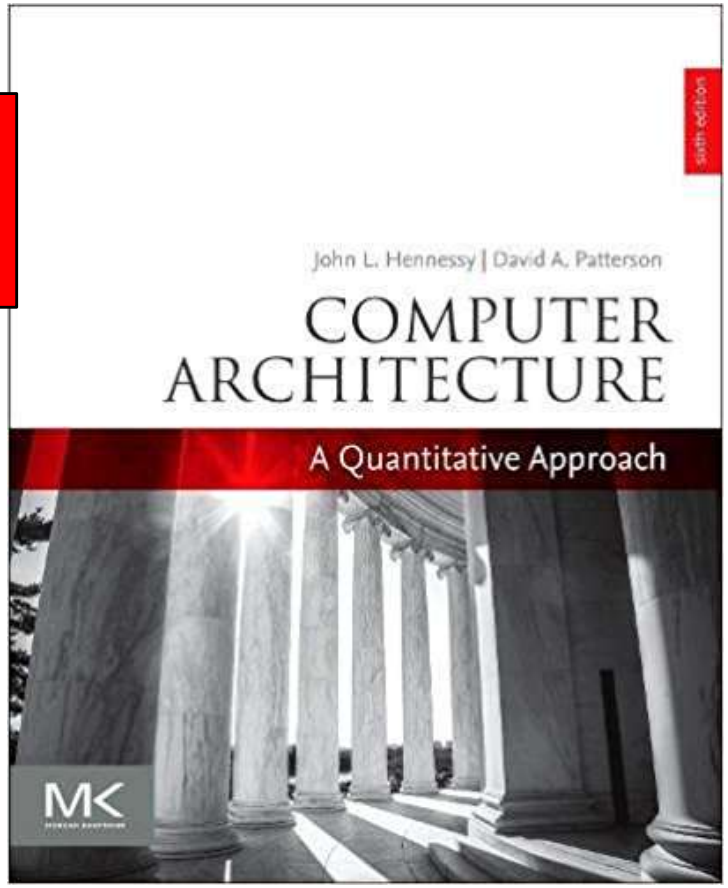
Compliance Task Group

+ Security Committee, HPC Special interest group, soft-core SIG, and Safety Task Group

RISC-V in Education



Books available now!
In multiple languages



RISC-V spreading quickly throughout curricula of top schools

Why is RISC-V so popular?

- Engineers sometimes "*don't see forest for the trees*"
- The movement is ***not*** happening because some benchmark ran 10% faster, or some implementation was 30% lower power
- The movement ***is*** happening because ***new business model*** changes everything
  - Pick ISA first, then pick vendor or build own core
  - Add your own extension without getting permission
- Implementation features/PPA will follow
  - Whatever is broken/missing in RISC-V will get fixed

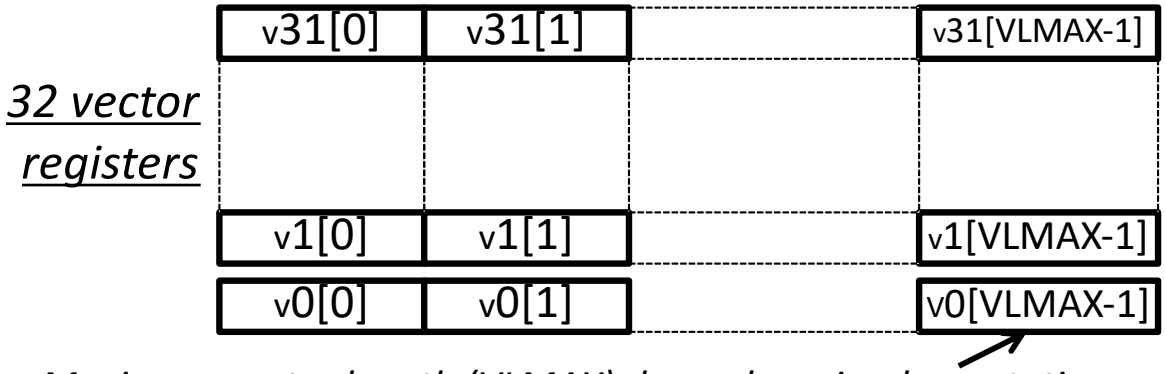
Modest RISC-V Project Goal

Become the industry-standard ISA for all computing devices

RISC-V and Domain-Specific Compute

- RISC-V originally designed for research into application-specific processors
- Small base, sufficient to run full C compiler and software stack
- Provides minimal “skeleton” on which to hang domain-specific extensions
- No “permission” needed to build your own extension

RISC-V Vector Extension (RVV) Overview



Maximum vector length (VLMAX) depends on implementation, number of vector registers used, and type of each element.

- Unit-stride, strided, scatter-gather, structure load/store instructions
- Rich set of integer, fixed-point, and floating-point instructions
- Vector-vector, vector-scalar, and vector-immediate instructions
- Multiple vector registers can be combined to form longer vectors to reduce instruction bandwidth or support mixed-precision operations (e.g., 16b*16b->32b multiply-accumulate)
- Designed for extension with custom datatypes and widths

Vector CSRs

vtype

Vtype sets width of element in each vector register (e.g., 16-bit, 32-bit, …)

vl

Vector length CSR sets number of elements active in each instruction

vstart

Resumption element after trap

vcsr (vxrm/vxsat)

Fixed-point rounding mode and saturation flag fields in vector CSR

Some RVV Design Points

Name	Issue Policy	Issue Width	VLEN (bits)	Datapath (bits)	VLEN/Datapath (beats)
Smallest	InO	1	32	32	1
Simple	InO	1	512	128	4
InO-Spatial	InO	2	128	128	1
OoO-Spatial	OoO	2-3	128	128	1
OoO-Temporal	OoO	2-3	512	128	4
OoO-Server	OoO	3-6	2048	512	4
OoO-HPC	OoO	3-6	16384	2048	8

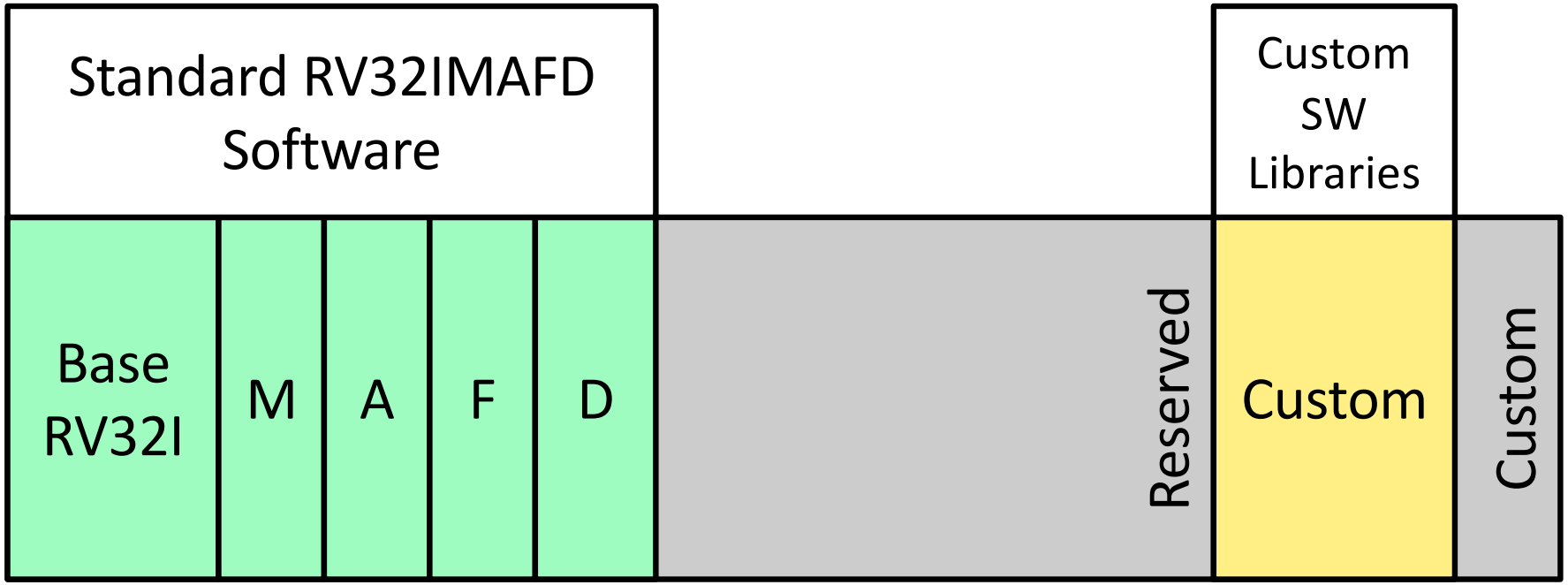
RISC-V Encoding Terminology

Standard: defined by the Foundation

Reserved: Foundation might eventually use this space for future standard extensions

Custom: Space for implementer-specific extensions, never claimed by Foundation

RISC-V Custom Extension Example



Fragmentation versus Diversity

Fragmentation:

Same thing done different ways

Diversity:

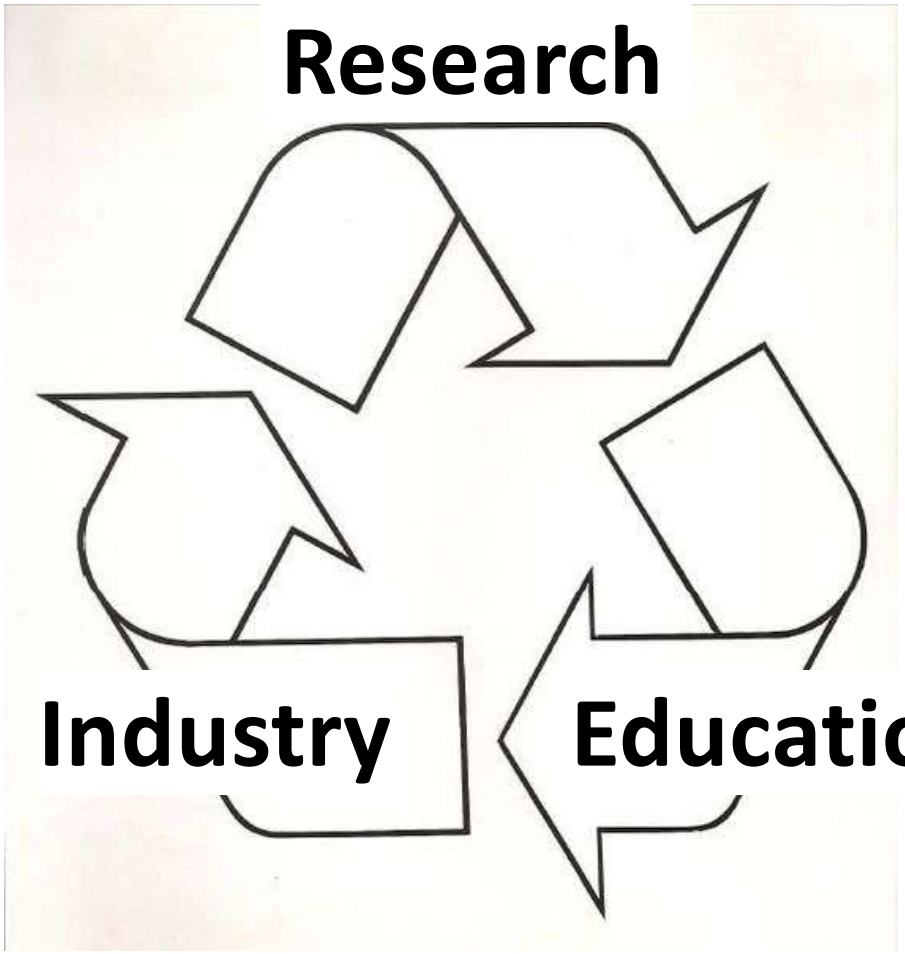
Solving different problems

How is RISC-V Avoiding Fragmentation?

Two powerful forces keep fragmentation at bay:

- **Users**: No one wants a repeat of vendor lock-in.
- **Software**: No one, not even nation state, can afford their own software stack. Upstream open-source projects only accept frozen/ratified Foundation standards.

RISC-V: Completing the Innovation Cycle



Open ecosystem is key to keeping the virtuous cycle going