RISC-Vプロセッサ向けALUとレジスターの3重実装の設計例

Design example of a triple modular redundancy ALU and a register file for RISC-V processors

磯邊 雅人[†] 渡邊 実[††] 渡邊 誠也[††]

Masato Isobe Minoru Watanabe Nobuya Watanabe

[†]岡山大学工学部情報系学科 [††]岡山大学学術研究院環境生命自然科学学域

[†]Okayama University Department of Information Technology [††]Okayama University Environmental, life, Natural, Science and Technology

あらまし

宇宙空間や原子力発電所などの放射線の強い場所では，プロセッサには放射線に対する耐性が求められる．既存のプロセッサは放射線に対して極めて脆弱であり，強い放射線環境下では急激に劣化し，故障に至る．

そこで我々は放射線に対する耐性を上げるためにプロセッサの三重化実装に取り組んでいる．本稿ではその設計例を示す．

Abstract

Under a strong radiation environment such as space and nuclear power plants, processors must have high-radiation tolerance. Currently available processors are always weak for radiation and are easily broken by radiation for a short period. Therefore, we have been developing a triple-modular-redundant processor to increase the radiation tolerance. This poster presents one design example for an Arithmetic Logic Unit (ALU) and a register file.

・研究の背景（Research Background）

3重化実装は通常、ソフトエラー対策として用いられるが、ここではトータルドーズ耐性の改善を目的として実装を試みた．

Although TMR is always used for increasing soft-error tolerance, here, in order to increase the total-ionizing-dose tolerance of a processor, we have introduced triple modular redundancy (TMR) for ALU and register file of the processor.

・通常のレジスタファイルの設計(Design of a normal register-file)

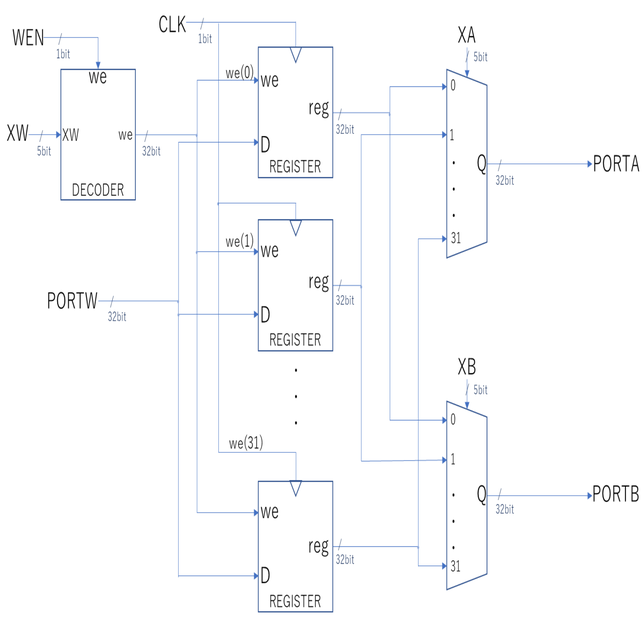

Fig. 1: Block diagram of a normal register consisting of register cells.

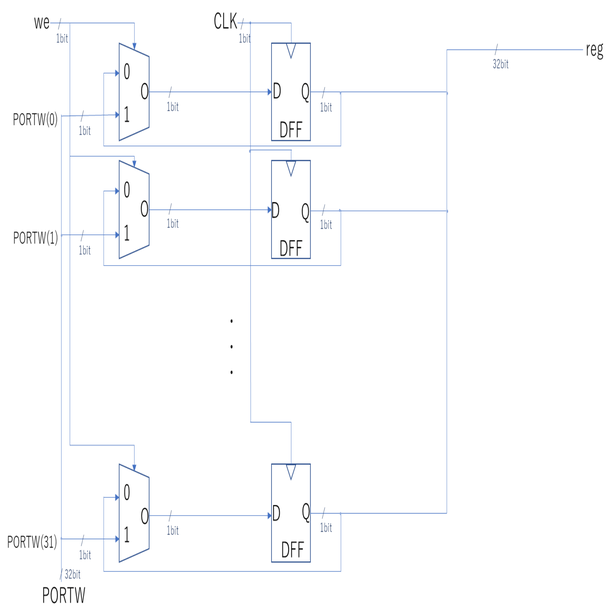

Fig. 2: Block diagram of a register cell.

耐放射線設計されていない普通のレジスタファイルのブロック図を図1，図2に示す．この場合，一か所でも故障すれば動作不良に至る．

Figures 1 and 2 show the block diagram of a normal register-file. In the register-file, if one transistor is broken, the function is down.

・三重化レジスタファイルの設計（Design of a triple modular redundancy register-file）

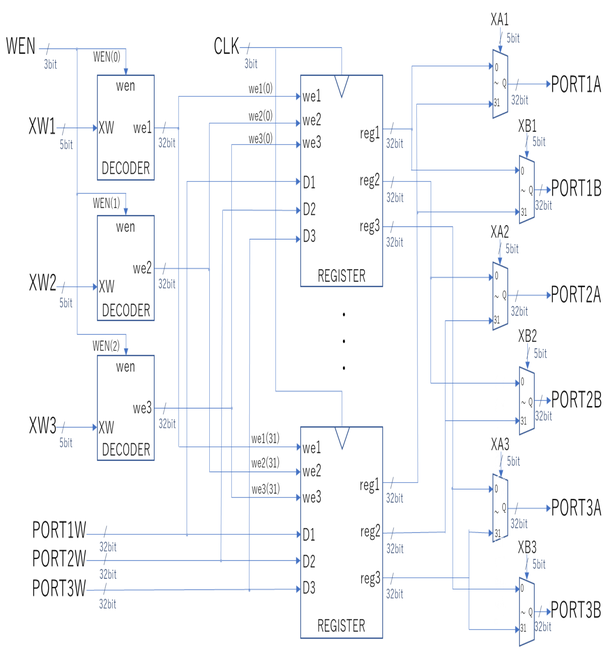

Fig. 3: Block diagram of triple modular redundancy (TMR) register-file.

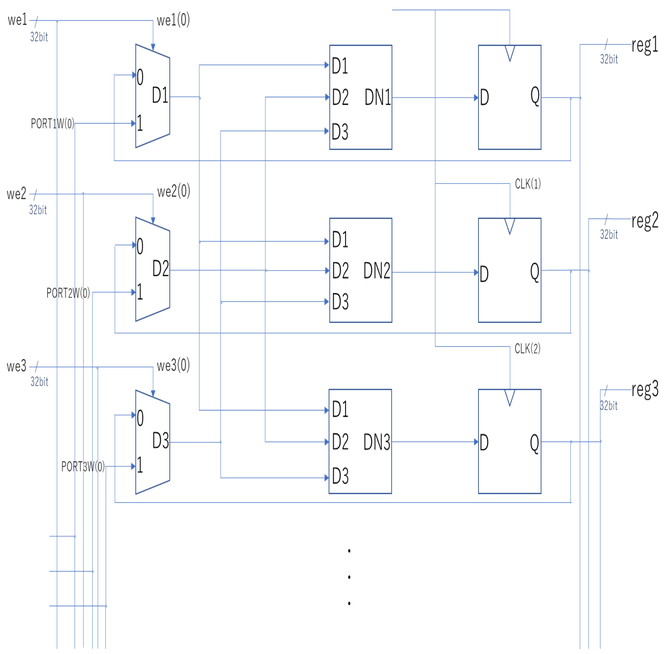

Fig. 4: Block diagram of a TMR register cell.

三重化レジスタファイルの設計例を図3，4に示す．三重化レジスタセルは多数決回路、D-flip-flop、セレクタから構成される．1モジュールが故障しても，そのまま継続利用することが可能である．図4にそれらを用いた3重化レジスタファイルのブロック図を示す．

Figures 3 and 4 show the block diagram of a triple modular redundancy register file. A triple modular redundant register cell consists of majority voting circuits, flop-flops, and selectors. At every clock cycles, the majority voting operation is automatically executed on the circuit. The entire triple modular redundancy register file was constructed by using the triple modular redundant register cells.

・三重化ALU (Triple-modular-redundant ALU)

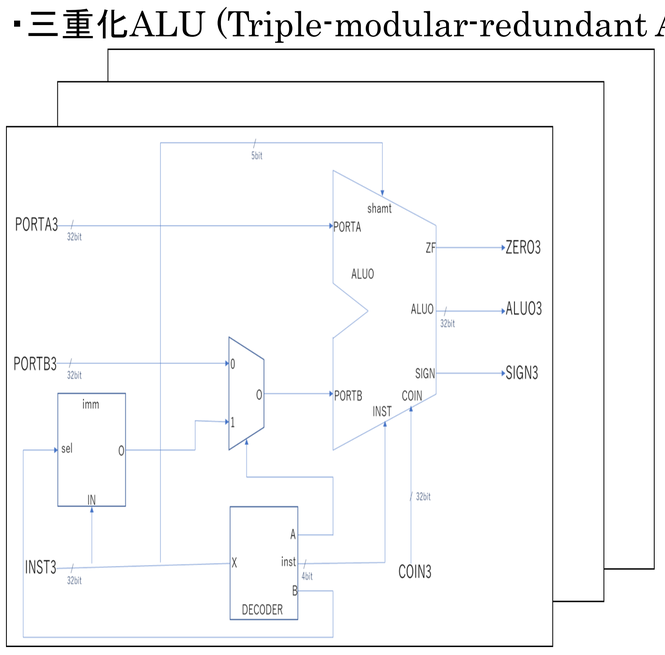

Fig. 5: Triple modular redundant ALU design.

imm[31:12]				rd	0110111	LUI
imm[31:12]				rd	0010111	AUIPC
imm[20|10:1|11|19:12]				rd	1101111	JAL
imm[11:0]		rs1	000	rd	1100111	JALR
imm[12|10:5]	rs2	rs1	000	imm[4:1|11]	1100011	BEQ
imm[12|10:5]	rs2	rs1	001	imm[4:1|11]	1100011	BNE
imm[12|10:5]	rs2	rs1	100	imm[4:1|11]	1100011	BLT
imm[12|10:5]	rs2	rs1	101	imm[4:1|11]	1100011	BGE
imm[12|10:5]	rs2	rs1	110	imm[4:1|11]	1100011	BLTU
imm[12|10:5]	rs2	rs1	111	imm[4:1|11]	1100011	BGEU
imm[11:0]		rs1	000	rd	0000011	LB
imm[11:0]		rs1	001	rd	0000011	LH
imm[11:0]		rs1	010	rd	0000011	LW
imm[11:0]		rs1	100	rd	0000011	LBU
imm[11:0]		rs1	101	rd	0000011	LHU
imm[11:5]	rs2	rs1	000	imm[4:0]	0100011	SB
imm[11:5]	rs2	rs1	001	imm[4:0]	0100011	SH
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	SW
imm[11:0]		rs1	000	rd	0010011	ADDI
imm[11:0]		rs1	010	rd	0010011	SLTI
imm[11:0]		rs1	011	rd	0010011	SLTIU
imm[11:0]		rs1	100	rd	0010011	XORI
imm[11:0]		rs1	110	rd	0010011	ORI
imm[11:0]		rs1	111	rd	0010011	ANDI
0000000	shamt	rs1	001	rd	0010011	SLLI
0000000	shamt	rs1	101	rd	0010011	SRLI
0100000	shamt	rs1	101	rd	0010011	SRAI
0000000	rs2	rs1	000	rd	0110011	ADD
0100000	rs2	rs1	000	rd	0110011	SUB
0000000	rs2	rs1	001	rd	0110011	SLL
0000000	rs2	rs1	010	rd	0110011	SLT
0000000	rs2	rs1	011	rd	0110011	SLTU
0000000	rs2	rs1	100	rd	0110011	XOR
0000000	rs2	rs1	101	rd	0110011	SRL
0100000	rs2	rs1	101	rd	0110011	SRA
0000000	rs2	rs1	110	rd	0110011	OR
0000000	rs2	rs1	111	rd	0110011	AND

Fig. 6: RISC-V instruction set.

図5に三重化されたALUのブロック図を示す．2つ同じセルが実装されている以外，通常のALUと同じデザインである．多数決演算は実装しておらず、ALUにライトバックされる時に自動的に多数決が行われるデザインとしている．

Figure 5 shows a triple-modular redundant ALU design. The ALU includes three ALU units which is same as a normal RISC-V ALU. Although the calculations on the triple-modular redundant ALU never include any majority voting operation, the majority voting operation is executed automatically when the calculation result is written back to the register-file.

・三重化レジスタのシミュレーション結果(Simulation result of the triple-modular-redundancy register-file)

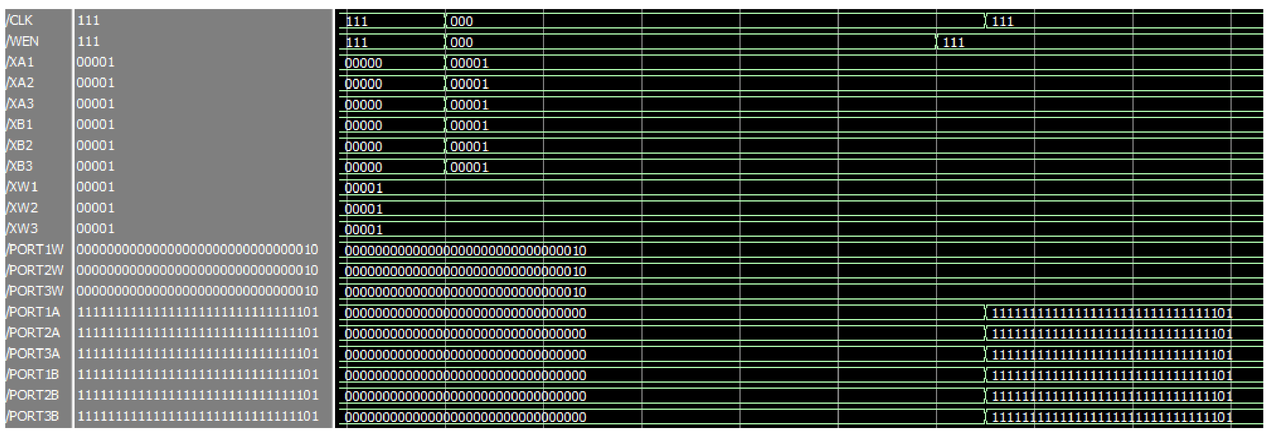

Fig. 7: Simulation result of the triple-modular-redundancy register-file .implementation test results.

図7は三重化レジスタのシミュレーション結果である．正しい動作を確認した．

Figure 7 shows the simulation result of the triple-modular-redundancy register-file. The correct operations could be confirmed.

・三重化ALUのシミュレーション結果（ Simulation result of the triple-modular-redundant ALU）

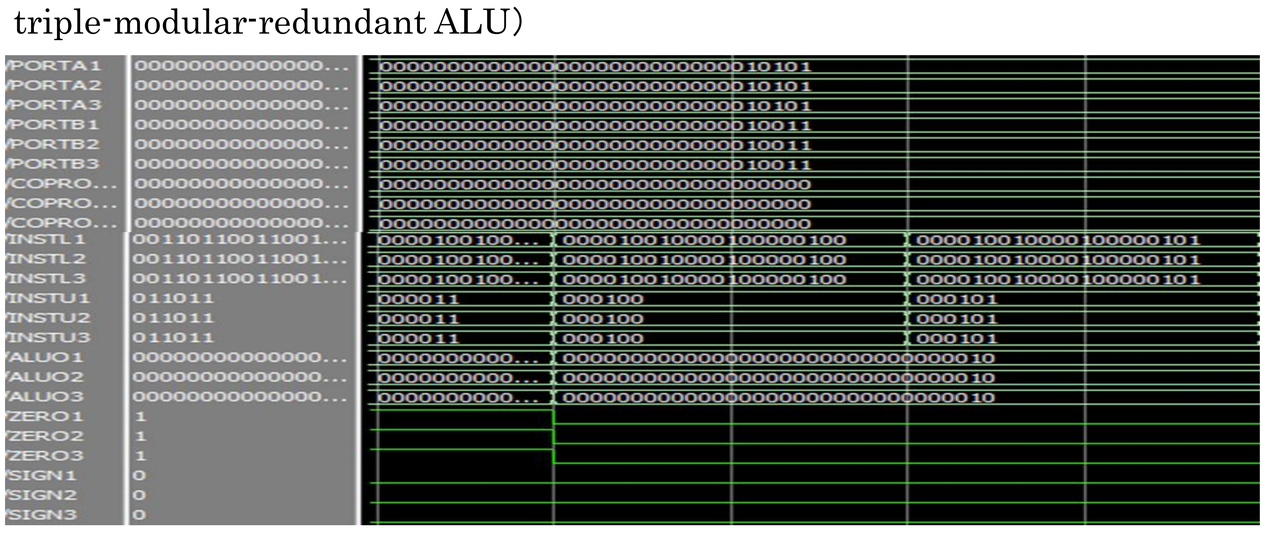

Fig. 8: Simulation result of the triple-modular-redundant ALU.

図8は三重化ALUのシミュレーション結果である．正しい動作を確認した．

Figure 8 shows the simulation result of the triple-modular-redundant ALU. The correct operations could be confirmed.