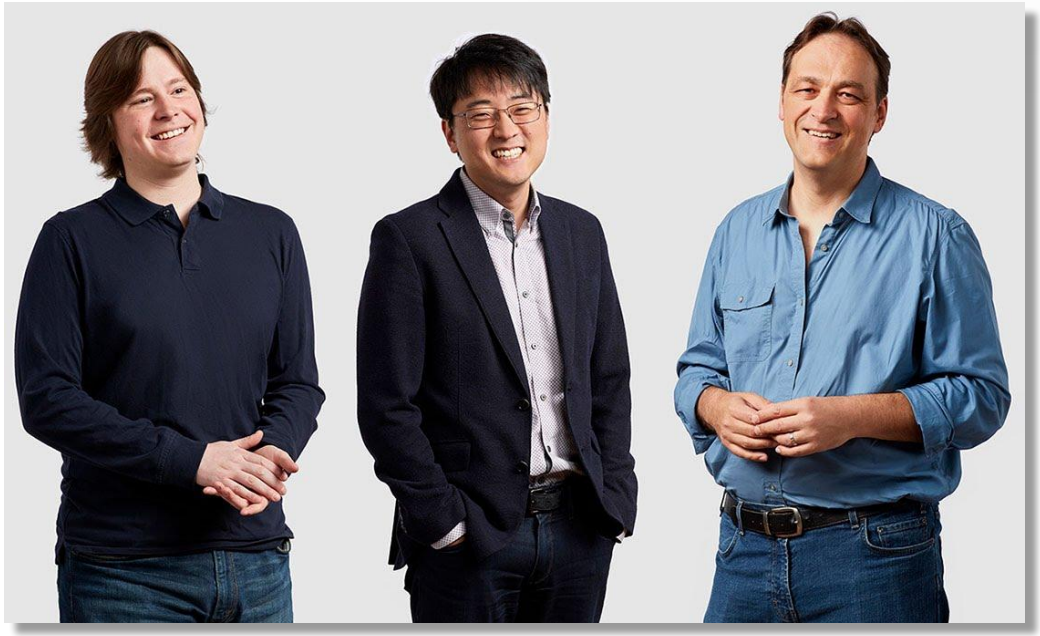
SiFive

The future of RISC-V has no limits

May 31, 2022

Leading the RISC-V revolution



We invented RISC-V

SiFive's founders are the same UC Berkeley professor and PhDs who invented and have been leading the commercialization of the RISC-V Instruction Set Architecture (ISA) since 2010

GSA 2018 Awards

GSA 2019 AWARDS Winner

GSA 2020 Most Respected Private Semiconductor Company

2018, 2019, 2020: SiFive Recognized as Most Respected Private Semiconductor Company

SiFive global presence

Presence

- 10+ Offices
- 600+ Employees (420+ Engineers)
- 375+ Tapeouts(OpenFive)
- 300+ Design Win(100 companies)
- 8 of the top 10 semiconductor companies

World Leading R&D

- Inventors of RISC-V
- 100+ PhDs
- Highly experienced Processor team (e.g., Arm, Apple, AMD)

Backed by the World's Most Innovative VCs, Silicon Companies

Undisputed leader in RISC-V computing

Complete portfolio of processors from embedded to high-performance computing

CPU Cores

SiFive Essential™

32 and 64-bit Processors

- Microcontrollers, IoT devices, real-time control, control plane processing
- Highly customizable to application specific requirements
- Mature, industry proven designs

SiFive Performance™

64-bit Application Processors

- Networking, Infrastructure, Enterprise, Consumer
- Highest performance, most advanced RISC-V Processor available
- Scale out, high performance, processing capabilities with vector compute

AI Cores

SiFive Intelligence™

Scalable AI Processors

- Edge AI, Cloud, Training, Inference
- Very high performance and efficiency for AI workloads (vector processing)
- Built on top of RISC-V Vectors and the SiFive Intelligence Extensions

$2.5B+

Valuation via $175M Series F Funding

“The market has spoken and made it abundantly clear that RISC-V computing will be competing for the heart of all future computing platforms. As the founder and market leader of RISC-V computing it’s our role to lead this ecosystem forward and offer customers advanced computing alternative to Arm and others. This valuation is a validation of our strategy, our incredible team, and our singular focus on building the leading portfolio of high-performance RISC-V compute products in the market. Our customers are signaling strong demand for SiFive to deliver the highest level of performance as quickly as possible.”

- Patrick Little, President, Chairman, and CEO, SiFive

SiFive

The Top 3 Global ISAs

x86 RISC-V® arm

SiFive

Recent Announcements

- Introduced new Product family branding aligned to Market Focus
- Entered Performance-driven markets with the fastest commercially available RISC-V IP
- Entered AI & ML-enabled markets with 2 RISC-V vector enabled processor IP products
- Execution of 3 Performance product launches & 3 RISC-V portfolio feature in 1 year
- Intel Foundry Services IP-Alliance Partner with optimized RISC-V IP & Next-Gen Developer Board

Design Wins

- Renesas
- Tenstorrent
- Deep Vision
- ArchiTek AiOnIc
- eTopus
- FADU
- Synaptics
- Intel Foundry Services
- Samsung
- Qualcomm

Partnerships

- Intel Foundry Services
  - IP Optimized for Intel 4 Process Technology
  - “Horse Creek” RISC-V Developer Platform in 2022
- Samsung Foundry
  - AI SoC Development Platform
- TSMC
  - First N5 RISC-V SoC Tapeout
- DARPA
  - First RISC-V IP provider

RISC-V Ecosystem

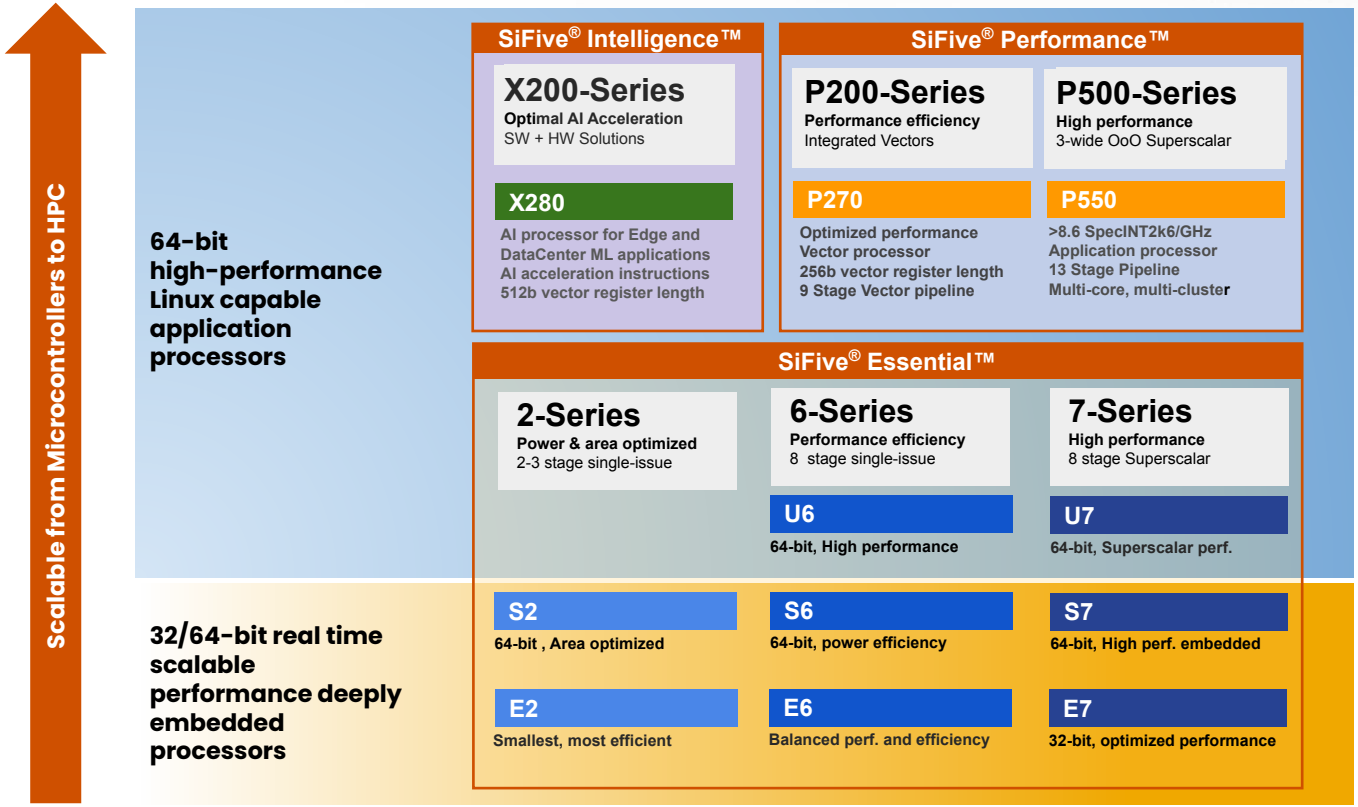
- Canonical
  - Ubuntu OS
- Green Hills
  - INTEGRITY RTOS
- SEGGER
  - emRun library
- SYSGO
  - PikeOS RTOS
- Wind River
  - VxWorks RTOS

SiFive

SiFive Vector Processors

May 2022

SiFive RISC-V processor IP portfolio



High Performance

Broadest Portfolio

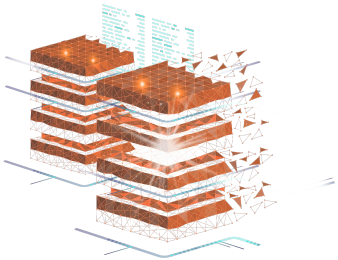
Relentless Innovation

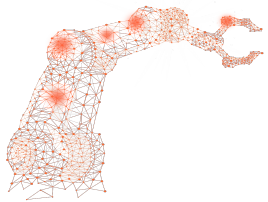
Evolving modern application trends

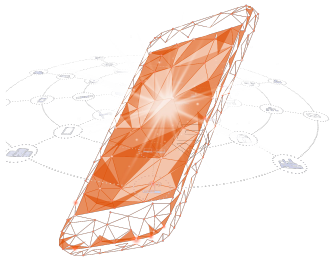
Drive towards simplicity, extensibility, and portability

Modern neural network models rapidly evolving

Access to the open-source community





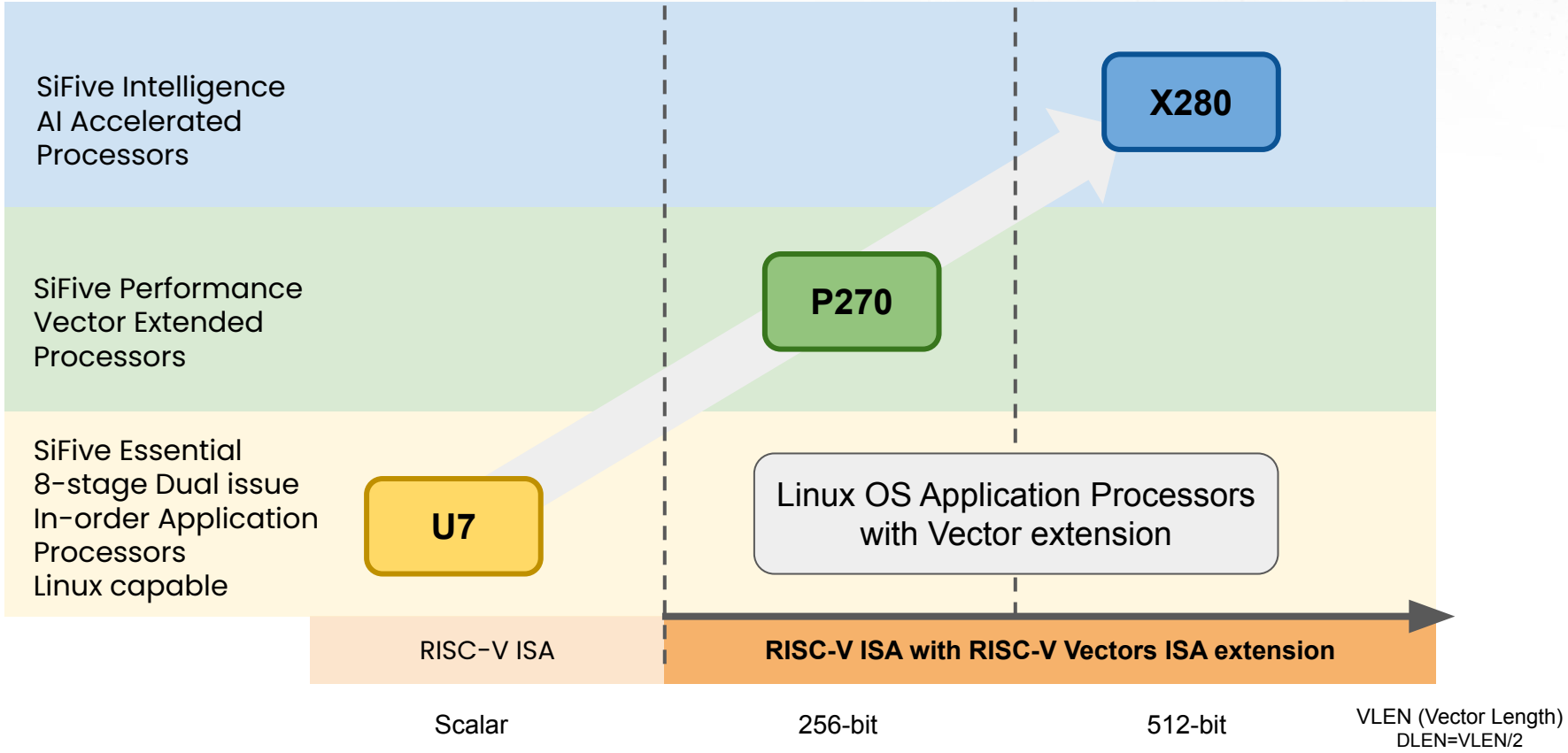


RISC-V Vectors benefits

- Single simple Vector ISA
- full reuse and portability
- Vector-length-agnostic
- design flexibility
- lower power
- smaller code size
- Linux-capable
- 48-bit virtual memory support
- Extensive vector data types and sizes
- Leverage the open-source




SiFive Vector Processors portfolio



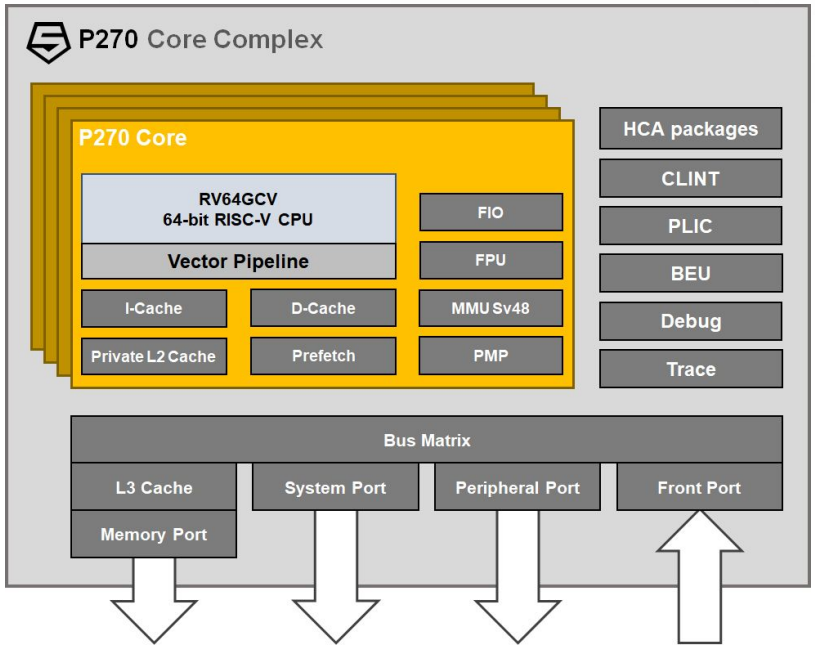
SiFive Performance P270

64-bit RISC-V Core
Virtual Memory, Linux OS Support
Hypervisor Extension

Vector Unit executing RISC-V Vector
256-bit Vector Length

8-Stage Dual-Issue In-Order
Superscalar Architecture.
Decoupled Vector Pipeline

Coherent Multicore Complex
Up to 16 cores



SiFive Intelligence X280

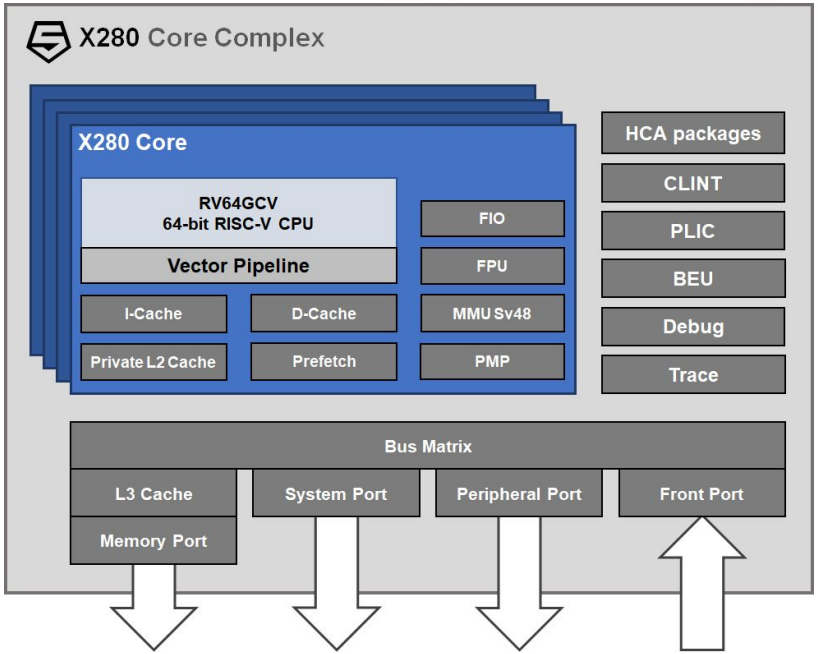
64-bit RISC-V Core
Virtual memory, Linux OS Support

512-bit vector register length
SiFive Intelligence Extensions
AI computation data type support

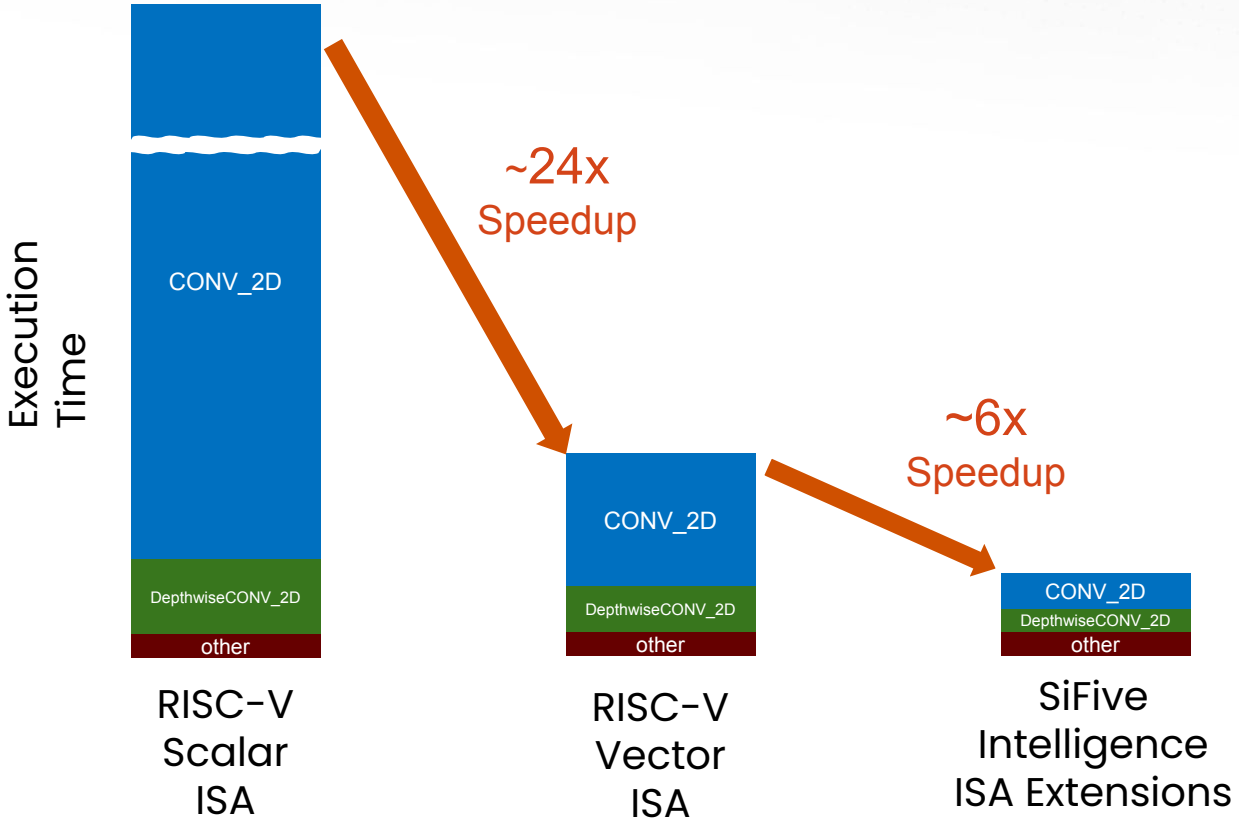
TensorFlow Lite Framework support
Optimized NN operators
Wide Range of NN models ported

8-Stage Dual-Issue In-Order
Superscalar Architecture.
Decoupled Vector Pipeline

Coherent Multicore Complex
Core Local Ports for Accelerator
Hardware connection



SiFive Intelligence: Accelerate end-to-end models

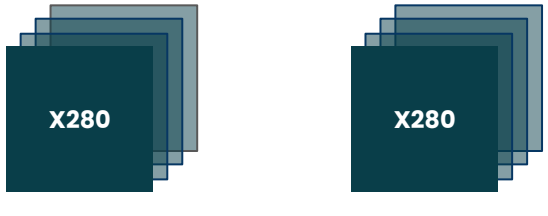


MobileNet v1 Inference (batch size=1), VLEN=512

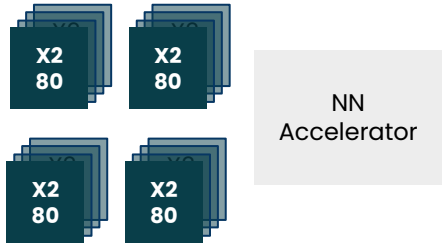
Scalable solution for wide range of AI use cases

Wearables	SmartHome	Mobile	Industrial / Drones	Data Center (Servers
~0.1 - 1 TOPS	~0.1 - 2 TOPS	1 - 5 TOPS	1 - 20 TOPS	>100 TOPS
◆ Imaging ◆ Sensor / Signal Processing ◆ Sensor Filtering / Fusion ◆ Speech Recognition				High Performance Computing (HPC) Dynamic Encryption / Security Audio/Video Streaming / Compression
Prediction Modeling / Control				

- Advanced Controller/Applications core with AI optimized Vector Extensions
- Multi-core configuration options
- Small size, lower power consumption



- Advanced Controller/Applications core with AI optimized Vector Extensions
- Multi-core configuration options
- Connectivity to NN accelerators



- Advanced Controller/Applications core with AI optimized Vector Extensions
- Multiple instantiations of Multi-core configuration options
- Connectivity to large NN accelerators
- Single unified system memory

SoC connection ports

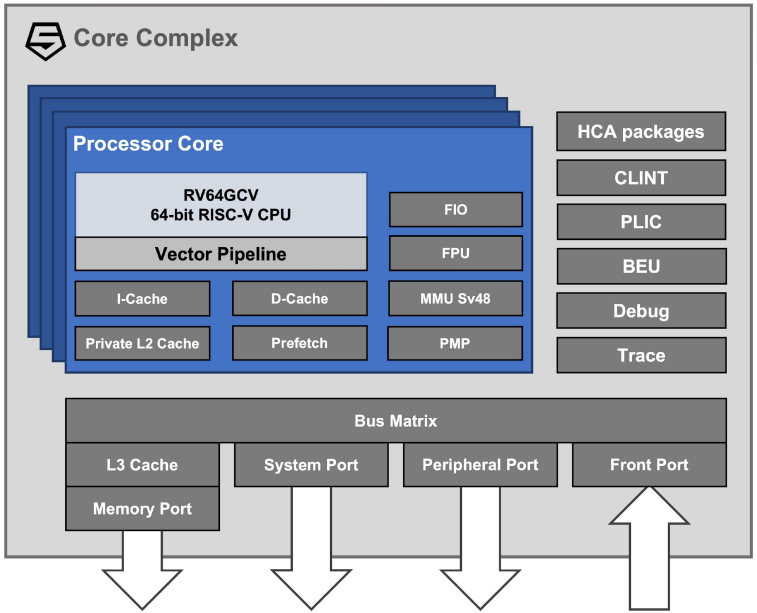
Memory Port
Highest performance interface to memory

System Port
Access to high-bandwidth uncached memory or devices

Peripheral Port
Interface with lower speed peripherals

Front Port
External Masters for accessing Core Complex devices and ports

FIO Fast I/O
Improves the throughput of uncached IO transactions (MMIO) subsystem



AMBA® AXI Protocol

Translate SIMD code to RISC-V Vectors

SiFive Recode: Protect your existing software investment, migrate with confidence

```
void dot_prod_f32(
   const float32_t *pSrcA, const float32_t
   *pSrcB, uint32_t blockSize, float32_t *result)
   {

  float32x4_t A, B;
  float32x4_t acc = vdupq_n_f32(0.0f);

  for (size_t i = 0; i < blockSize; i += 4) {
    A = vld1q_f32(&pSrcA[i]);
    B = vld1q_f32(&pSrcB[i]);
    acc = vmlaq_f32(acc, A, B);
  }
  *result = vaddvq_f32(acc);
}
```

SIMD to RVV

```
        addi    t2, zero, 4
        vsetvli a4, t2, e32,m2,tu,mu
        fmv.w.x ft0, zero
        vfmv.v.fv2, ft0
        beqz    a2, .LBB0_3
        mv      a5, zero
        slli    a2, a2, 32
        srli    t4, a2, 32
.LBB0_2:
        vle32.v v4, (a0)
        vle32.v v6, (a1)
        vfmacc.vv       v2, v4, v6
        addi    a5, a5, 4
        addi    a1, a1, 16
        addi    a0, a0, 16
        bltu    a5, t4, .LBB0_2
.LBB0_3:
        addi    a0, zero, 1
        vsetvli a0, a0, e32,m1,tu,mu
        vfmv.v.fv1, ft0
        vsetvli a0, t2, e32,m2,tu,mu
        vfredosum.vs    v4, v2, v1
        vsetvli zero, zero, e32,m1,tu,mu
        vfmv.f.sft0, v4
        fsw     ft0, 0(a3)
        ret
```

SIMD Source code

Compiled SiFive Assembly Code

Extending LLVM with auto-vectorizing compiler

- SiFive Toolsuite includes both GCC and LLVM compilers
- SiFive LLVM compiler supports RISC-V Vector intrinsics and auto-vectorization

C Code

```
void saxpy (size_t n, const float a,
const float *x, float *y)
{
 for (size_t i = 0; i < n; ++i) {
   y[i] = a * x[i] + y[i];
 }
}
```

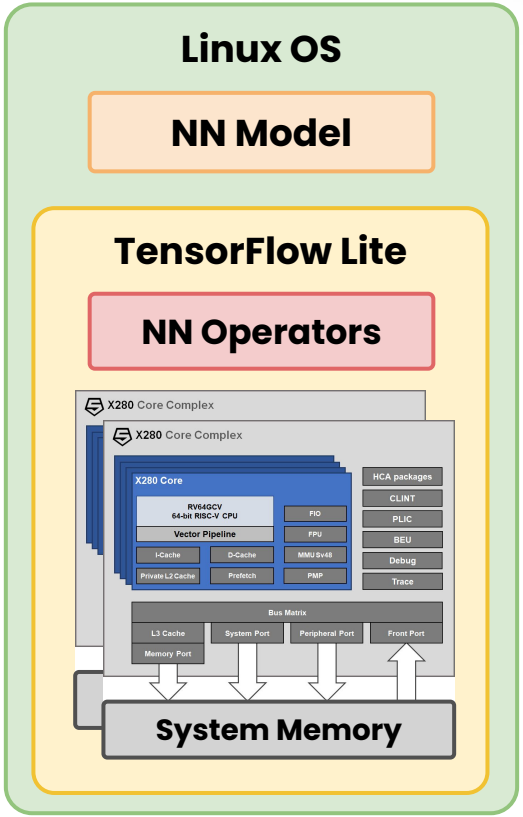
Auto-Vectorized Code

```
.LBB0_5:
        addi      a3, a4, -16
        vle32.v   v26, (a3)
        vle32.v   v27, (a4)
        vfmul.vv  v26, v26, v25
        vfmul.vv  v27, v27, v25
        addi      a3, a5, -16
        vle32.v   v28, (a3)
        vle32.v   v29, (a5)
        vfadd.vv  v26, v26, v28
        vfadd.vv  v27, v27, v29
        vse32.v   v26, (a3)
        vse32.v   v27, (a5)
        addi      a7, a7, -8
        addi      a4, a4, 32
        addi      a5, a5, 32
        bnez      a7, .LBB0_5
```

Re-Written Using C Intrinsics

```
.LBB0_1:
   vsetvli a3, a0, e32,m8,ta,mu
   vle32.v v8, (a1)
   vle32.v v16, (a2)
   vsetvli zero, a3, e32,m8,tu,mu
   vfmacc.vf  v16, fa0, v8
   sh2add  a1, a3, a1
   vsetvli zero, zero, e32,m8,ta,mu
   sub     a0, a0, a3
   vse32.v v16, (a2)
   sh2add  a2, a3, a2
   bnez    a0, .LBB0_1
```

Edge AI inferencing running TensorFlow Lite



Out-of-the-box full software and processor hardware solution with TensorFlow Lite, running under Linux OS

Run NN models in the Object detention, Image Classification, Segmentation; Text and Speech domains

Broad range of optimized NN operators in Float 32-bit and Quantized 8-bit

Enables NN models to be run with minimal porting effort

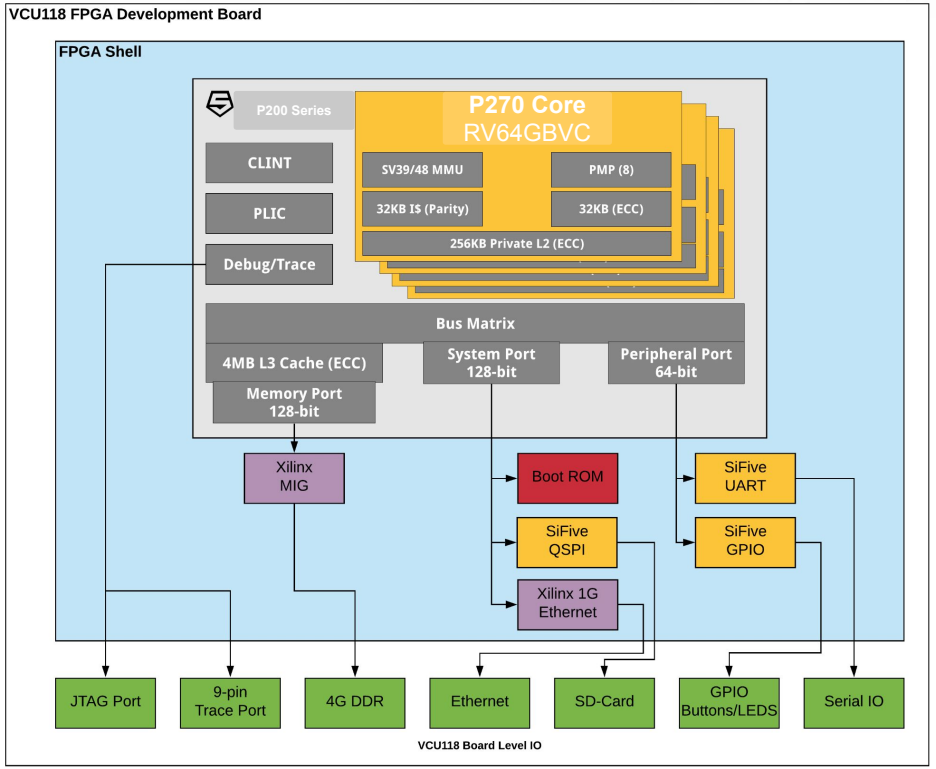
FPGA Software Development Platform

Off the Shelf FPGA Platform for Multi-Core Software Development

- Based on Xilinx VCU118 - Readily available high-capacity FPGA development board
- Image contains multi-core X280 or P270 and IO subsystem running at 32MHz.
- Ethernet, Serial, Debug, Trace, 4GB DDR

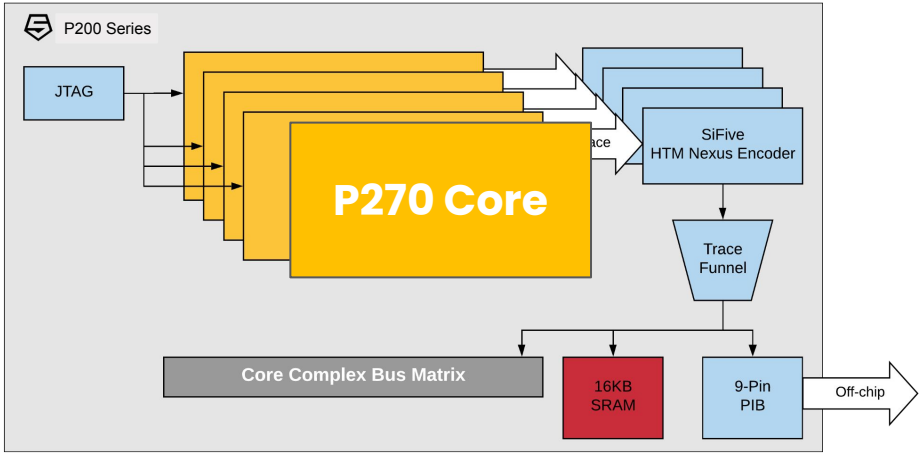
Freedom-U-SDK Linux BSP

- SD-Card based Linux boot image with naitive development tools
- Cross-Compiler environment for User-Space application development
- Yocto based workflow also available for BSP level development



SiFive Insight advanced trace and debug

- Nexus HTM Trace Encoder
- PC Sampling
- Trace Funnel
- Multiple Trace Sinks
- 40-bit Trace Timestamps
- Instrumented Trace (ITC)



Future roadmap and enhancements

SiFive Intelligence

X200-Series
Optimal AI Acceleration
SW + HW Solutions

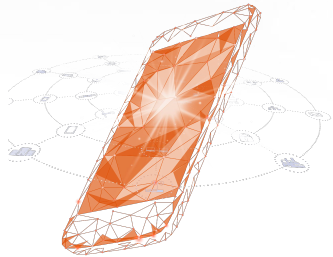
X280
AI processor for Edge and DataCenter ML applications
AI acceleration instructions
512b vector register length

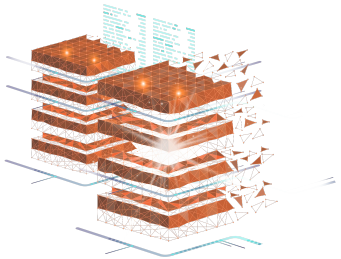
SiFive Performance

P200-Series
Performance efficiency
Integrated Vectors

P270
Optimized performance
Vector processor
256b vector register length
9 Stage Vector pipeline

- New, significantly higher performance product line
- Enriched feature set
- Extended AI software library support
- Enhanced support for Custom Accelerators





SiFive Vectors
The Intelligent Choice

SiFive Vector processors:

- High performance and built for scalability

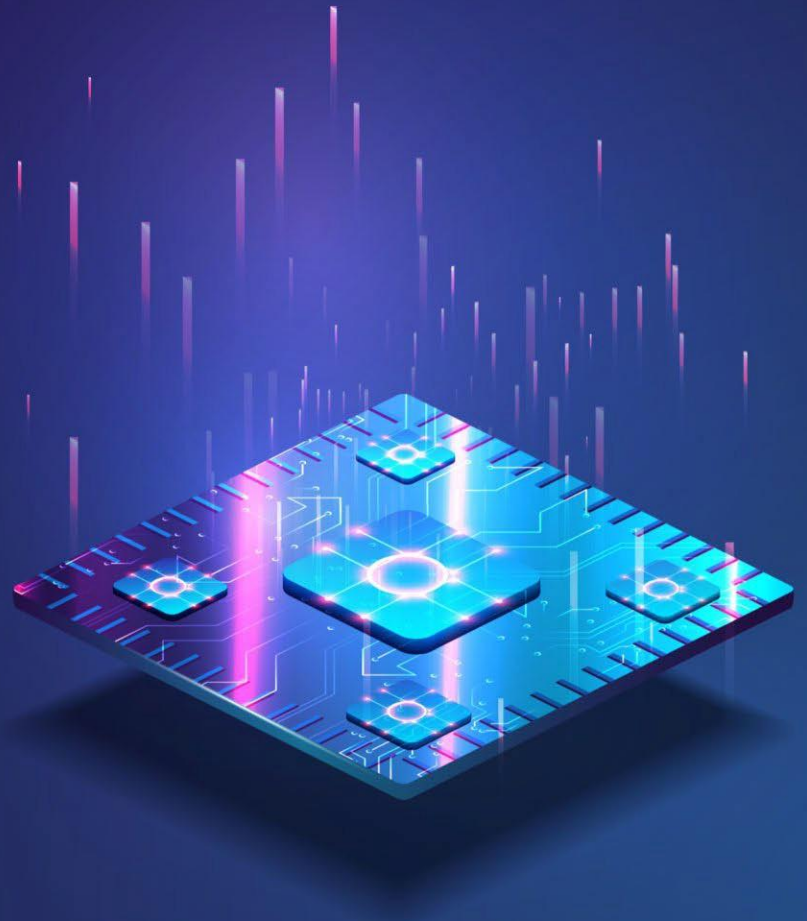
SiFive is driving innovation in AI:

- SiFive Intelligence Extensions for optimized power and performance
- Future proof from evolving ML models
- Easy adoption into existing platforms

RISC-V Vectors are the intelligent choice:

- Consolidating today's fragmented alternatives
- Open platform with vast open-source community

openfive



Custom silicon with differentiated IP

Custom Silicon Solutions

May 2022

About OpenFive

Custom silicon focus with differentiated IP

SoC design capabilities from spec-to-silicon

HQ in Silicon Valley, CA with offices globally

SiFive Business Unit

A solution-centric silicon company delivering high quality products

350+ Successful Tapeouts

<25 DPPM

150+ Million Parts shipped

18+ Years of Experience

Global Semiconductor Awards Winner

GSA Award Winner **2008** — Open-Silicon

GSA Award Winner **2009** — Open-Silicon

GSA Award Winner **2018** — SiFive

GSA Award Winner **2019** — SiFive

GSA Award Winner **2020** — SiFive

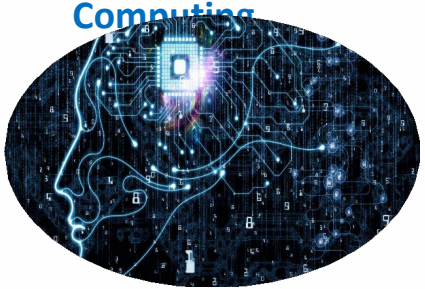
Custom Silicon Optimized for your Applications

Applications

HPC/Compute/Networking

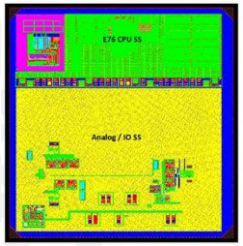
Storage

AI/Edge Computing



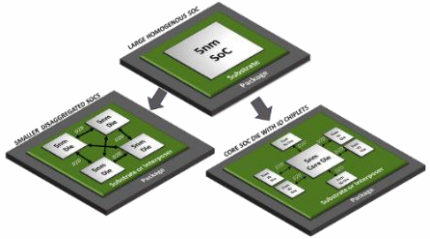
Capabilities

5nm



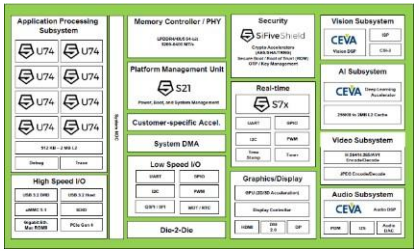
TSMC 5nm silicon
RISC-V, HBM3, D2D I/F

2.5D & Chiplets



- OpenFive Die-to-Die (D2D) IP
- 2.5D Interposer Design Capabilities
- Advanced Packaging: PI/SI Flows

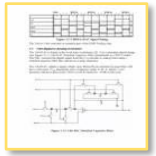
AI



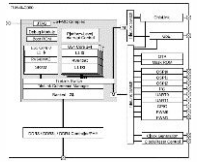
RISC-V based Apps Processor SOC

OpenFive Spec-to-Silicon Capabilities

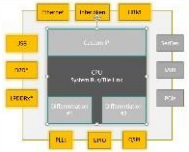
Specification | **, RTL, Verification** | | **Software** | **Prototyping** | **Physical Design**



Product Requirement & Specification



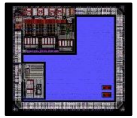
Architecture Analysis, RTL Design & Verification



IP Development, Procurement & Integration

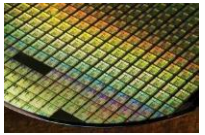
Driver Development, Firmware

FPGA & Emulation

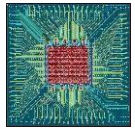


Physical Design

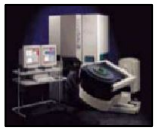
Fabrication



Assembly | **Test** | **Protos** | **Boards** | **Silicon Bring Up** | **Production**



Package Design & Assembly



Test & Product Engineering

Packaged ASIC Parts

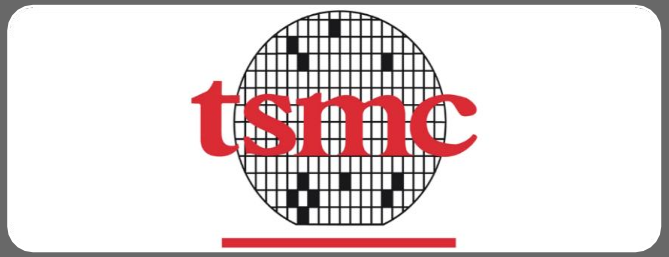
Board Design & Manufacturing

Post Silicon Validation & Software Bring-up

Production & Logistics

Flexible Design Engagement Models
Spec | Netlist | GDS2 | Production Handoff

Deep Partnerships and Engagements with Major Foundries



TSMC Value Chain Aggregator (VCA)

Early access to PDKs, foundry IP,

preferred business terms

Taped-out 250+ designs

Leading-edge engagements (16, 12, 7, 6, 5nm)

Global Foundries

22FDX platform ideal for wearable & hearables

Multiple mission critical application engagements in 22FDX, 12LP+

OpenFive IP developed in 22FDx and 12LP+

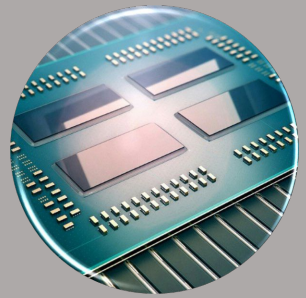
OpenFive SoC IP Portfolio – Customizable and Differentiated

Connectivity

- 400/800GbE MAC
- RS/KR/KP FEC
- FlexE
- LL Chip2Chip Controller
- AXI add-on

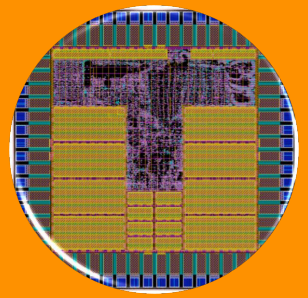
Memory Interfaces

- HBM2E PHY & Controller
- HBM3 PHY & Controller*
- LPDDR5/4X PHY
- AXI add-on



Chiplets

- Die-2-Die PHY
- Universal Die-2-Die Controller
- Light weight FEC
- Ethernet Chiplet subsystem*



System IPs

- PVT Sensors
- Custom SRAMs/TCAMs
- PLLs
- DLLs
- LVDS IOs

Soft and Physical IP on leading process nodes

OpenFive Products – Custom Silicon Solutions with Differentiated IP

Custom Silicon with differentiated IP

Idea-to-silicon capabilities
Major **foundry** partnerships

Wide access to **Ecosystem IP**

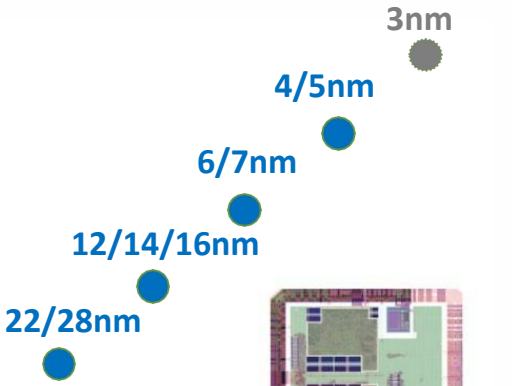
Advanced **methodologies**

Experts in **SOC IP**

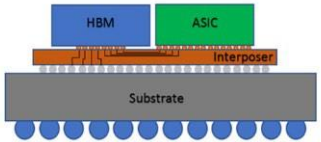
integration Manufacturing

excellence

Leading Edge Technology



Highly Integrated SoC



2.5D Solution

Customizable SOC IP

Memory Interface IP

HBM 3/2E/2

LPDDR5/4x

Connectivity IP

D2D
Interlaken

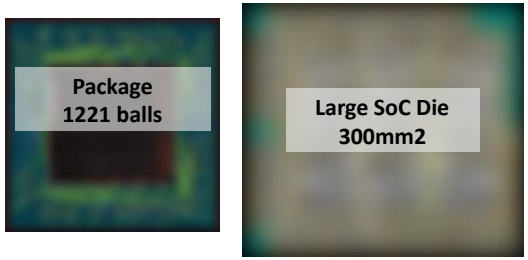
Ethernet

USB

Custom Silicon Experience with High Performance SoCs

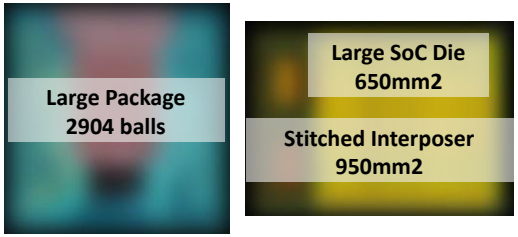
openfive

Large Networking PCIe Switch ASIC



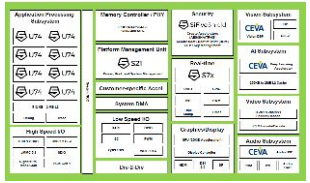
48 Lanes 56G SerDes

High Performance Networking



2.5D TSMC CoWOS
80 Lanes 56G SerDes

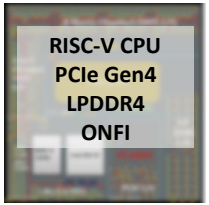
AI Vision Application Processor



Spec-to-Silicon

3D GPU, Vision, AI Acceleration, Audio Codec, DSP

Datacenter Storage/SSD



Low Power
PCIe Gen4, LPDDR4 sub-systems

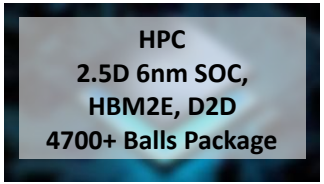
High Performance Sub-Systems Integration

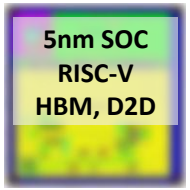
RISC-V

PCIe, HBM, DDR, SerDes
Die-to-Die and 2.5D Packaging

PD Methodologies

Many in Progress...





- OpenFive Die-to-Die (D2D) IP
- 2.5D Interposer and INFO_OS
- Advanced Packaging: PI/SI Flows
- Low-Latency Subsystems

CXL Compute Express Link

OpenFive IP Portfolio

Memory Interface IP Subsystems

HBM3, HBM2, HBM2E, LPDDR5/4X

Connectivity IP

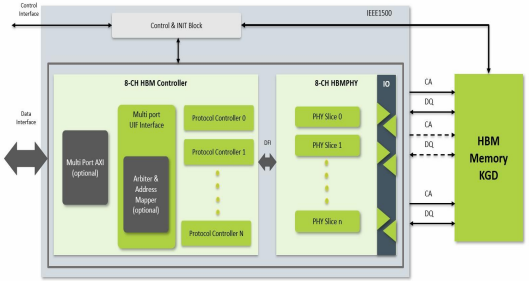
Die-2-Die(D2D), Interlaken(C2C), Ethernet, USB

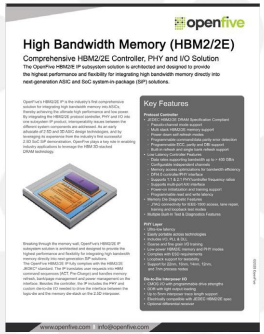
System & Peripheral IP

DMA, SPI & more …

OpenFive IP Sub-Systems - Differentiated and Customizable

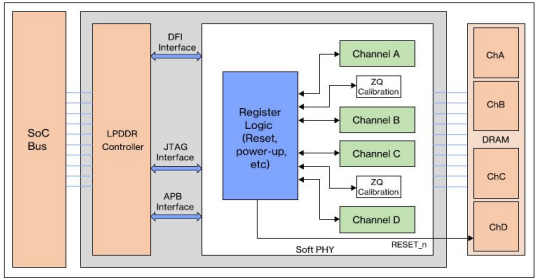
HBM

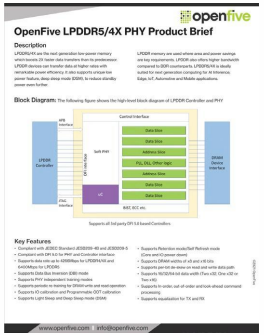




* https://openfive.com/hbm2-2e-ip-subsystem/

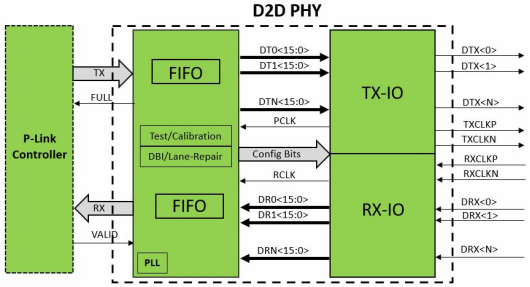
LPDDR5

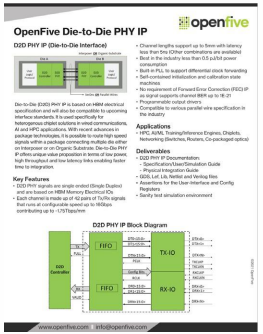




* https://openfive.com/lpddr5-4x-ip-subsystem/

D2D





* https://openfive.com/die-to-die-ip-subsystem/

Creating The Next Wave: Chiplet Solutions

PROCESSOR CHIPLETS

Scalable architecture:

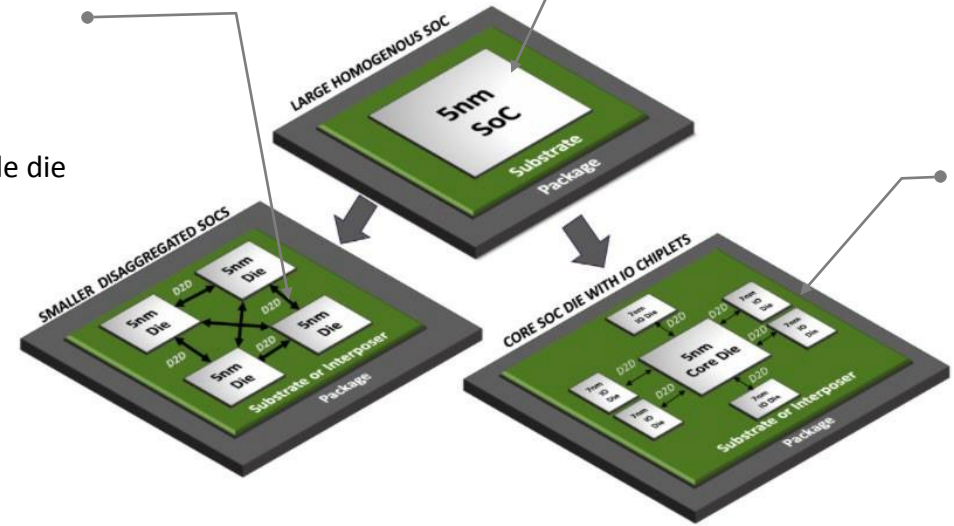
- Add dies to increase performance

Cost effective:

- Better yields with smaller die

Time to Market:

- Combine custom SoC + available die



Chip Size limit : maximum reticle size

Very large Die : Lower Yield, Power Limit

Bandwidth limit: Number of IO on die

Time to Market: Design complexity and IP readiness

IO CHIPLETS

Higher Bandwidth:

- Increase # of IO

Time to Market:

- Mix die from different nodes
- Use pre-verified chiplets

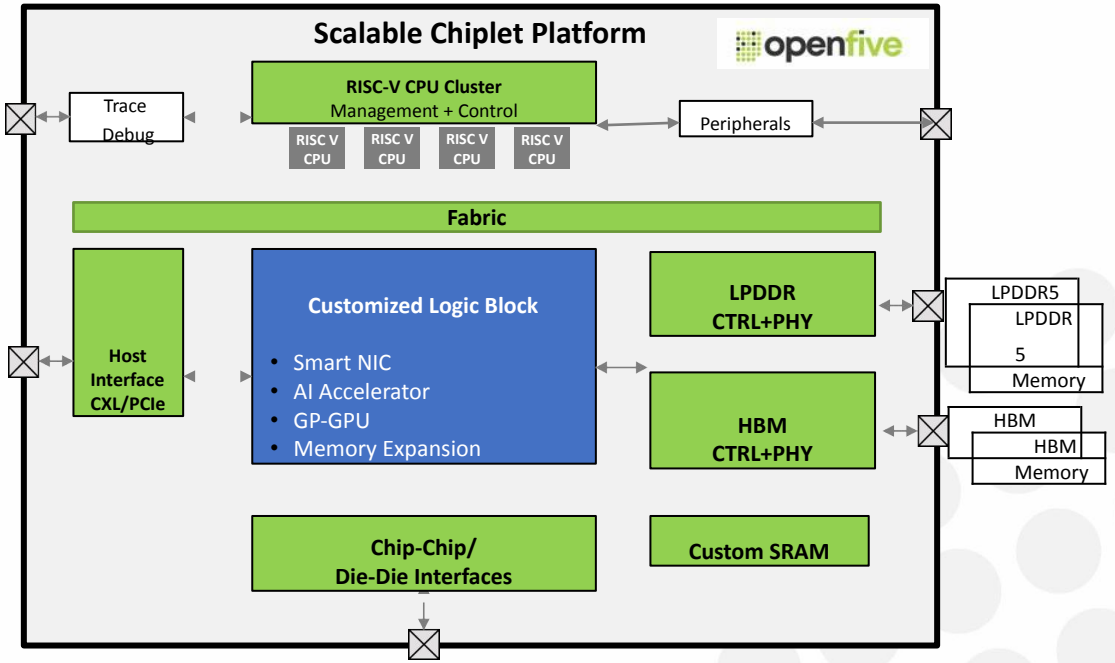
Lower Development Cost

- Share chiplets across products

OpenFive Scalable Chiplet Platforms (Compute, Memory and Connectivity)

Developed in 5nm, 6nm, 7nm nodes

- **Die-to-Die Subsystem:**
  - 640Gbps throughput D2D (single word)
  - Scalable up to 4Tbps/mm on beachfront
- **Chip-to-Chip Subsystem:**
  - 32G NRZ SerDes to 112G PAM4 SerDes
  - Scalable from 1 to N Serdes
- **Memory Subsystem:**
  - 16/32-bit LPDDR5/4x at 6.4Gbps
  - 8/16-channel HBM IOs at up to 7.2Gbps
  - Custom SRAM Macros that can achieve up to 40% Area/Power benefits at up to 2GHz
- **CPU Subsystem:**
  - 64b RISC-V multi-core, multi-cluster CPU
  - P-I-E - Depending on application needs
- **Advanced 2.5D Package:**
  - Interposer to connect multiple die on advanced nodes – silicon proved!



System and SoC IP — **Differentiated and Customizable Subsystems**

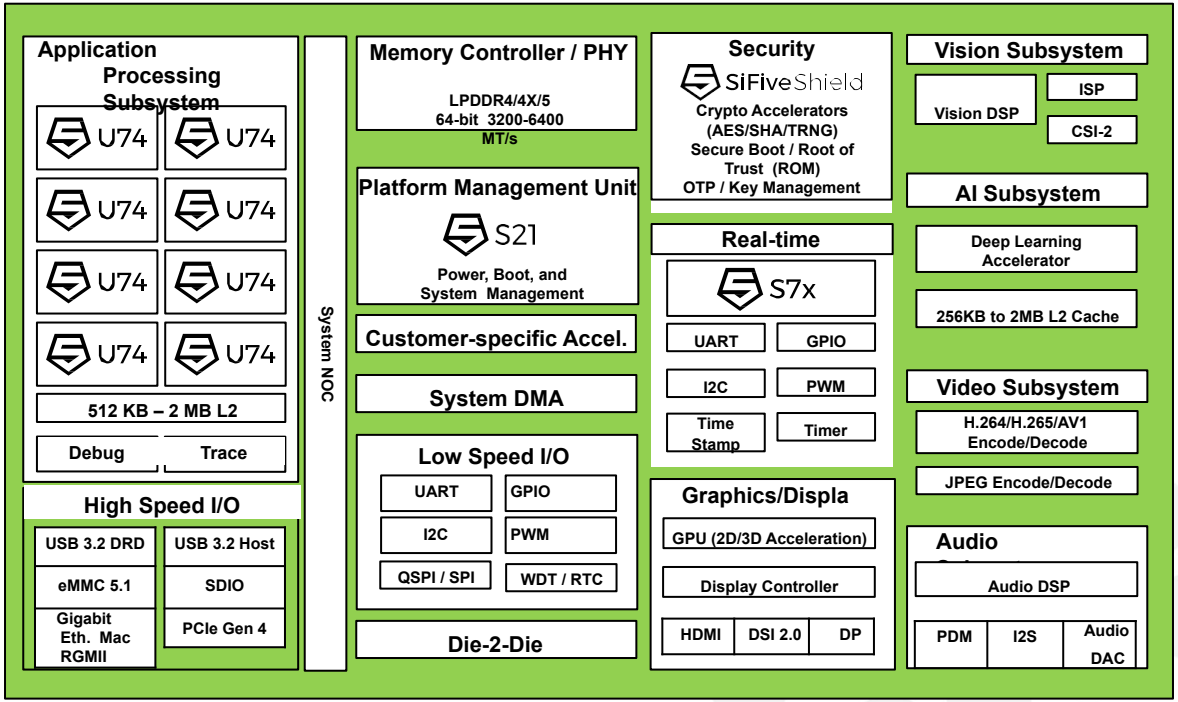
Custom IP — **Custom blocks developed for the application**

Custom silicon with differentiated IP

OpenFive RISC-V Based AI Vision SoC Platform

OpenFive AI Vision Platform

- Customizable Application Processor Chassis
  - Powerful Linux Capable RISC-V CPUs
  - High Performance LPDDR4/5 for data processing
  - Heterogenous subsystems to offload and accelerate various usages
- Reuse of pre-hardened subsystems
- Focus on your key differentiator



Key Features of an AI Vision Platform

The Brains
Running High-level Processing
4-8 SiFive Linux Capable CPUs
Up to 2 MB L2 Cache

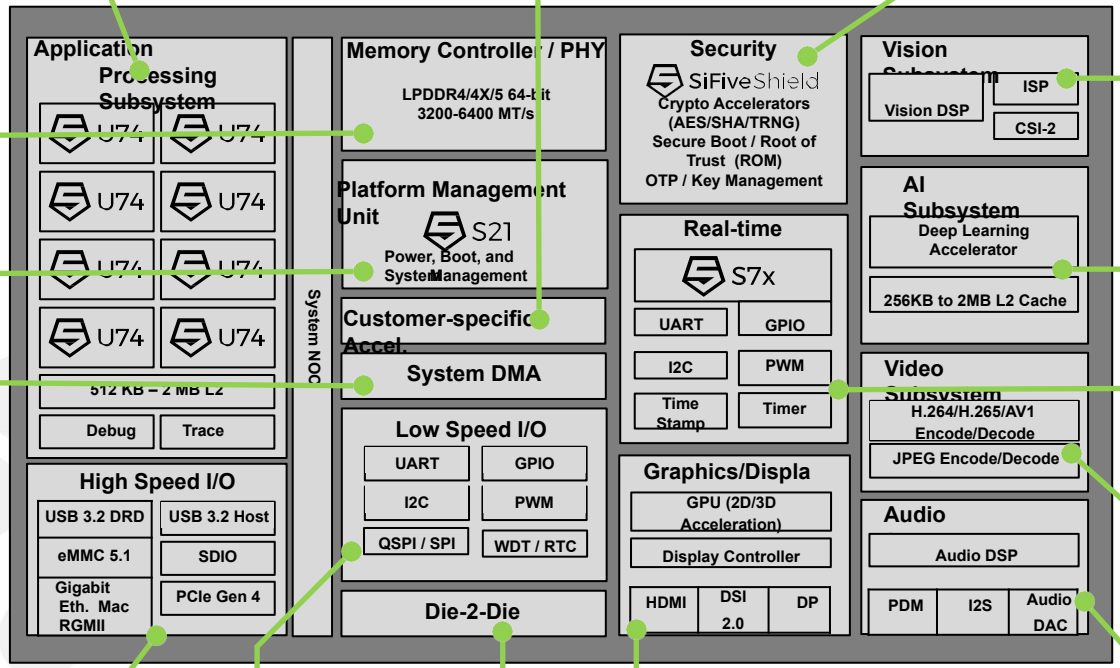
Memory
High Bandwidth 4-8GB DRAM
32-/64-bit LPDDRx 6400 MT/s

SoC Platform Management
SiFive S21 Embedded CPU
Power, Boot, System Health

System DMA
Offload moving bulk data

High Speed I/O
USB 3.2 for external cameras and peripherals
eMMC 5.1 for GB Flash Storage
SDIO, PCI Express, Gigabit Ethernet for Wireless and Wired Network Connectivity

Your Secret Sauce
Customer specific accelerator and logic



Low Speed I/O
Connect to off chip peripherals

Die-2-Die
Expansion Integration

Visualization
2D/3D Graphical User Interface
Output to DSI, HDMI, Display port

SiFive Shield
Security to protect data
Run Trusted Software

The Eyes
Vision DSP for Traditional Computer Vision
ISP to preprocess RAW video from CSI Cameras

AI
Accelerate Deep Learning Algorithms

Real Time Processors
Actuation
Motion Control

Recorder
Hardware accelerated video encoding and decoding

The Ears
Echo cancellation
Noise suppression
Predictive maintenance

Software Development for the AI Vision SoC

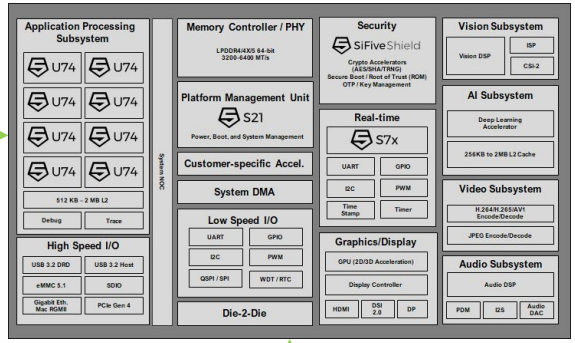
TensorFlow
Caffe PyTorch
ML Frameworks

Trained networks

NN Compiler

Optimized networks

"Customer Defined" AI Vision SoC



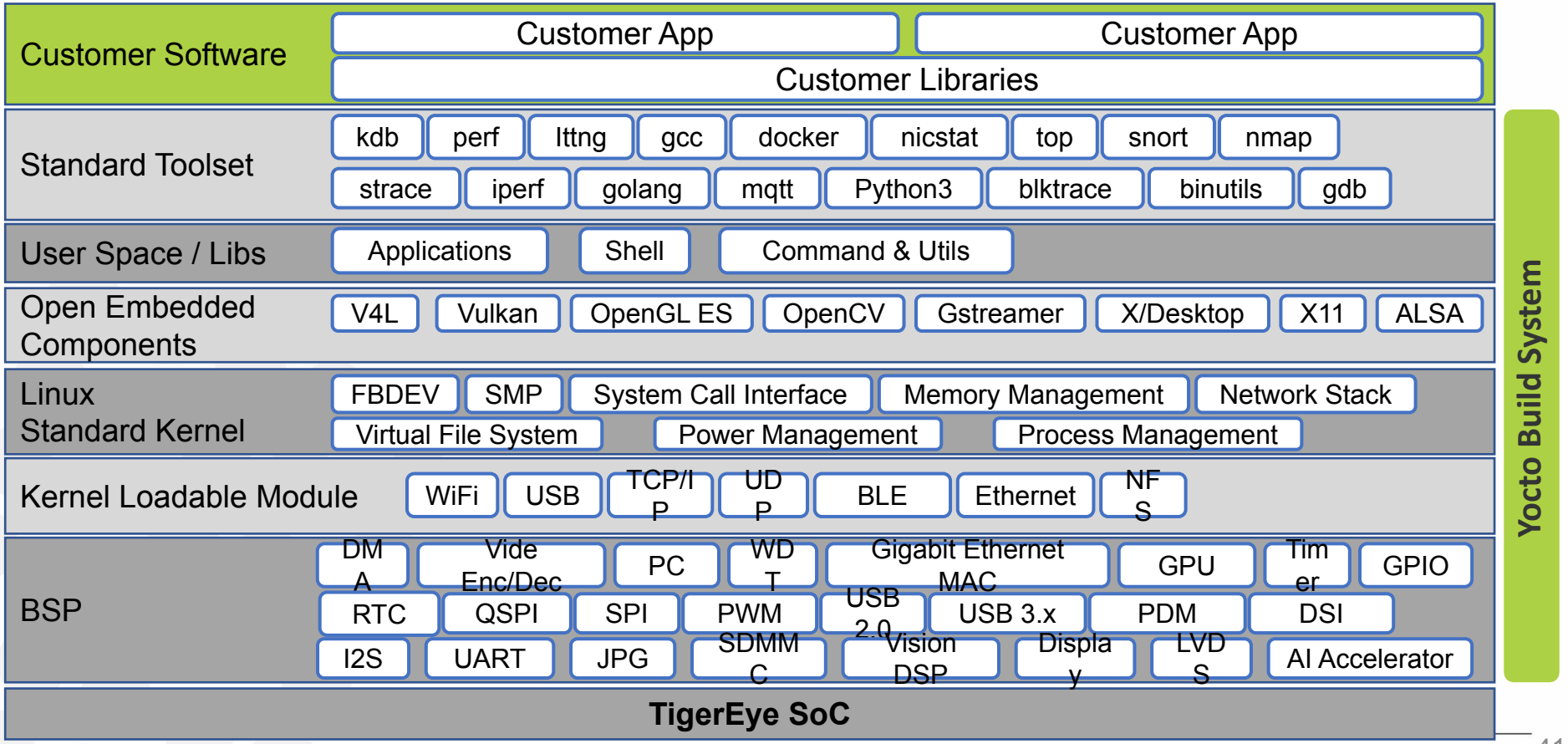
Drivers, APIs, Applications

Base SDK

FPGA Emulation

Full chip representation during development

Software Stack



Thank you