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# IoT-oriented RISC-V-based SOTB-65nm System-on-Chip Implementations

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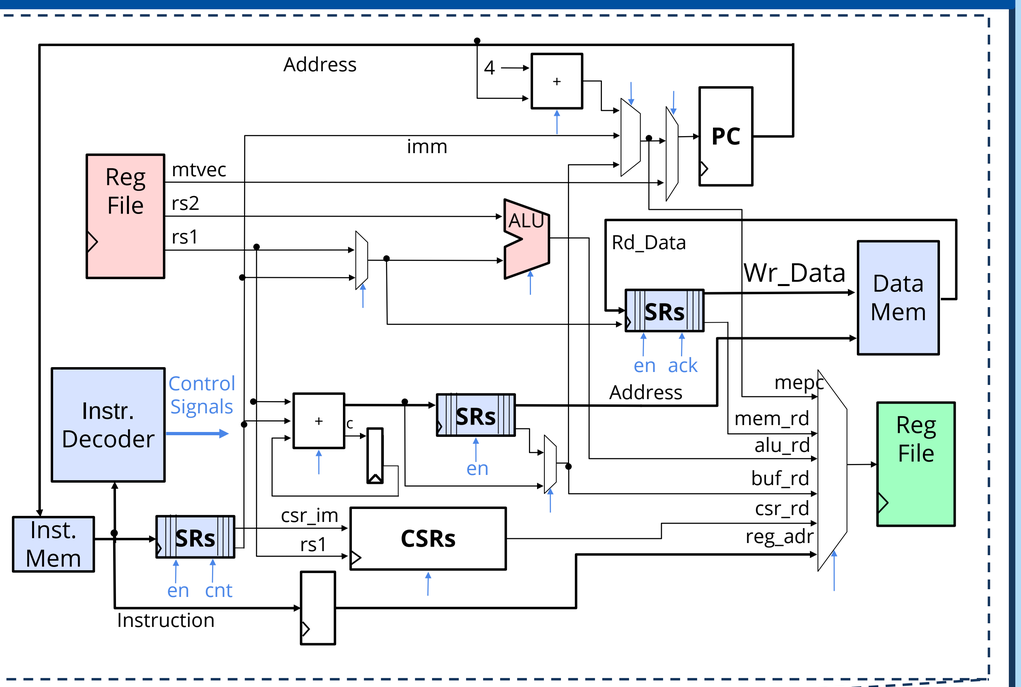
## I. INTRODUCTION

Some Internet of Things applications require data processing and communication capabilities. Even when power sources are limited, these capabilities need to be granted, such as energy harvesting and batteries. The architectural heterogeneity can be dissected to shed light on the trade-offs in the RISC-V design to achieve a minimal processor. In this paper, we present two System-on-Chips, SERV-32I and SERV-32E, based on low power and low footprint RISC-V processor, due to serial architecture and leakage control using the tension on the body exploiting the characteristics of the technology. As for the core area, SERV-32E is 28% smaller than SERV-32I while achieving negligible performance loss. The Dhrystone benchmark achieved by the SERV-32I is 1.11 DMIPS, while that of the SERV-32E is 1.05 DMIPS. The experiment results show that energy per cycle in reverse-body bias can be reduced to 3.53pJ/cycle and 2.32pJ/cycle with a 0.29-V power supply for SERV-32I and SERV-32E, respectively.

## II . PROPOSED ARCHITECTURE



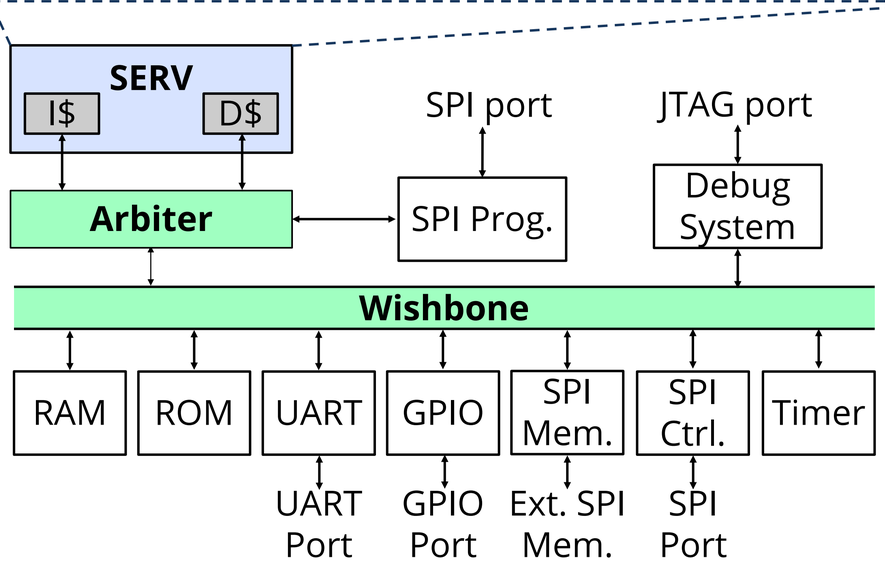




***Fig. 1*:** SERV System on Chip

## III . CHIP MICROGRAPH

| | | |
|---|---|---|
| VDD:0.27V~1.2V<br>VBB: -2.0V~2.0V | Operating Voltage | VDD:0.27V~1.2V<br>VBB: -2.0V~2.0V |
| 98,423 | Area[µm2] | 118,026 |
| ~70,000 | Gate Count | ~84,000 |
| 11kHz~30MHz | Operating Frequency | 10kHz~30MHz |
| VDD: 0.27V ~ 1.1V<br>VBB: -2.0V ~ -0.4V | Sub-µW Operating | VDD: 0.27V ~ 0.9V<br>VBB: -2.0V ~ -0.4V |
| SERV-32E | Microprocessor | SERV-32I |

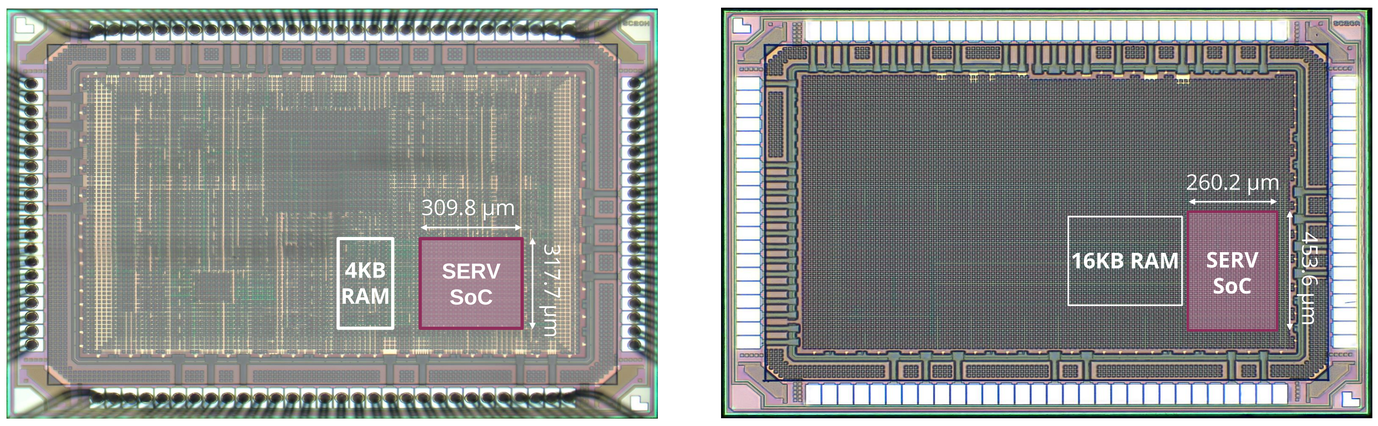



***Fig. 2*:** SERV SoCs Micrograph.

***Table I.*** ASIC Implementation in comparison.

| | Tech. | VDD [V] | Power [µW/MHz] | Leakage [µW] | NAND Gate | Freq. [MHz] |
|---|---|---|---|---|---|---|
| **[4]** | SOTB 65nm | 0.22 | 13.3 | 0.049 | 50.1k | 14 |
| **[5]** | FDX 22nm | 0.42 | 4.47 | 105.4 | - | 18 |
| **[6]** | FDX 22nm | 0.55 | 6.3 | 6.6 | - | 40 |
| **[7]** | FDSOI 28nm | 0.4 | 3.3 | 8.4 | - | 40 |
| **[8]** | FDSOI 65nm | 0.5 | 13.4 | - | - | 0.00207 |
| **SERV-32I** | SOTB 65nm | 0.29 | 3.53 | 0.007 | - | 0.011 |
| **SERV-32I SoC** | SOTB 65nm | 0.29 | 6.97 | 0.03 | 84k | 0.011 |
| **SERV-32E** | SOTB 65nm | 0.29 | 2.37 | 0.0024 | - | 0.01 |
| **SERV-32E SoC** | SOTB 65nm | 0.29 | 3.11 | 0.0037 | 70k | 0.01 |

## IV . MEASUREMENT RESULTS

SERV-32I and SERV-32 are compared side-by-side in terms of power per cycle, power consumption, and area distribution. They are also compared with other state-of the-art implementations. The SERV-32E's energy per cycle is the lowest of all the implementations compared.

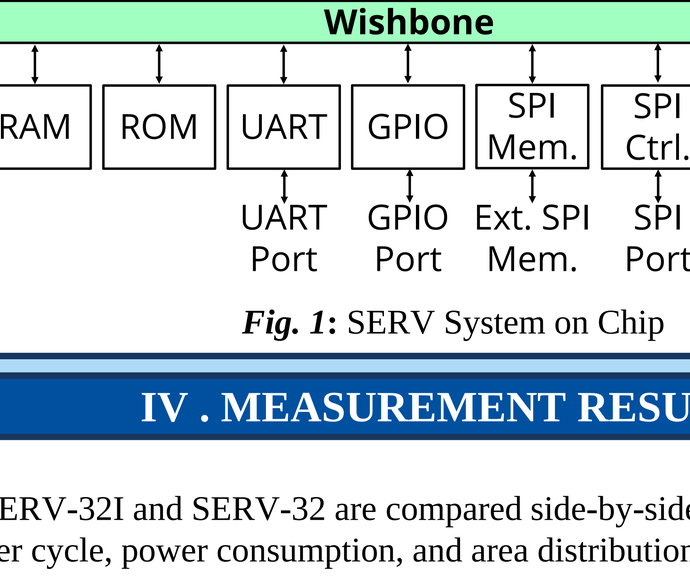



***Fig. 3*:** SERV SoCs Power breakdown at VDD = 0.4V and different Bias Voltage..

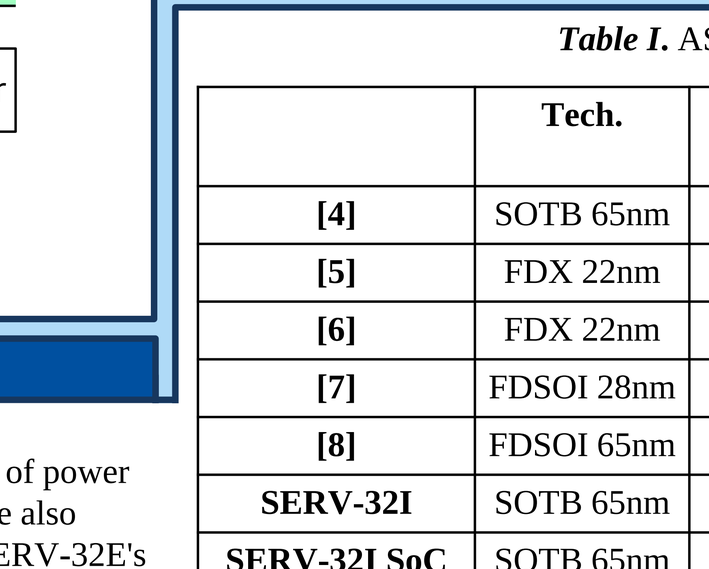



***Fig. 4*:** SERV Active Energy per cycle at different VDD.

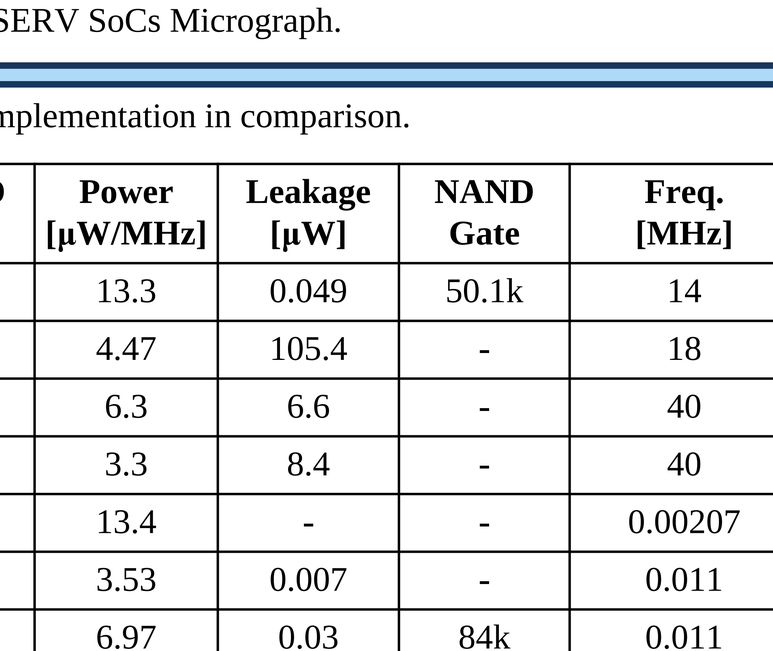



***Fig. 5*:** Area distribution of SoCs

## REFERENCES

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## ACKNOWLEDGEMENT

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