



# IoT-oriented RISC-V-based SOTB-65nm System-on-Chip Implementations

Khai-Duy Nguyen<sup>1</sup>, Koichiro Ishibashi<sup>1</sup>, Cong-Kha Pham<sup>1</sup>, and Trong-Thuc Hoang<sup>1</sup>  
<sup>1</sup>University of Electro-Communications (UEC), Tokyo, Japan

## I. INTRODUCTION

Some Internet of Things applications require data processing and communication capabilities. Even when power sources are limited, these capabilities need to be granted, such as energy harvesting and batteries. The architectural heterogeneity can be dissected to shed light on the trade-offs in the RISC-V design to achieve a minimal processor. In this paper, we present two System-on-Chips, SERV-32I and SERV-32E, based on low power and low footprint RISC-V processor, due to serial architecture and leakage control using the tension on the body exploiting the characteristics of the technology. As for the core area, SERV-32E is 28% smaller than SERV-32I while achieving negligible performance loss. The Dhrystone benchmark achieved by the SERV-32I is 1.11 DMIPS, while that of the SERV-32E is 1.05 DMIPS. The experiment results show that energy per cycle in reverse-body bias can be reduced to 3.53pJ/cycle and 2.32pJ/cycle with a 0.29-V power supply for SERV-32I and SERV-32E, respectively.

## II. PROPOSED ARCHITECTURE

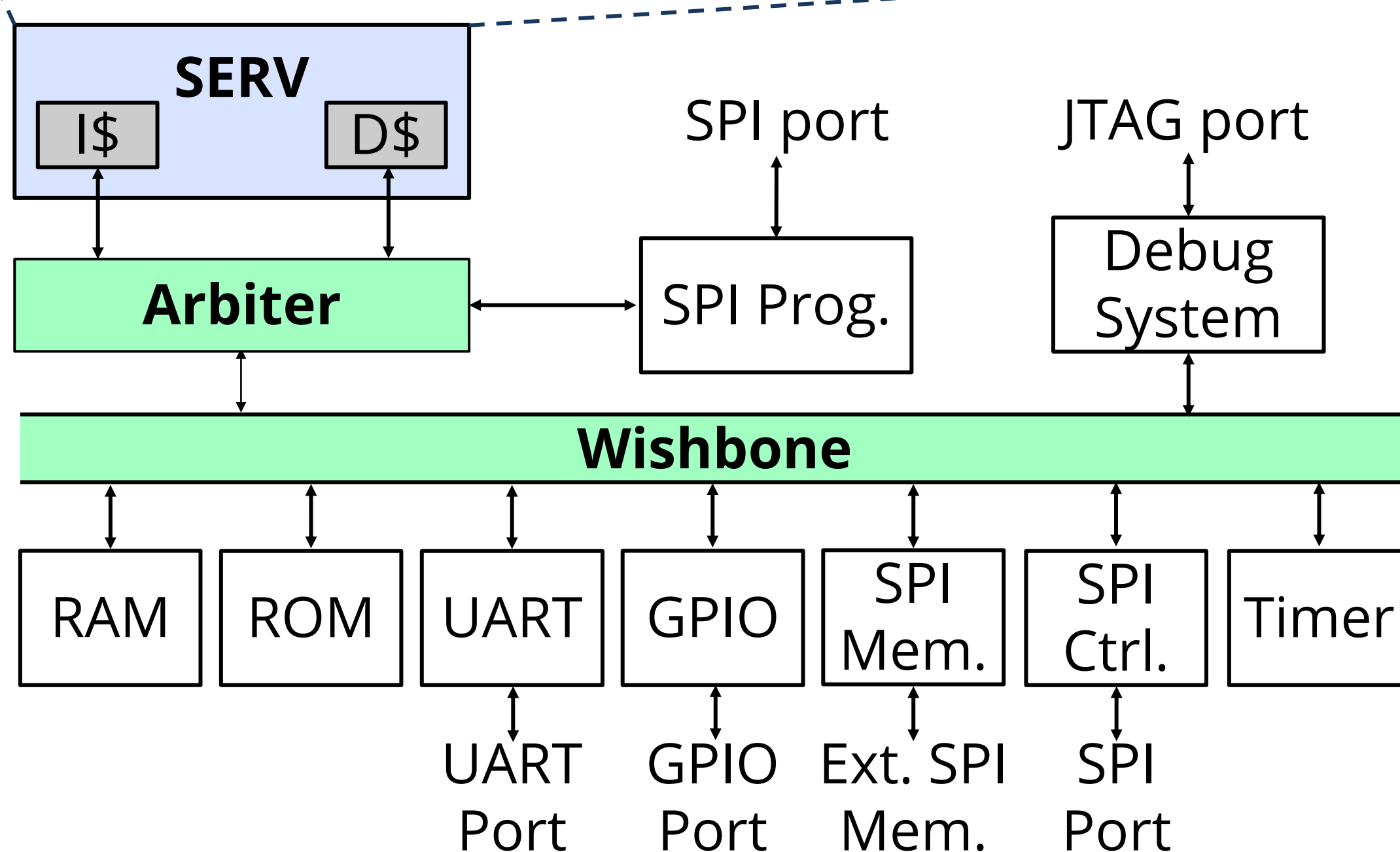
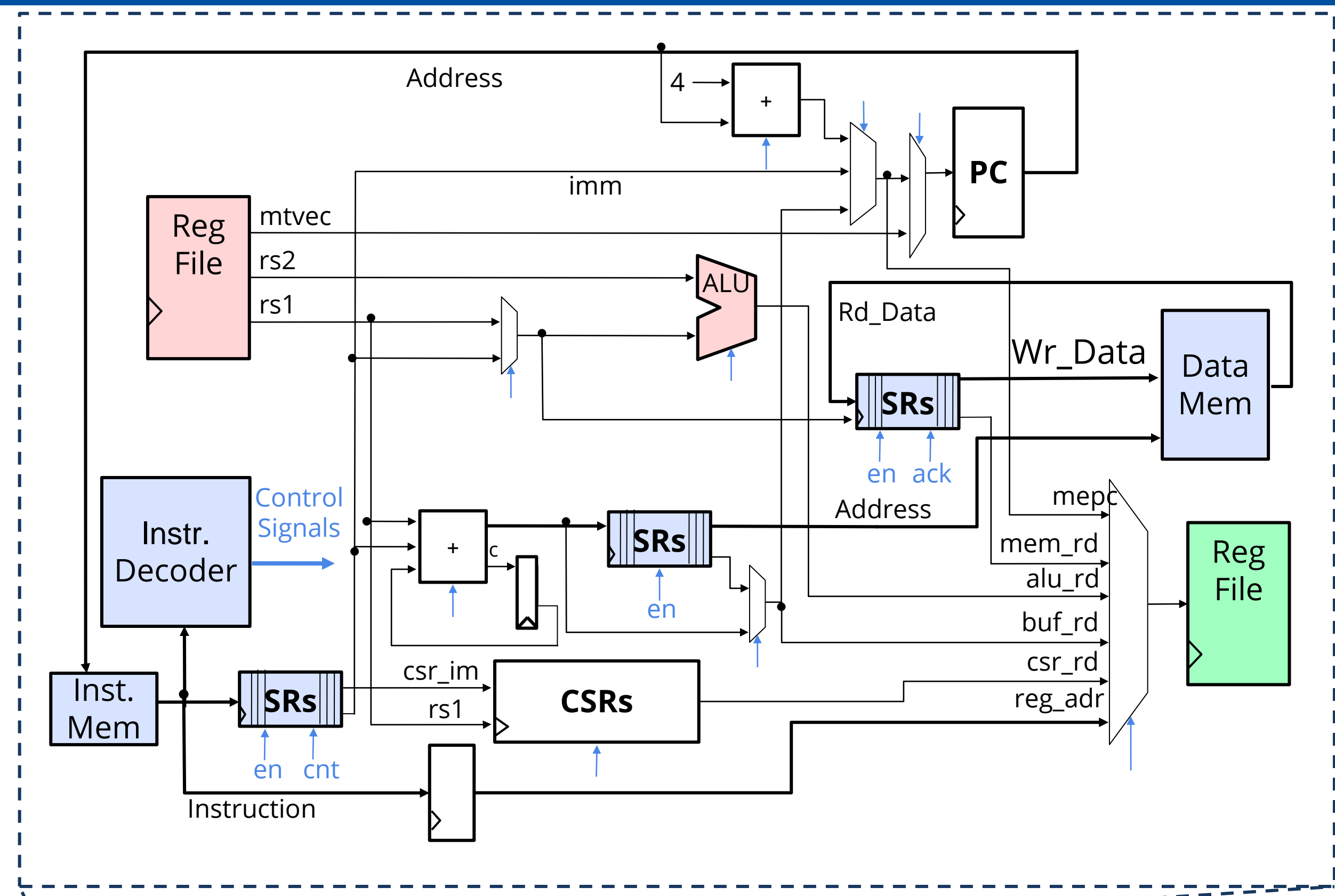


Fig. 1: SERV System on Chip

## IV. MEASUREMENT RESULTS

SERV-32I and SERV-32E are compared side-by-side in terms of power per cycle, power consumption, and area distribution. They are also compared with other state-of-the-art implementations. The SERV-32E's energy per cycle is the lowest of all the implementations compared.

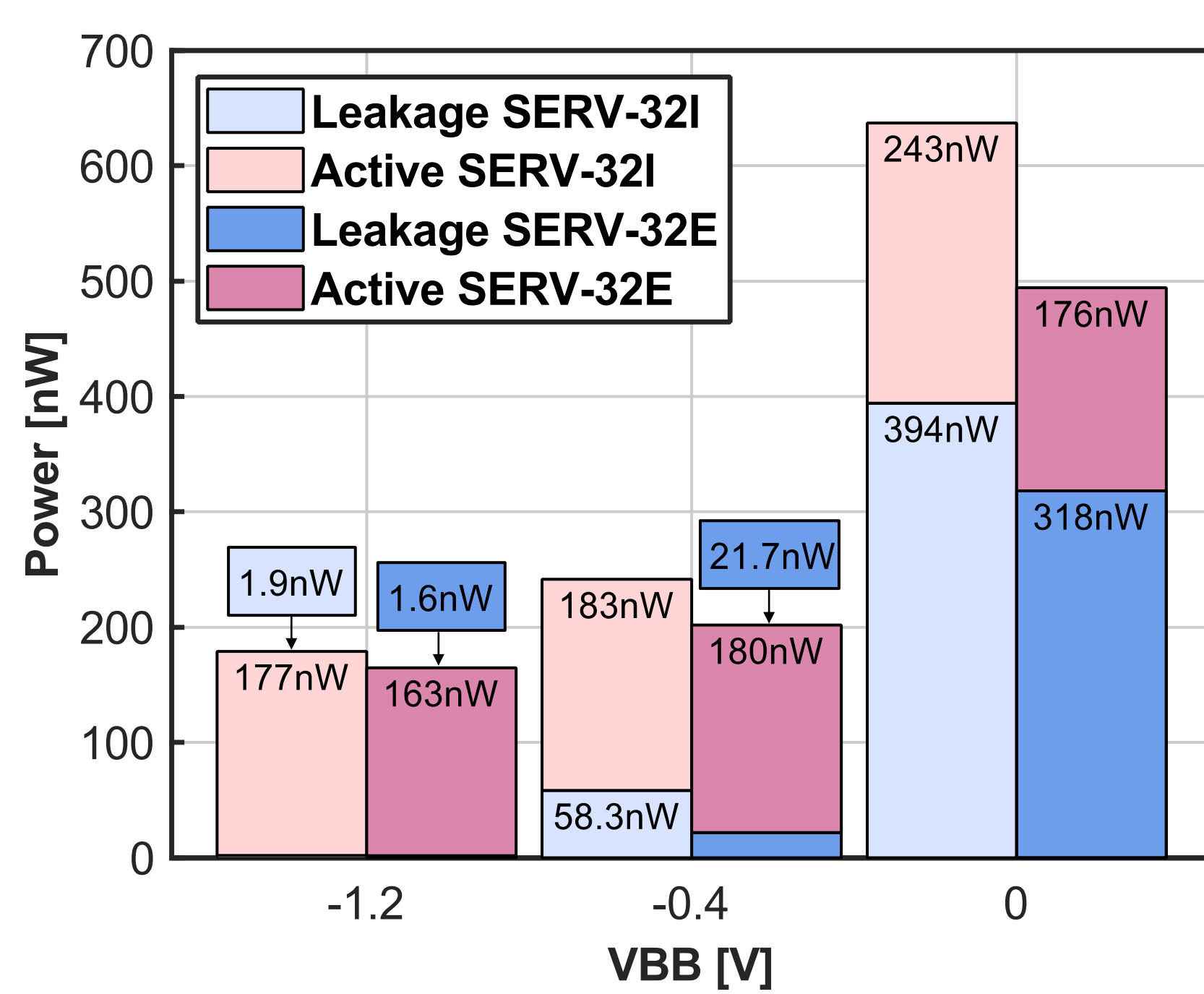


Fig. 3: SERV SoCs Power breakdown at VDD = 0.4V and different Bias Voltage.

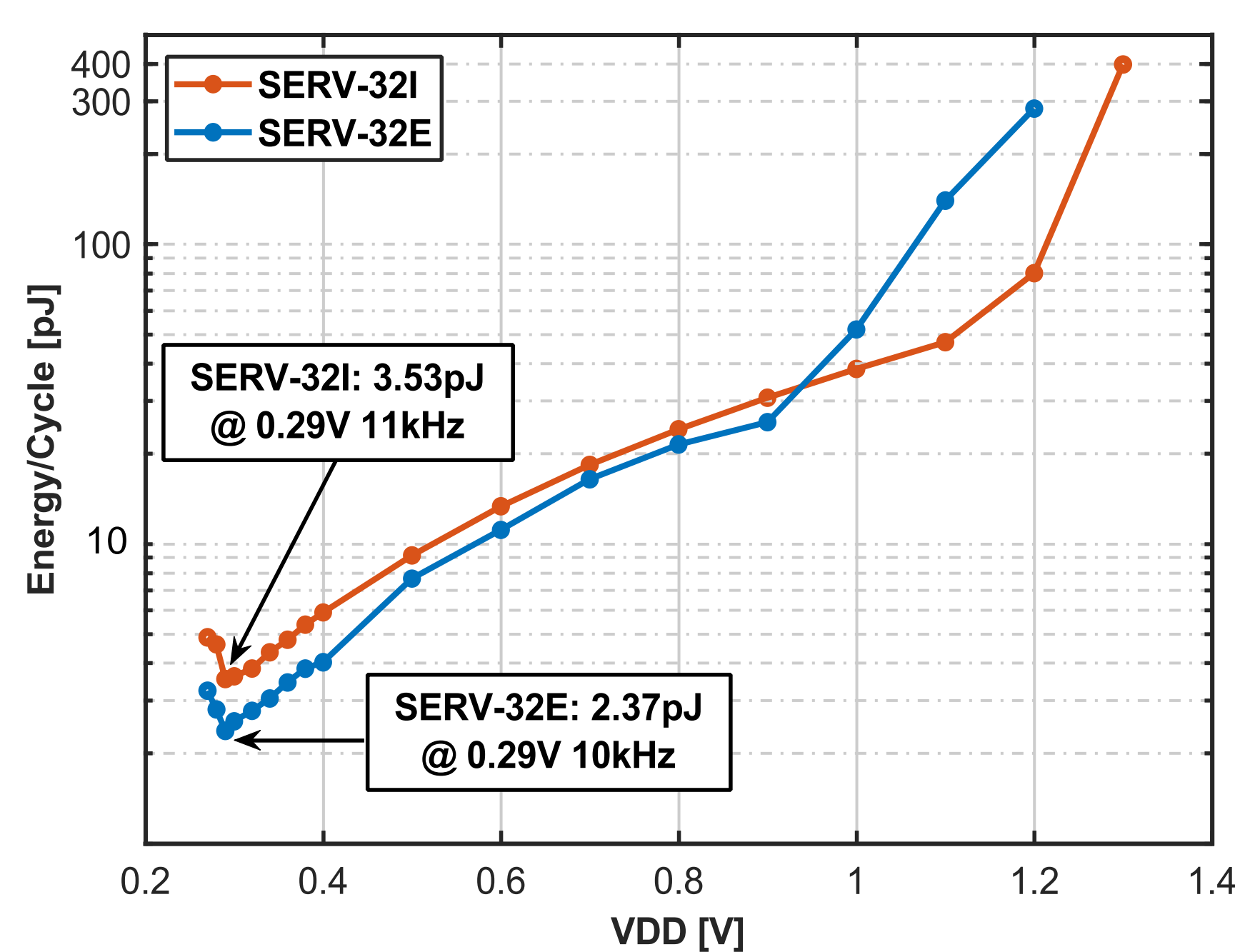


Fig. 4: SERV Active Energy per cycle at different VDD.

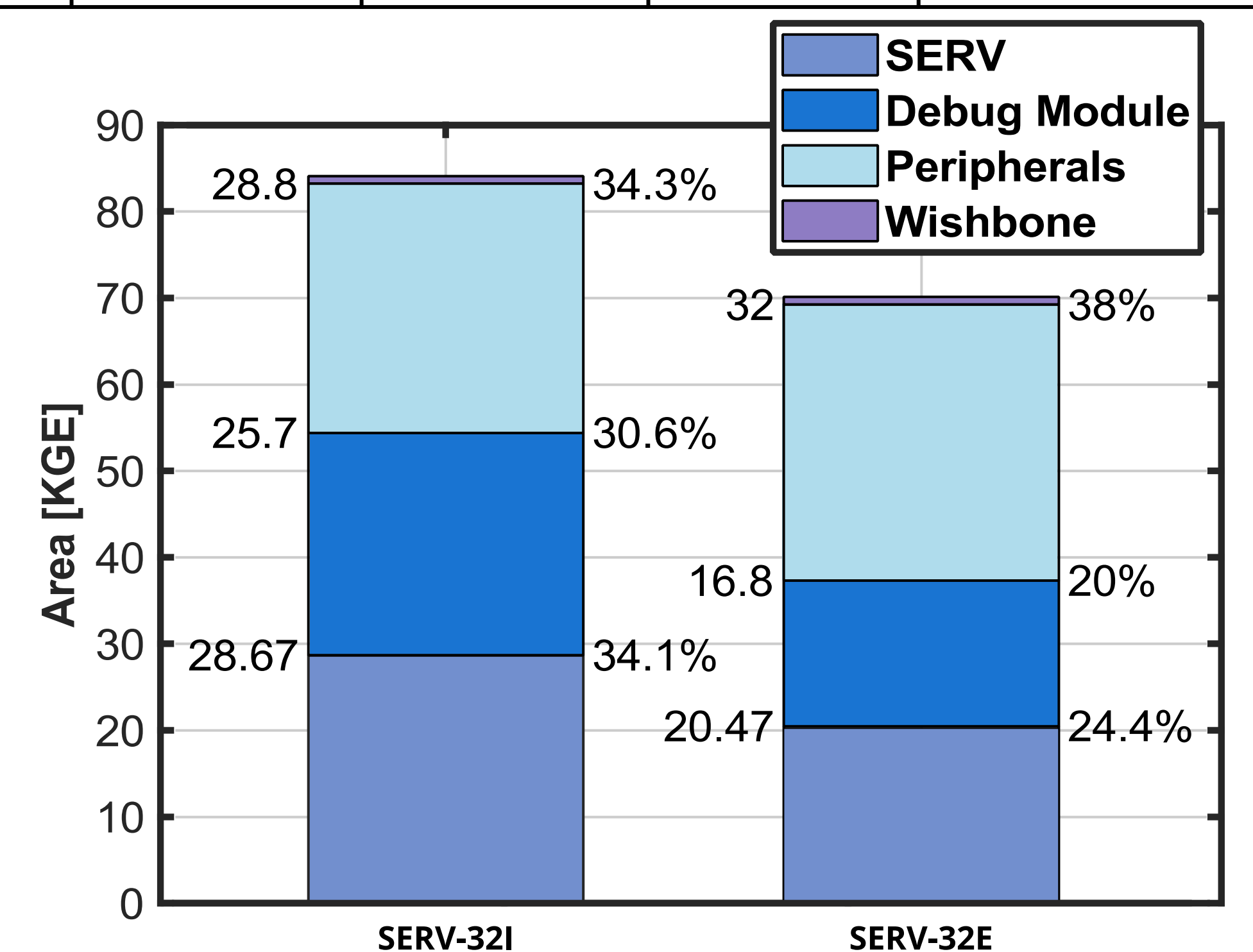


Fig. 5: Area distribution of SoCs

## III. CHIP MICROGRAPH

| VDD:0.27V~1.2V<br>VBB: -2.0V~2.0V       | Operating Voltage            | VDD:0.27V~1.2V<br>VBB: -2.0V~2.0V       |
|---|------------------------------|---|
| 98,423                                  | Area[ $\mu\text{m}^2$ ]      | 118,026                                 |
| ~70,000                                 | Gate Count                   | ~84,000                                 |
| 11kHz~30MHz                             | Operating Frequency          | 10kHz~30MHz                             |
| VDD: 0.27V ~ 1.1V<br>VBB: -2.0V ~ -0.4V | Sub- $\mu\text{W}$ Operating | VDD: 0.27V ~ 0.9V<br>VBB: -2.0V ~ -0.4V |
| SERV-32E                                | Microprocessor               | SERV-32I                                |

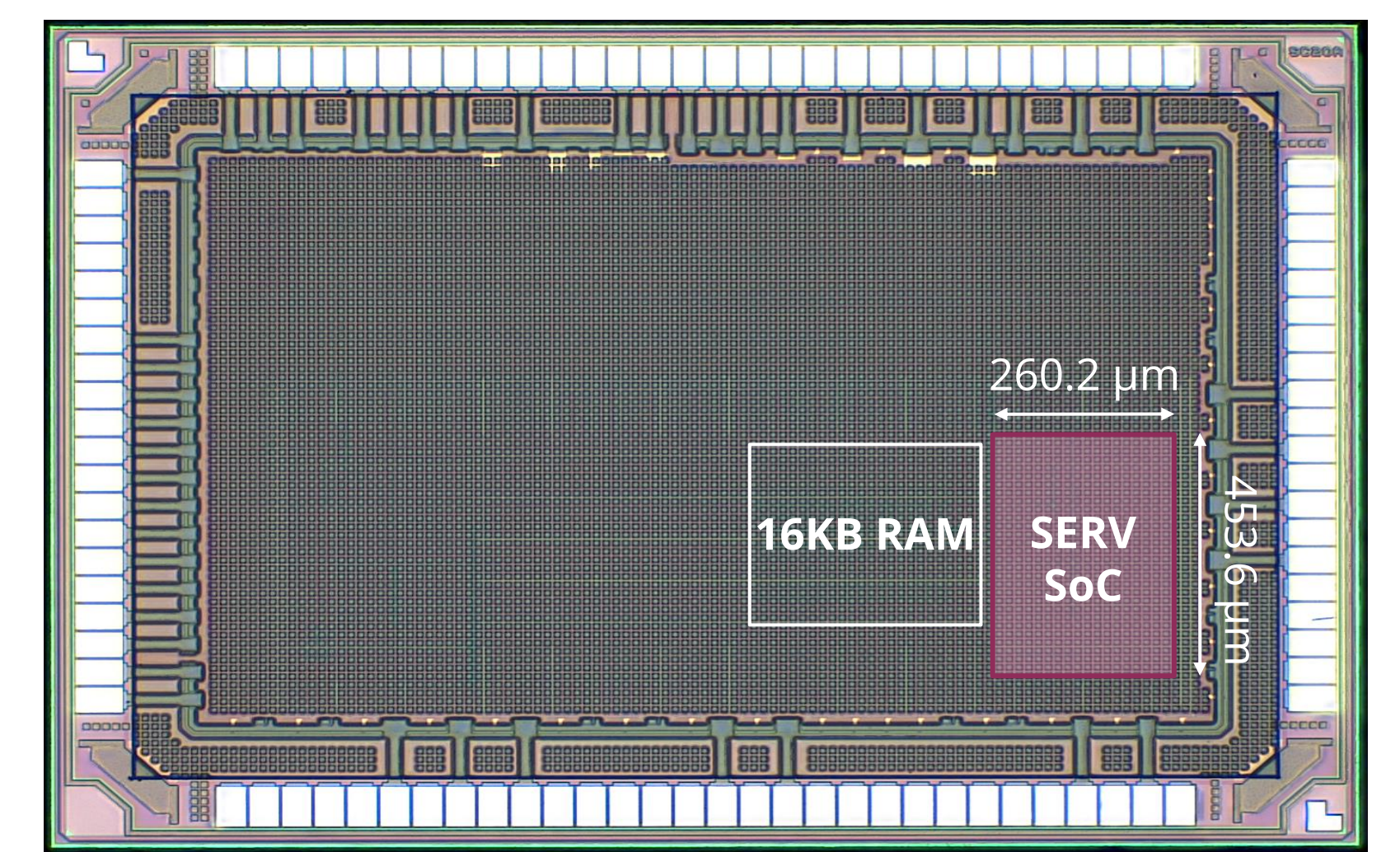
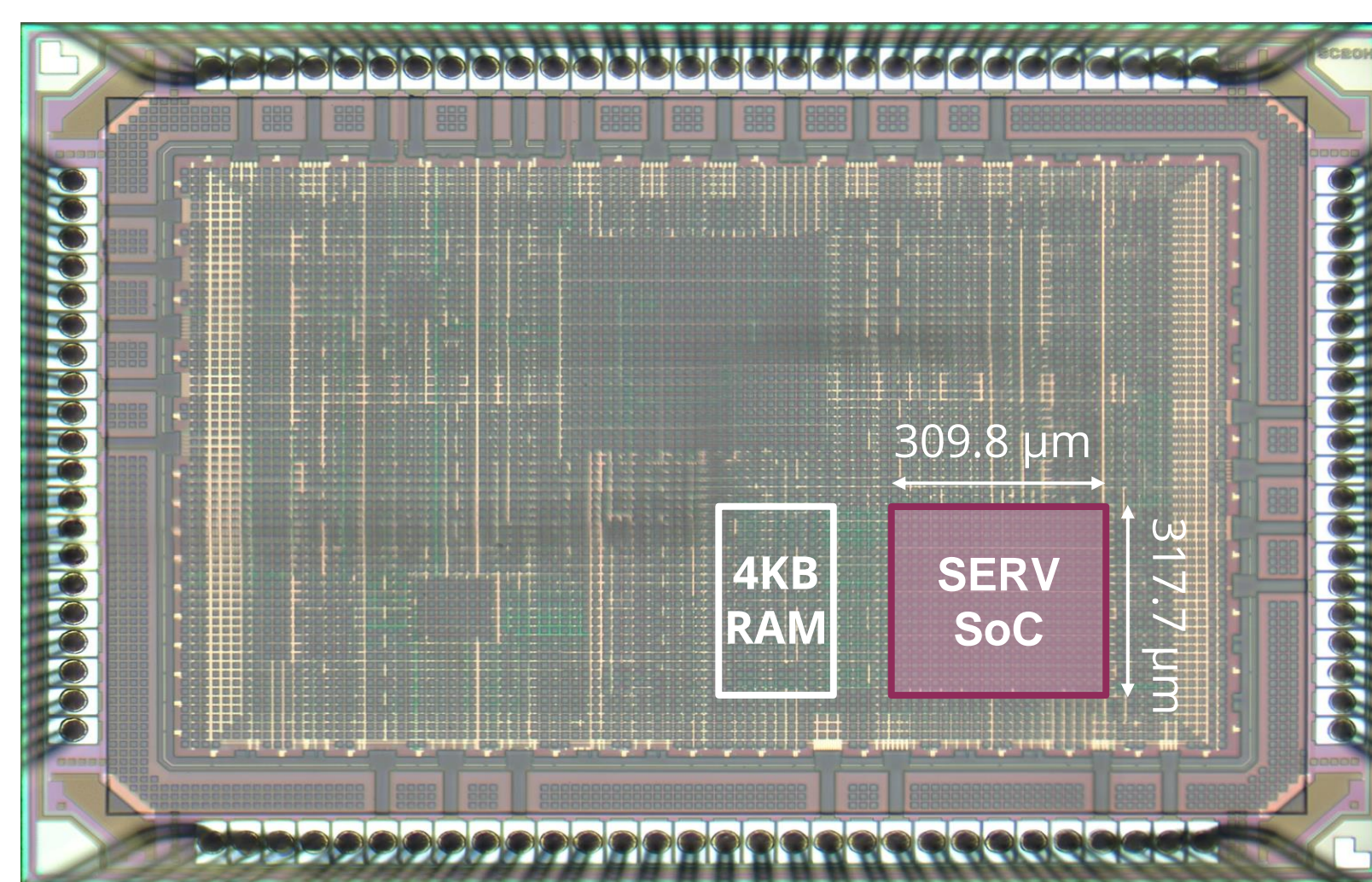


Fig. 2: SERV SoCs Micrograph.

Table I. ASIC Implementation in comparison.

|                     | Tech.      | VDD [V] | Power [ $\mu\text{W}/\text{MHz}$ ] | Leakage [ $\mu\text{W}$ ] | NAND Gate | Freq. [MHz] |
|---------------------|------------|---------|------------------------------------|---------------------------|-----------|-------------|
| [4]                 | SOTB 65nm  | 0.22    | 13.3                               | 0.049                     | 50.1k     | 14          |
| [5]                 | FDX 22nm   | 0.42    | 4.47                               | 105.4                     | -         | 18          |
| [6]                 | FDX 22nm   | 0.55    | 6.3                                | 6.6                       | -         | 40          |
| [7]                 | FDSOI 28nm | 0.4     | 3.3                                | 8.4                       | -         | 40          |
| [8]                 | FDSOI 65nm | 0.5     | 13.4                               | -                         | -         | 0.00207     |
| <b>SERV-32I</b>     | SOTB 65nm  | 0.29    | 3.53                               | 0.007                     | -         | 0.011       |
| <b>SERV-32I SoC</b> | SOTB 65nm  | 0.29    | 6.97                               | 0.03                      | 84k       | 0.011       |
| <b>SERV-32E</b>     | SOTB 65nm  | 0.29    | 2.37                               | 0.0024                    | -         | 0.01        |
| <b>SERV-32E SoC</b> | SOTB 65nm  | 0.29    | 3.11                               | 0.0037                    | 70k       | 0.01        |

## REFERENCES

- [1] K. Ishibashi *et al.*, "A Perpetuum Mobile 32bit CPU with 13.4pJ/cycle, 0.14 $\mu\text{A}$  sleep current using Reverse Body Bias Assisted 65nm SOTB CMOS technology," COOL Chips, 2014.
- [2] A. D. Mauro *et al.*, "Always-On 674 $\mu\text{W}$ @4GOP/s Error Resilient Binary Neural Networks With Aggressive SRAM Voltage Scaling on a 22-nm IoT End-Node," TCAS-I, 2020.
- [3] D. Walter *et al.*, "A 0.55V 6.3uW/MHz Arm Cortex-M4 MCU with Adaptive Reverse Body Bias and Single Rail SRAM," COOL Chips, 2020.
- [4] D. Bol *et al.*, "SleepRunner: A 28-nm FDSOI ULP Cortex-M0 MCU With ULL SRAM and UFBR PVT Compensation for 2.6-3.6- $\mu\text{W}/\text{DMIPS}$  40-80-MHz Active Mode and 131-nW/kB Fully Retentive Deep-Sleep Mode," JSSC, 2021.
- [5] D. S. Truesdell *et al.*, "A 6-140-nW 11Hz-8.2-kHz DVFS RISC-V Microprocessor Using Scalable Dynamic Leakage-Suppression Logic," SSC-L, 2021.

## ACKNOWLEDGEMENT

The VLSI chip in this study has been fabricated through the activities of VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Synopsys, Inc., Cadence Design Systems Inc., Mentor Inc., Renesas Electronics Corp., and Nippon Systemware Co., Ltd.