# RISC-V® Everywhere

Calista Redmond
CEO, RISC-V International

May 2022

**Open source and collaboration**
are strategic to software and hardware across industries and geographies.

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This is our time.
RISC-V empowers our community to seize growing opportunities

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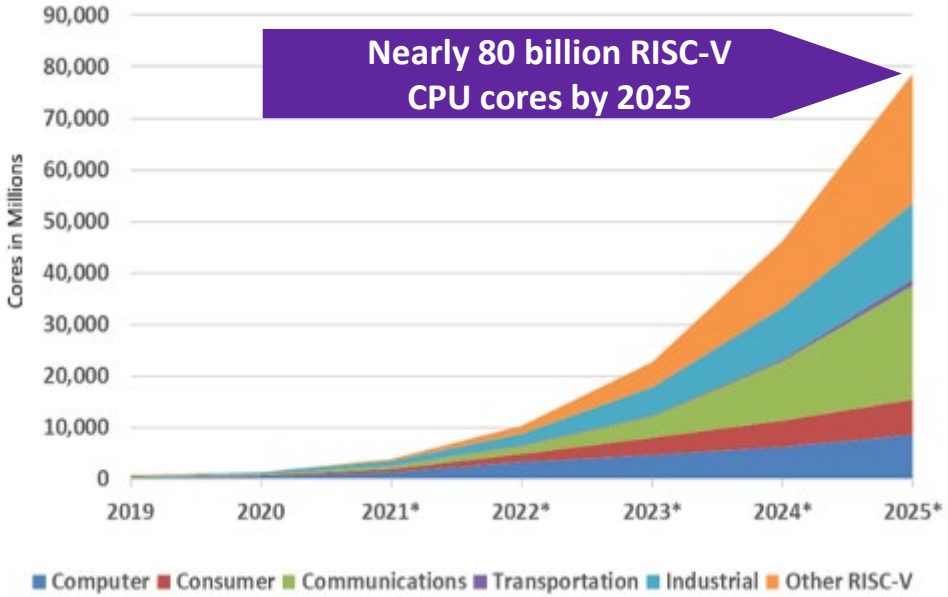
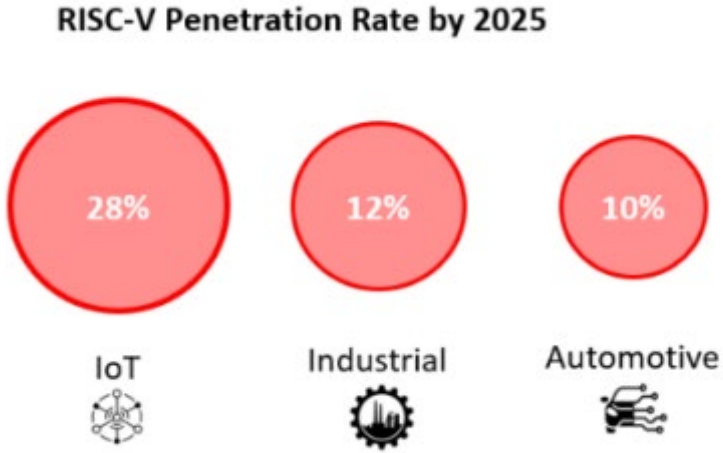
# RISC-V CPU core market grows 114.9% CAGR, capturing >14% of all CPU cores by 2025




"The rise of RISC-V cannot be ignored... RISC-V will shake up the $8.6 Billion semiconductor IP market."

-- William Li, Counterpoint Research

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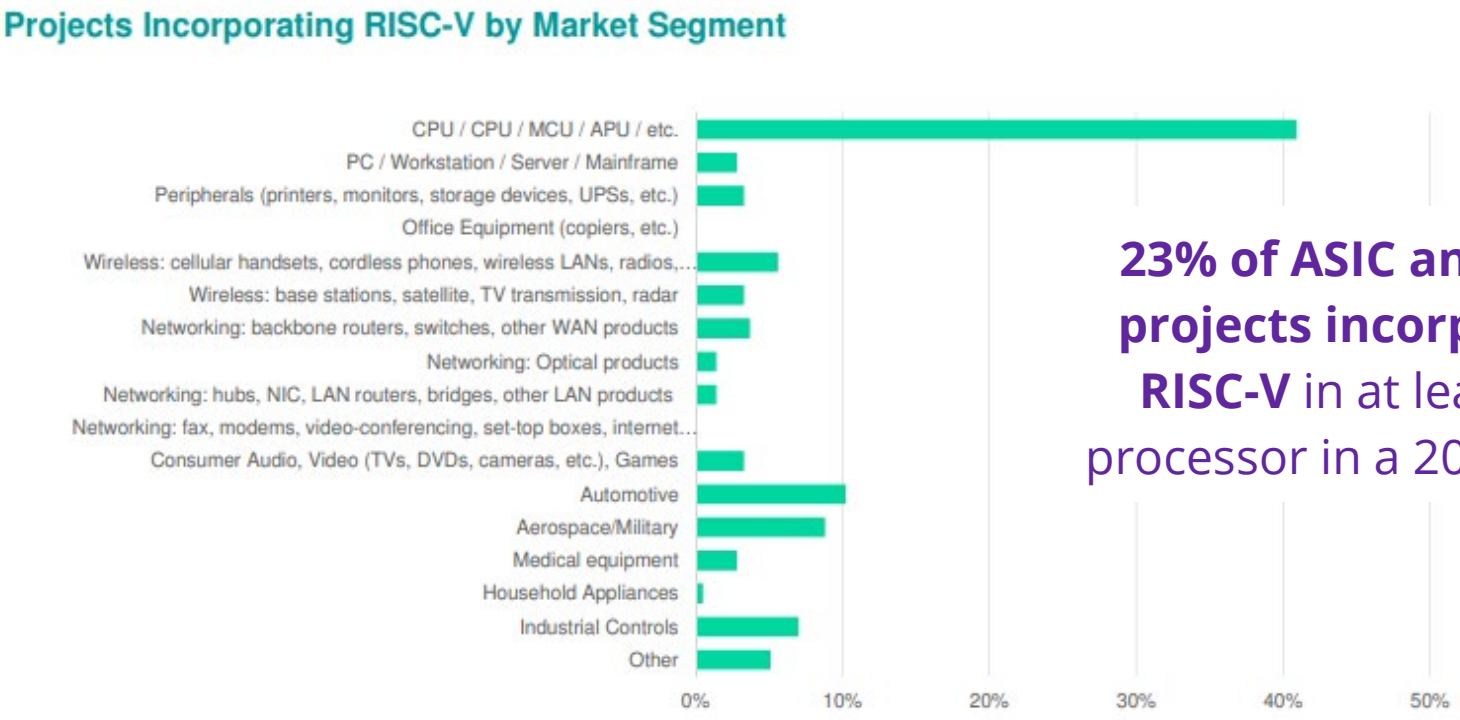
Source: Semico Research Corp, March 2021

Source: Counterpoint Research, September 2021

# Nearly a quarter of designs incorporate RISC-V




**23% of ASIC and FPGA projects incorporated RISC-V** in at least one processor in a 2020 study.

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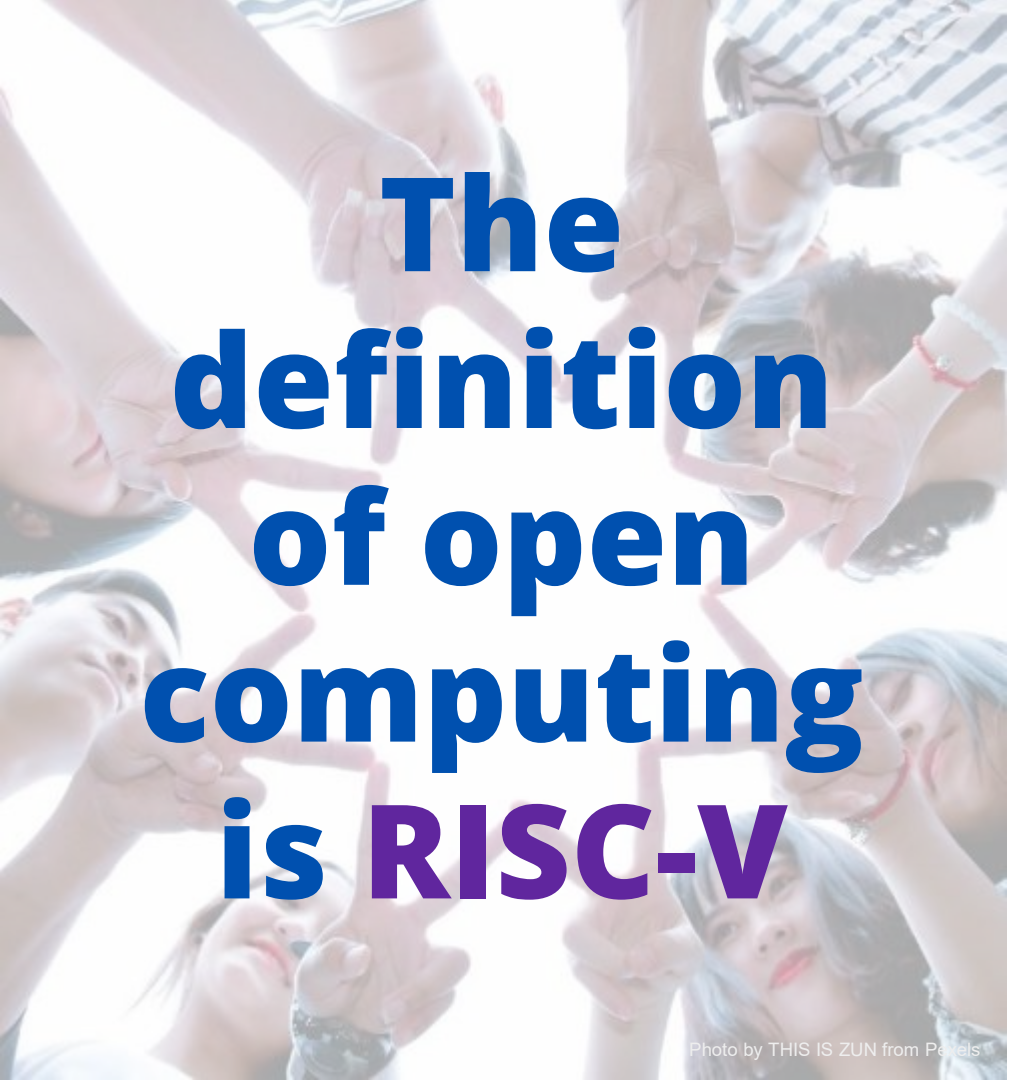
Source: Tech Design Forum, November 2020




## RISC-V is the free and open Instruction Set Architecture

- Simple, modular architecture
- Open collaboration
- Design freedom
- Strategic future

# Disruptive **Technology**

| Barriers | Proprietary | RISC-V |
|---|---|---|
| Complexity | 1500+ base instructions<br>Incremental ISA | **Simple.**<br>47 base instructions, Modular ISA |
| Design freedom | Complex and limited,<br>deep investment | **Complete freedom.**<br>Flexible, open building blocks |

| Barriers | Proprietary | RISC-V |
|---|---|---|
| License fees, Cost of entry | $$$ | **Free** |
| Design cost + constraint | $$$ – Limited | **Free – Unlimited** |
| Strategic risk | Vendor lock in and<br>dependency | **Global community.**<br>Invested stakeholders, No vendor lock in |

# Unconstrained **Opportunity**

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# 2 billion RISC-V cores in market in 2021

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"Deloitte Global predicts that

**the market for RISC-V processing cores will double in 2022 from what it was in 2021, and that it will double again in 2023**,

as the served addressable market available for RISC-V processing cores continues to expand."

December 2021

*>10 billion RISC-V cores in 2021*

industry adoption

# Investment and traction accelerate in 2022

intel

**Intel Corporation Makes Deep Investment in RISC-V Community to Accelerate Innovation in Open Computing**

RISC-V welcomes Intel to the Board of Directors to collaborate on RISC-V IP

**Intel Creates $1B Innovation Fund To Grow RISC-V Market (And Attract New Foundry Customers) | Karl Freund, Forbes**

February 7, 2022

European Commission

The European Commission [announced a new European Chips Act of €15 billion in additional public and private investments until 2030](). This adds to €30 billion of public investments previously earmarked.

Tue, Feb 8 2022

**SiFive**
@SiFive

We're thrilled to be featured on the @Nasdaq video wall this morning to celebrate our historic moment: a $2.5B valuation from our Series F round! #RISCV #NoLimits


10:02 am · 16 Mar 2022 · HubSpot

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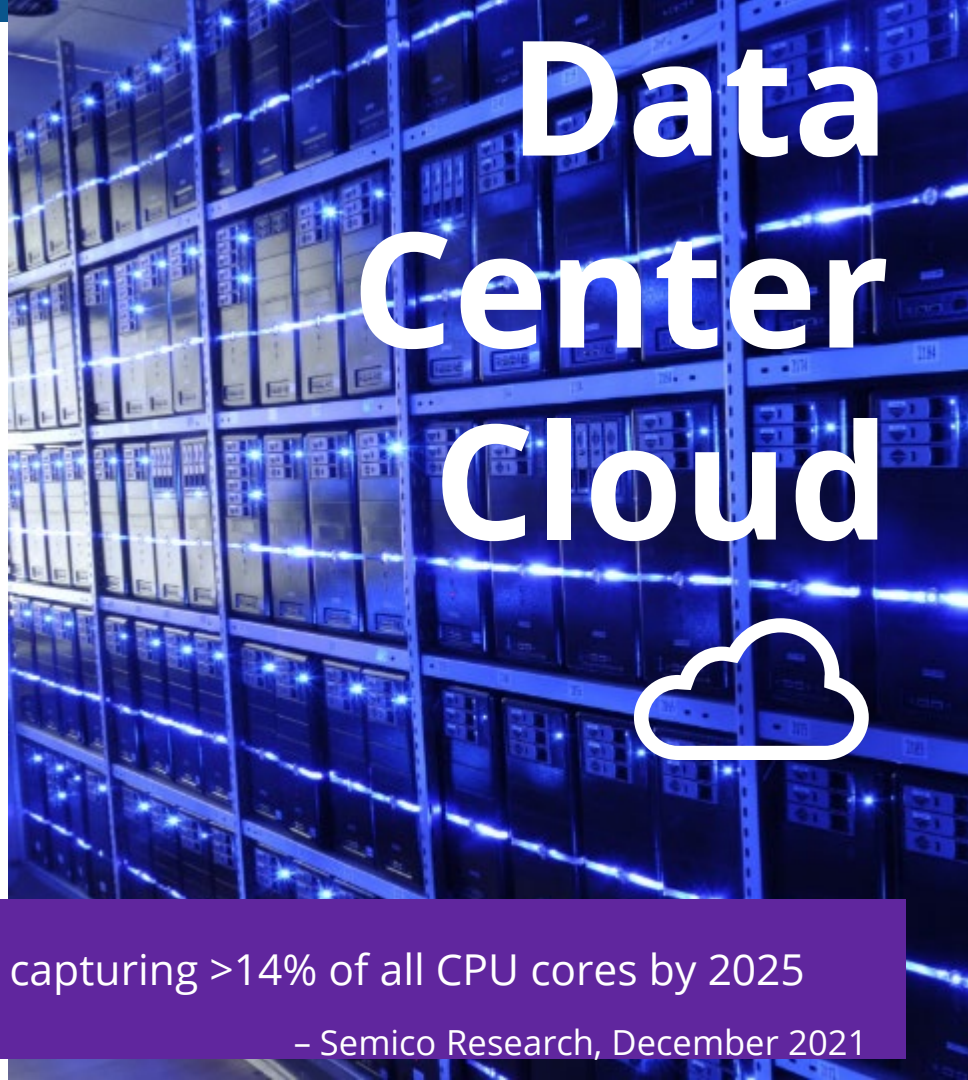
# Data Center Cloud



- **Esperanto** 1,000-Core RISC-V AI accelerator.
- **Alibaba** RISC-V Xuantie processors with 4 open source cloud and edge processors
- **Imagination** RISC-V CPU family, for discrete and heterogeneous computing
- **Seagate** hard disk drive controller with high-performance RISC-V CPU.
- **Ventana** performance chiplet approach to data center SoC design
- **Intel** Nios processor based on RISC-V, designed for performance.

RISC-V CPU core market will grow 115% CAGR, capturing >14% of all CPU cores by 2025

– Semico Research, December 2021

# Telecom & Communications

Communication AI SoC RISC-V designs will grow 21.2% CAGR from 2019-27
– Semico Research, December 2021

- **Andes** RISC-V processor adopted by SK Telecom for AI products.
- **Alibaba** supporting Android 12 on their 64-bit RISC-V core emulated in QEMU
- **Sipeed** RISC-V chip runs Android 10, RV64 phone coming next
- **Alibaba** ported TensorFlow Lite for AI image, audio, and optical in smart devices.
- **Google** Pixel 6 Titan M2 RISC-V processor, with extra speed and memory, more resilient to advanced attacks.

- **MobileEye** vision-based advanced driver assist systems chips capable of 176 trillion ops per second with 12 RISC-V CPU cores.
- **Andes** ISO 26262 Functional Safety ASIL D Dev Process Certification for RISC-V embedded automotive safety with Andes processors
- **Imagination Technologies** GPU linked by a RISC-V core for ASIL-B level designs with ISO 26262 safety critical certification.
- **IAR Systems** extended functional safety of its Embedded Workbench sw tool chain to the RISC-V core of NSITEXE, subsidiary of automotive leader Denso.
- **Europe GaNext** simplifies power converters with GaN power semiconductors with better efficiency and compactness for EV chargers.

# Automotive

2020 RISC-V automotive opportunity 4M cores; growing to 150M cores in 2022 and 2.9B cores by 2025.

– Deloitte, December 2021

RISC-V will capture 10% of the Automotive market by 2025

– Counterpoint, September 2021

# Consumer, IoT devices

- **Huawei** Hi3861 RISC-V board for Harmony OS developers for IoT
- **Zepp Health** / Huami wearable manufacturer OS supporting RISC-V Reference Models for RISC-V P extension
- **GreenWaves** ultra-low power GAP9 hearables platform for scene-aware and neural network-based noise reduction.
- **RIOS Lab** announced PicoRio, an affordable RISC-V open source small-board computer.
- **SiFive** world's fastest development board for RISC-V Personal Computers.

RISC-V will command 28% of the IoT market by 2025

– Counterpoint Technology Market Research, September 2021

# RISC-V-based AI SoCs will grow **73.6% CAGR to 25B units and $291B in revenue by 2027**

– Semico Research, December 2021

- **Alibaba Cloud** tops MLPerf Tiny v0.7 Benchmark with its IOT processor
- **StarFive** released the world's first RISC-V AI visual processing platform
- **Andes** released superscalar multicore and L2 cache controller processors.
- **NVIDIA CUDA** support on Vortex RISC-V GPGPU enables scaling from 1-core to 32-core GPU based on RV32IMF ISA with OpenCL 1.2 graphics API support.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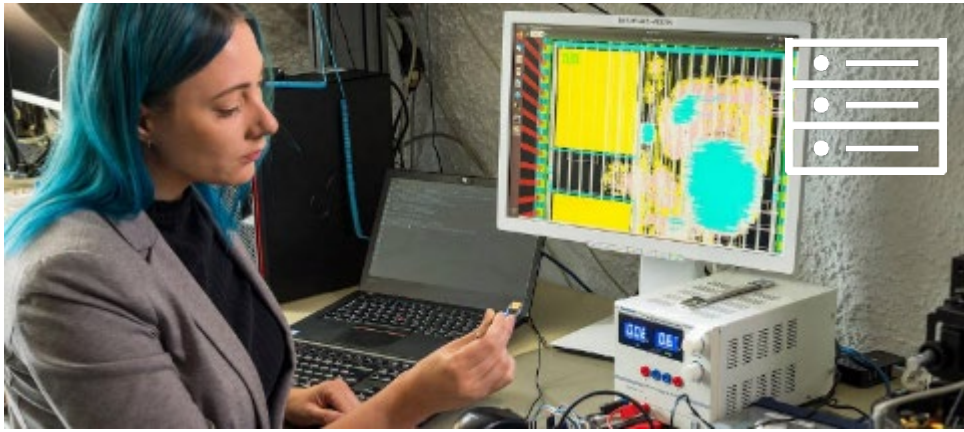
# Edge Computing

- **Fraunhofer** ported Tensorflow lite to their RISC-V processor core for Edge AI applications incl sensor data evaluation, gesture control, or vibration analysis.
- **Seeed Studio**'s new Sipeed MAIX, a RISC-V 64 AI board for Edge Computing makes it possible to embed AI to any IoT device.
- **Micro Magic** announced an incredibly fast 64-bit RISC-V core achieving 5GHz and 13,000 CoreMarks at 1.1V.
- **Western Digital** SweRV Core enables spectrum of compute at the edge
- **Microchip** released the first SoC FPGA development kit based on the RISC-V ISA.

# High Performance Computing

- **E4** Monte Cimone Cluster along with DEI-UNIBO contributing to architecture, software, and integration.
- **European Processor Initiative** RISC-V accelerator with first chip Sep 2021
- **Technical University of Munich** (TUM) quantum cryptography chip for quantum computing security demands
- **Tactical Computing Labs** HPC-centric software test suite for GCC and LLVM
- **Cortus** is developing a high-performance RISC-V Out-of-Order processor core for the European eProcessor project.
- **De-RISC** HW-SW platform for multi-core RISC-V SoC for safety critical aerospace



Johanna Baehr of TUM heads a team that has hidden four hardware Trojans on this chip - malicious functions that are integrated directly into the circuits.

Image: Astrid Eckert / TUM

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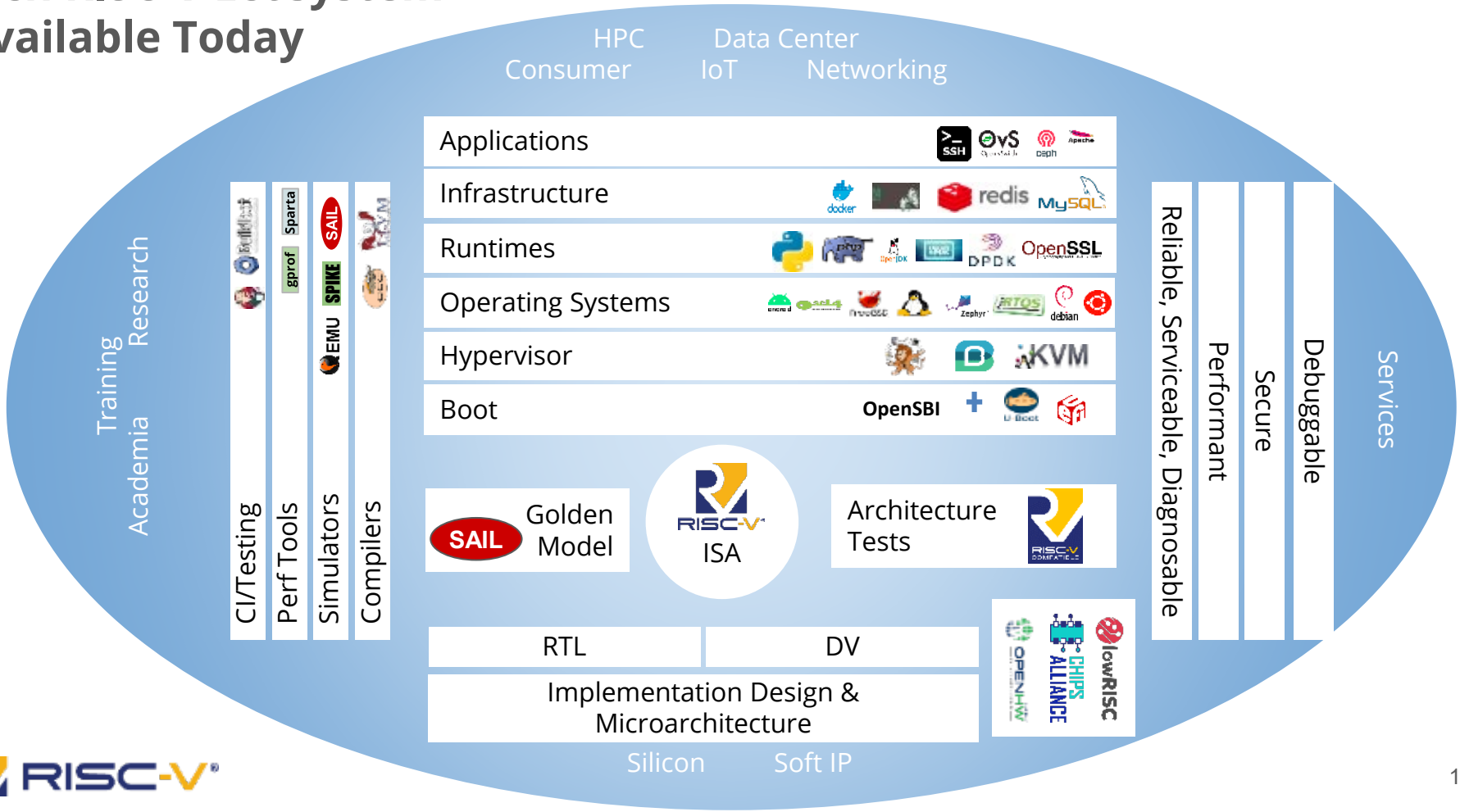
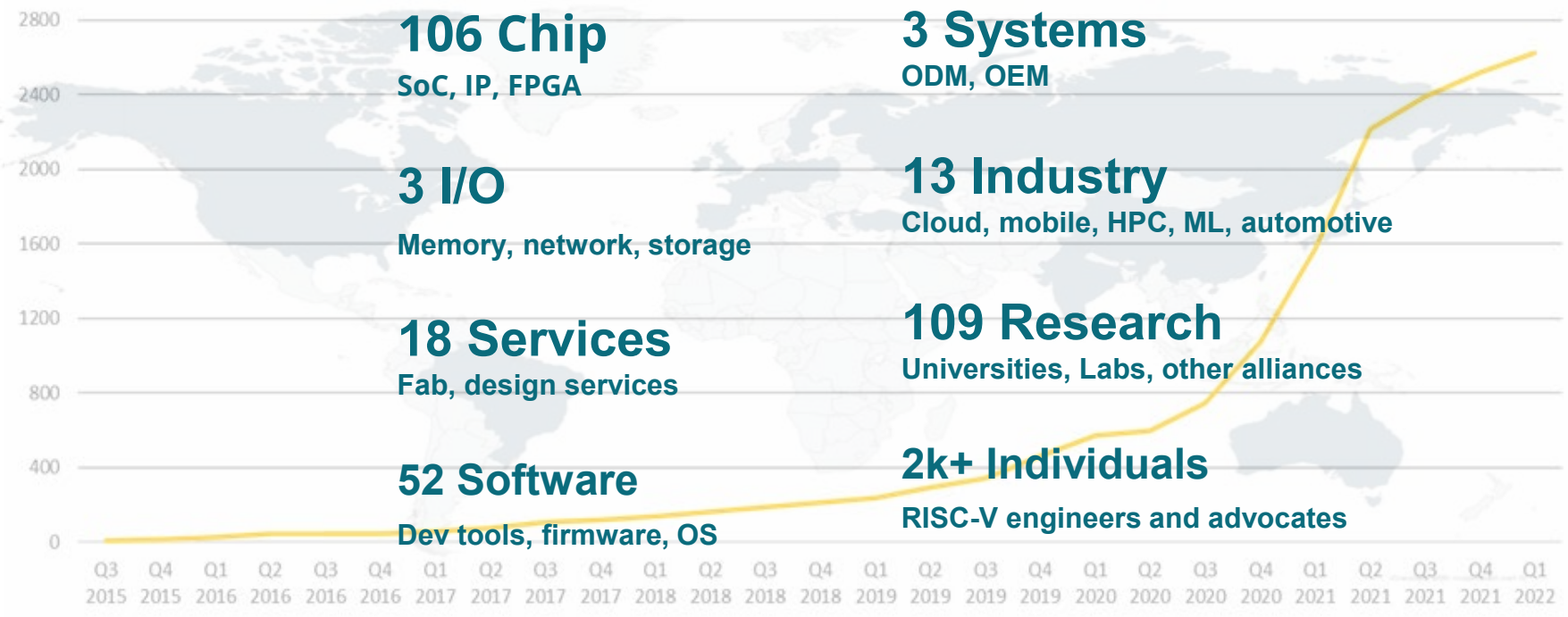
# Rich RISC-V Ecosystem Available Today



# More than 2,700 RISC-V Members
## across 70 Countries




**106 Chip**
SoC, IP, FPGA

**3 I/O**
Memory, network, storage

**18 Services**
Fab, design services

**52 Software**
Dev tools, firmware, OS

**3 Systems**
ODM, OEM

**13 Industry**
Cloud, mobile, HPC, ML, automotive

**109 Research**
Universities, Labs, other alliances

**2k+ Individuals**
RISC-V engineers and advocates

Mar 2022

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**RISC-V membership rapid growth of 134% in 2021**

## Technical Deliverables

Technical **governance**
Build **technical deliverables**
Guide strategic technical **Work groups**

## Compatibility & Verification

Profiles & Platforms & Architecture Compatibility Tests (ACT) & Platform Compatibility Tests (PCT)

## Visibility

**Amplify** member news, content, and success with press and analysts
**Original** content programs
RISC-V, industry, and regional **events**

## Learning & Talent

Multi-level **online learning**
Connecting **universities** with labs, tests, and curricula
RISC-V **Training Partners**
**Jobs and internships**

## Advocacy + Alliances

RISC-V **Ambassadors**
Geo and industry **alliances**
**Local** developer groups and events

## Marketplace Exchange

**Online marketplace** of providers, products, services, and learn
Technical **developer forums**

# RISC-V delivers incredible member support

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# RISC-V Innovation Roadmap

## Ecosystem

| 2010-2016 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 → |
|---|---|---|---|---|---|---|
| Test Chips<br>Software tests<br>Linux port | Proof of Concept SoCs<br>Minion processors for power management & communications<br>Bare metal software | IoT SoCs<br>Microcontrollers<br>RTOS, Firmware<br>Development tools<br>Technical Steering Committee,<br>HPC SIG, GlobalPlatform partnership | | AI SoCs, Application processors, Linux Drivers, AI Compilers<br>**SIGS**: Security Response, AI, Graphics, Android, Embedded, Datacenter/Cloud, Blockchain, Simulators, Managed Runtimes, Android, Functional Safety<br>**Programs**: Dev Board Seed, Development Partners, RISC-V Labs | **SIGS**: Vector, Perf Modeling, Perf Analysis, Trusted Computing, Control Flow Integrity, Memory Protection, Microarchitecture Side Channel, QOS, E2E Data Integrity, Error Handling, Automotive, Communications, Floating Point, Vector<br>**Security specs**; RISC-V Security Model, AP-TEE, IOPMP<br>**Platform specs**: Platforms, SEE, SBI, ABI, Discovery,Watchdog, ACPI, UEFI<br>**SOC specs**: E-Trace, Nexus, IOMMU | |

## ISA Extensions

| | | | | | | |
|---|---|---|---|---|---|---|
| ISA Definition<br>RISC-V Foundation | RV32 | RV32I and RV64I<br>Base instructions: Integer, float,double, quad, atomic, and compressed instructions<br>Priv modes, Interrupts, exceptions, memory model, protection, and virtual memory | Architecture Compatibility Framework<br>Trace | Vector<br>Crypto Scalar<br>Bitmanip<br>Hypervisor<br>ePMP<br>Cache Mgt<br>Virtual Memory<br>Zfh<br>Zfinx<br>Zihintpause | Profiles<br>Packed SIMD<br>Advanced Interrupts<br>Java: ptr masking, I/D synch<br>RV32E & RV64E<br>Bfloat16<br>Vector Half-Precision Floating Point<br>Code Size<br>Crypto Vector<br>Fast Interrupts<br>SMPU<br>Zmmul<br>Ztso<br>Zihintntl | Matrix Ops<br>Crypto Gost |

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# Investments in open source bring a 4x return

**EU companies invested €1 billion** in Open Source Software in 2018, providing economic impact of €65 - €95 billion, with a cost-benefit ratio of >1:4.

# Technical advantage

**Lower maintenance costs.** Contributing to upstream projects ensures technical elements will be included in future updates without ongoing development costs.

**Influence direction.** New features come from contributions. To include functionality important to your organization, you need to support active project contributors.

# Talent matters

**Open source saves time and money.** Developers can save ~45 minutes a day with open source. For an organisation of 1,800 people, this can be financial savings of $12.4 million over three years.

**Attract, retain, and build technical talent and collaborative culture.** 48% of businesses contributed to open source projects to access developer talent. Employees relationships and identify good fits for your company while working on their favorite project.

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RISC-V is a community of passionate, dedicated, and invested stakeholders

**As individuals**
**As companies**
**As universities**
**As public institutions and non-profits**
**As nations**

As one Global, connected movement

# Build RISC-V into your company strategy, and your personal mission

# Thank You

www.riscv.org

@risc_v
@calista_redmond

risc-v-international
calistaredmond

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# Benefits of engaging in RISC-V

- ✓ **Accelerate technical traction** and insight
- ✓ **Contribute** technical priorities, approaches, and code
- ✓ Gain strategic and **technical advantage**
- ✓ **Increase visibility**, leadership, and market insight
- ✓ Fill and increase **engineering skills**, retain and attract talent
- ✓ Build **innovation partner** network and customer pipeline
- ✓ **Deepen, engage, and lead** in local and industry developer network
- ✓ **Showcase RISC-V products**, services, training, and resources

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# Membership Options

RISC-V Membership details may be found online here

## Premier Member Benefits

- Board seat and Technical Steering Committee seat included at $250k level
- Technical Steering Committee seat included at $100k level
- Board level includes seat on RISC-V Legal Committee
- Eligible to lead workgroup and/or committee

- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Premier members
- Solution / Product listing highlighted on RISC-V Exchange, noted with member level
- 4 case studies a year
- 2 blogs per month
- 2 social media spotlights per month
- Spotlight member profile
- Event sponsorship discount

### Premier Requirements

- Membership open to any type of legal entity
- $250k Annual membership fee that includes Board seat and TSC seat
- $100k Annual membership fee that includes TSC seat

## Strategic Member Benefits

- 3 Board reps elected for the Strategic tier, including Premier members that do not otherwise have a board seat
- Eligible to lead workgroup and/or committee

- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Strategic members
- Solution / Product listing highlighted on the RISC-V Exchange, noted with member level
- 1 case study a year
- 1 blog per month
- 1 social media spotlight per month
- Event sponsorship discount

### Strategic Member Requirements

- Membership open to any type of legal entity
- Annual membership fee based on employee size
  - 5,000+ employees: $35k
  - 500-5,000 employees: $15k
  - <500 employees: $5k
  - <10 employees & company <2 yrs old: $2k

## Community Member Benefits

- Two Board representatives
- 1 Community Board representative, elected
- 1 Individual Board representative, elected

- Member logo / name listing on RISC-V website, by member level
- 1 case study a year
- 1 blog per quarter
- 1 social media spotlight per quarter
- Event sponsorship discount

### Community Requirements

- Membership open to
  - academic institutions,
  - non-profits,
  - individuals not representing a legal entity
- No annual membership fee

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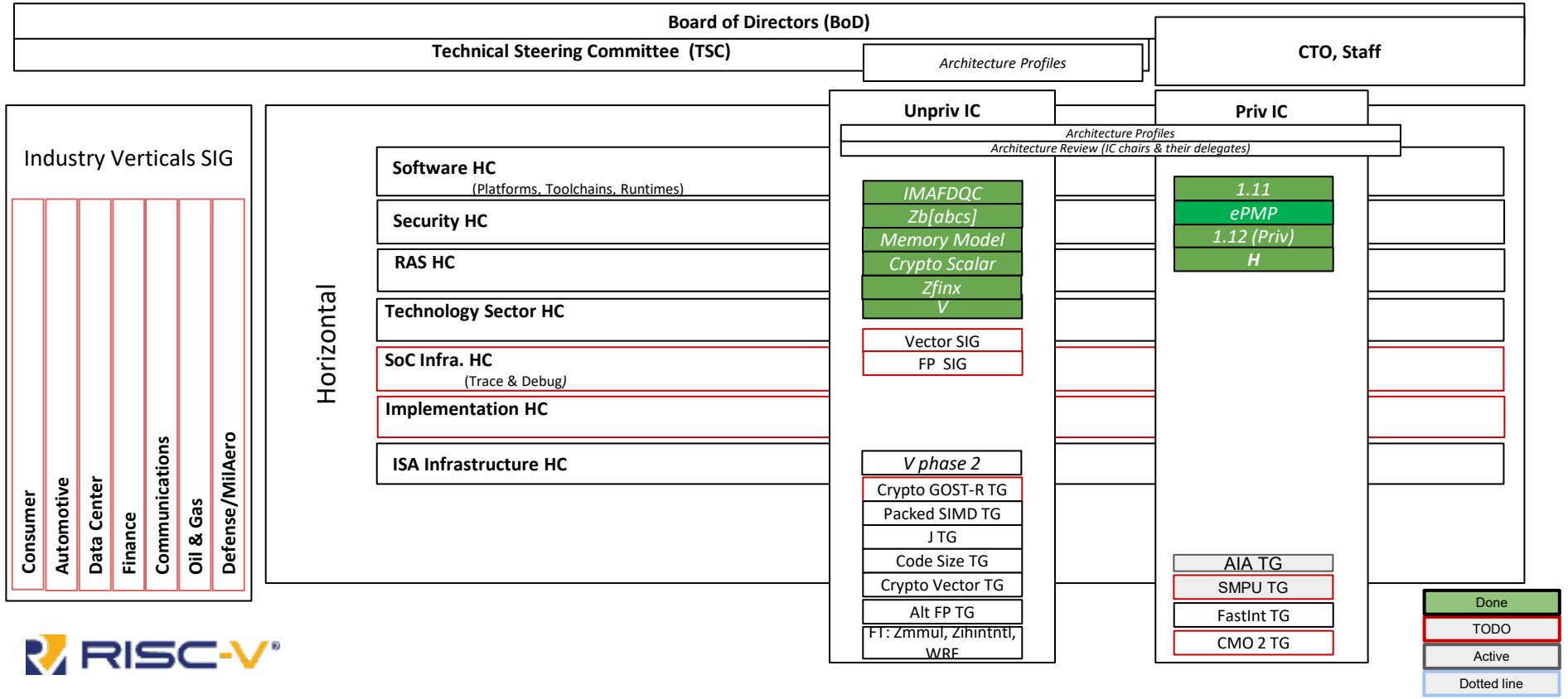
# Technical Organization



# Software Horizontal Committee

AI/ML/NLP/Graphics SIG

Android SIG

Perf Modeling SIG

Perf Analysis SIG

IOMMU TG

## Platform HSC

(includes platform specs)

Config TG

Hypervisors SIG

AIA TG

IOPMP TG

OS-A Platform SIG

RVM-CSI Platform TG

OS-A SEE TG

OS-A PlatformTG

OS-A PCT TG

Topics TODO:

- Linux class OSs
- RTOSs
- DMA
- Multi-processing
- JITs
- IOMMU, Buses
- Bootloaders
- Distro coordination/build/rel
- QOS
- Perf monitoring

TGs for specs underway

## Toolchain & Runtimes HSC

psABI TG

Topics TODO:

- Benchmarks
- Regression test strategy
- Ecosystem changes
- Extensions needed
- Worst Case Execution Time (WCET)
- Spatial & Timing interference
- DSP
- DB & Hadoop et al
- Performance analysis
- Native code
  - GCC
  - LLVM
  - Optimizer
  - Profiler
  - gdb

Code Size TG

HPC SIG

Managed Runtimes SIG

Done

TODO

Active

Dotted line

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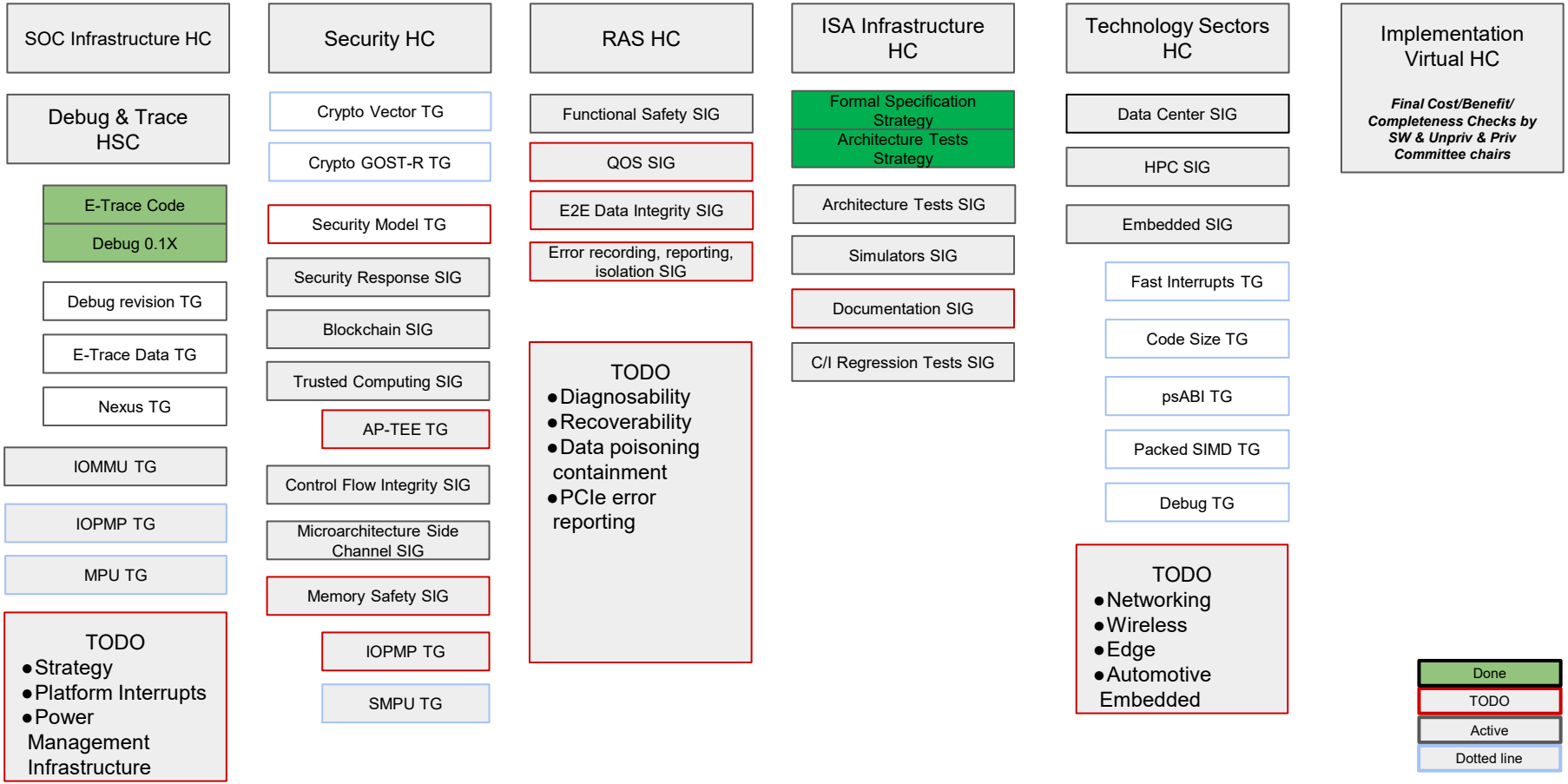
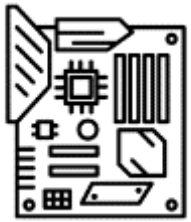

SOC Infrastructure HC
Debug & Trace HSC
E-Trace Code
Debug 0.1X
Debug revision TG
E-Trace Data TG
Nexus TG
IOMMU TG
IOPMP TG
MPU TG
TODO
Strategy
Platform Interrupts
Power Management Infrastructure
Security HC
Crypto Vector TG
Crypto GOST-R TG
Security Model TG
Security Response SIG
Blockchain SIG
Trusted Computing SIG
AP-TEE TG
Control Flow Integrity SIG
Microarchitecture Side Channel SIG
Memory Safety SIG
IOPMP TG
SMPU TG
RAS HC
Functional Safety SIG
QOS SIG
E2E Data Integrity SIG
Error recording, reporting, isolation SIG
TODO
Diagnosability
Recoverability
Data poisoning containment
PCIe error reporting
ISA Infrastructure HC
Formal Specification Strategy
Architecture Tests Strategy
Architecture Tests SIG
Simulators SIG
Documentation SIG
C/I Regression Tests SIG
Technology Sectors HC
Data Center SIG
HPC SIG
Embedded SIG
Fast Interrupts TG
Code Size TG
psABI TG
Packed SIMD TG
Debug TG
TODO
Networking
Wireless
Edge
Automotive Embedded
Implementation Virtual HC
Final Cost/Benefit/ Completeness Checks by SW & Unpriv & Priv Committee chairs
Done
TODO
Active
Dotted line

# RISC-V Technical Programs



**RISC-V Developer Boards**
Available to spur innovation, provide hands-on education, and engage early adopters to test and develop.


**RISC-V Development Partner**
Recognizes the investment and dedication of organizations making significant technical contributions to RISC-V.


**RISC-V Lab**
Institutions that host a lab with RISC-V hardware for CI/testing and general availability sandboxing.


**RISC-V Compatible**
Architectural Tests created to help ensure that software written will run on implementations that comply with that profile. Branding available for compatibility.

**RISC-V Platform**
A common, reusable runtime environment that operating systems and applications can target to improve portability and reuse. Provides interoperability assurance.

**RISC-V Profiles**
Refers to a base ISA and one or more extensions that are specified as a group so that applications can be compiled once, run on different implementations, and get the same results.

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https://wiki.riscv.org/display/TECH

# Visibility Opportunities

## Events

RISC-V and Industry events

Local, regional, and global events

Speaking opportunities

Showcase and announce RISC-V solutions

Networking

Host your own RISC-V Event

## Content

The RISC-V blog program showcases leadership, industry commentary, and technical information.

To submit content, fill out the Google Form or email content@riscv.org.

## Proactive AR / PR

Share member and community news "In the News"

RISC-V provides quotes for member press releases

Participate in media panels and interviews

## Social

Twitter LinkedIn

Members submit original content for posting on RISC-V social channels

Members and the community submit content for re-sharing.

Amplify member announcements via social

To submit content, fill out the Google Form or email content@riscv.org.

## Exchange

Promote member and community solutions

Connect developer community

## Case Studies

Elevate technical conversations to business objectives and challenges, showing adoption of RISC-V.

Case studies on riscv.org are shared to media channels and analysts.

## Engage!

RISC-V Marketing Committee
RISC-V Events Committee
RISC-V Content Committee

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# Community and Learning

## Alliances

Alliances are Technical and strategic relationships across industries, geographies, and technical domains providing mutual community support

## Ambassadors

RISC-V Ambassadors are the technical experts and leaders in the RISC-V community. They work together with RISC-V to help drive our global momentum and adoption of RISC-V technologies.

Meet the Ambassadors

## Learn

There are many materials to help you learn or teach RISC-V, including trainings, published books, technical and scholarly articles written around the world, and a lengthy collection of open educational materials provided by our community.

University resources

Online Courses

Training Partners

## Talent

RISC-V paid Mentorships are offered quarterly with projects submitted by members and open applications to the community.

Looking for a job or want to post a RISC-V related job? Check our the Careers page!

Open Hardware Diversity Alliance bringing together the open hardware community to support the professional advancement of underrepresented individuals in open source hardware.

Travel scholarships offered for RISC-V Summit.

## Engage!

RISC-V Academia + Training SIG

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