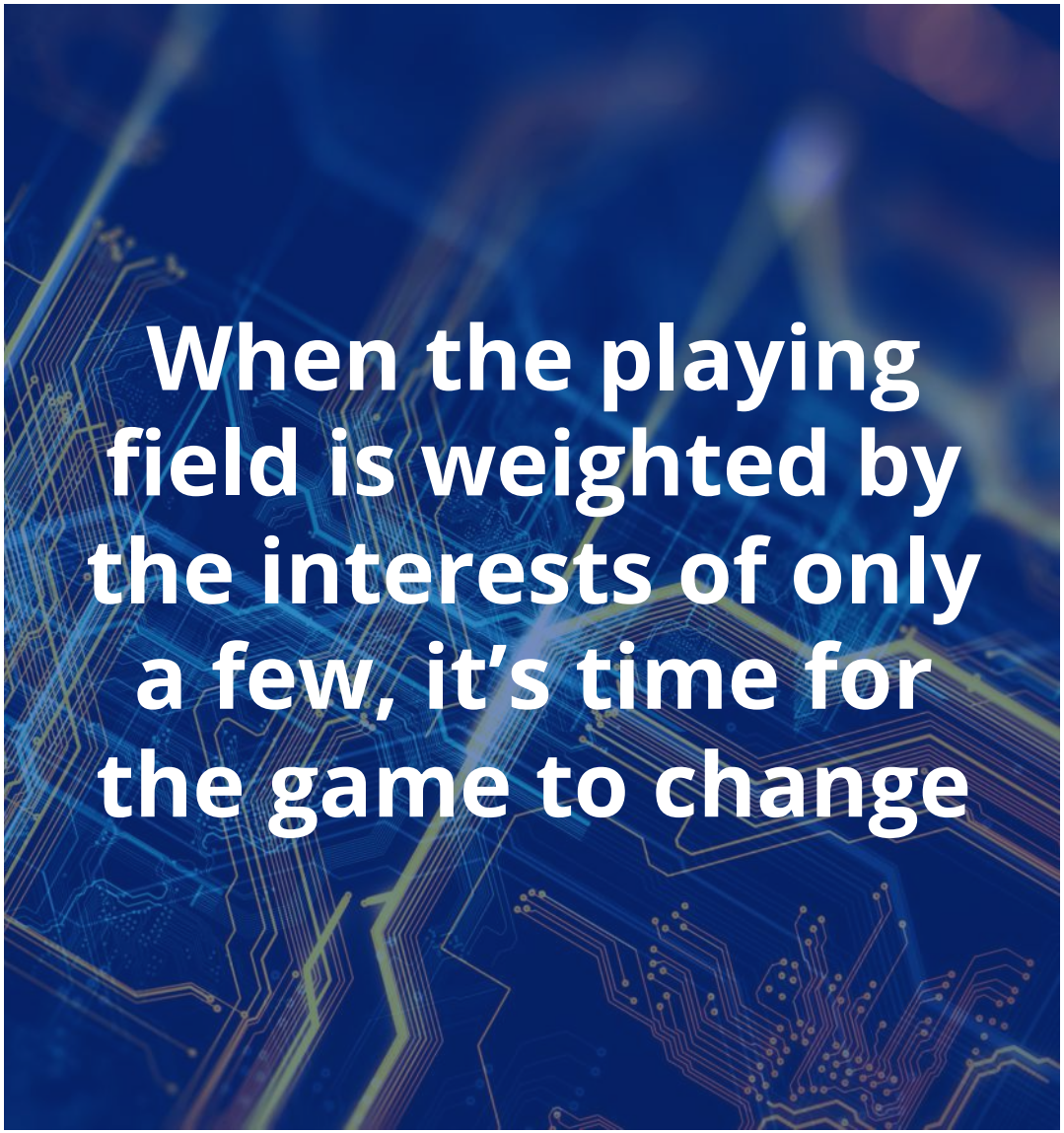
RISC-V Unconstrained

Technology. Opportunity. Community.

Calista Redmond
CEO, RISC-V International

Our world is shaped

- ... through positive inventions and negative disruptions
- ... through advances in technology and new business models
- ... through economic and political setbacks



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Reshaping history
is about removing barriers,
coming together, and
taking a united approach

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Disruptive **Technology**

Barriers	**Legacy ISA**	**RISC-V ISA**
Complexity	1500+ base instructions Incremental ISA	47 base instructions Modular ISA
Design freedom	$$$ – Limited	Free – Unlimited
License and Royalty fees	$$$	Free
Design ecosystem	Moderate	Growing rapidly. Numerous extensions, open and proprietary cores
Software ecosystem	Extensive	Growing rapidly

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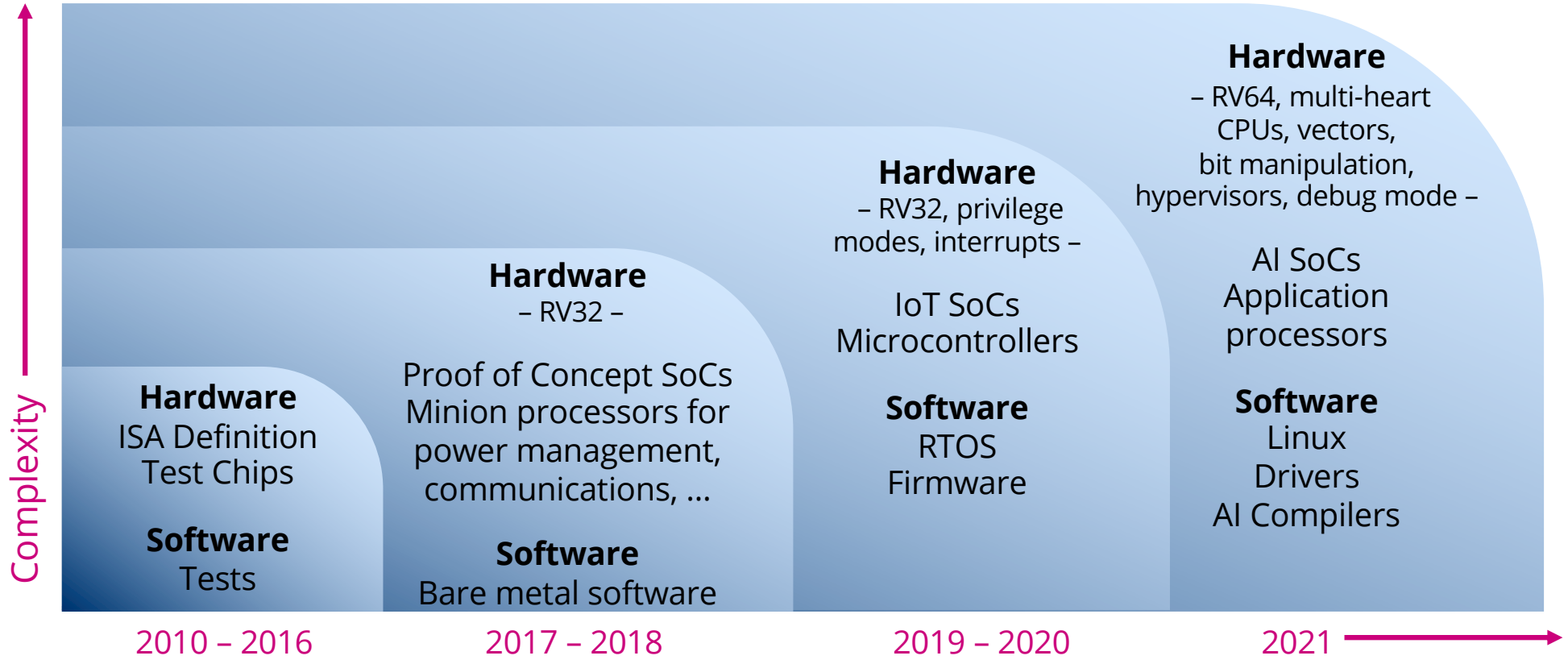
Industry innovation on RISC-V



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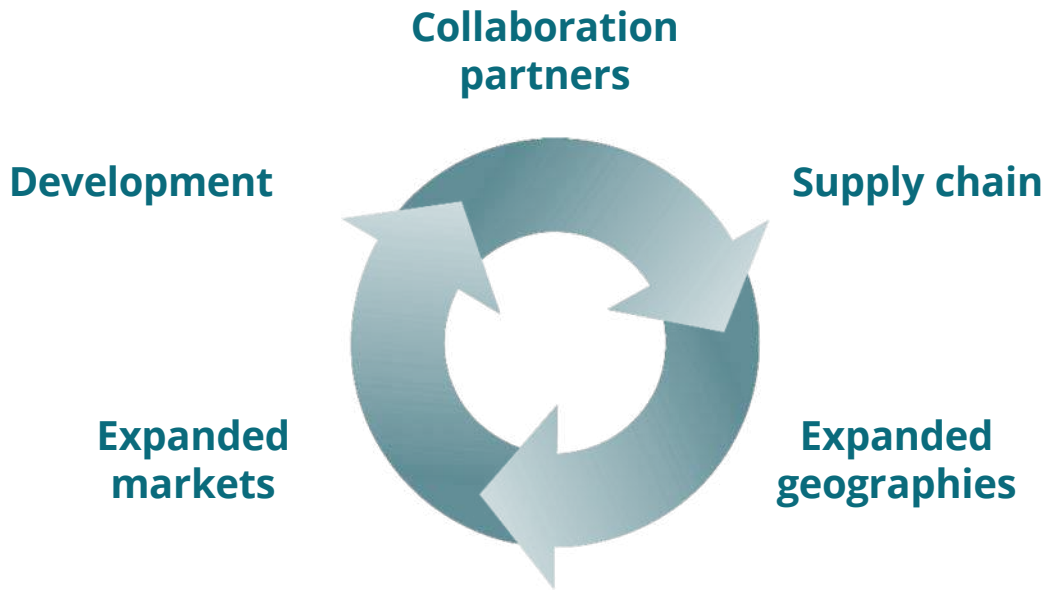
Unconstrained **Opportunity**

Barriers removed

- Design risk
- Cost of entry
- Partner limitations
- Supply chain

RISC-V Business Model



Beyond removing barriers, RISC-V fuels our community to seize growing opportunities

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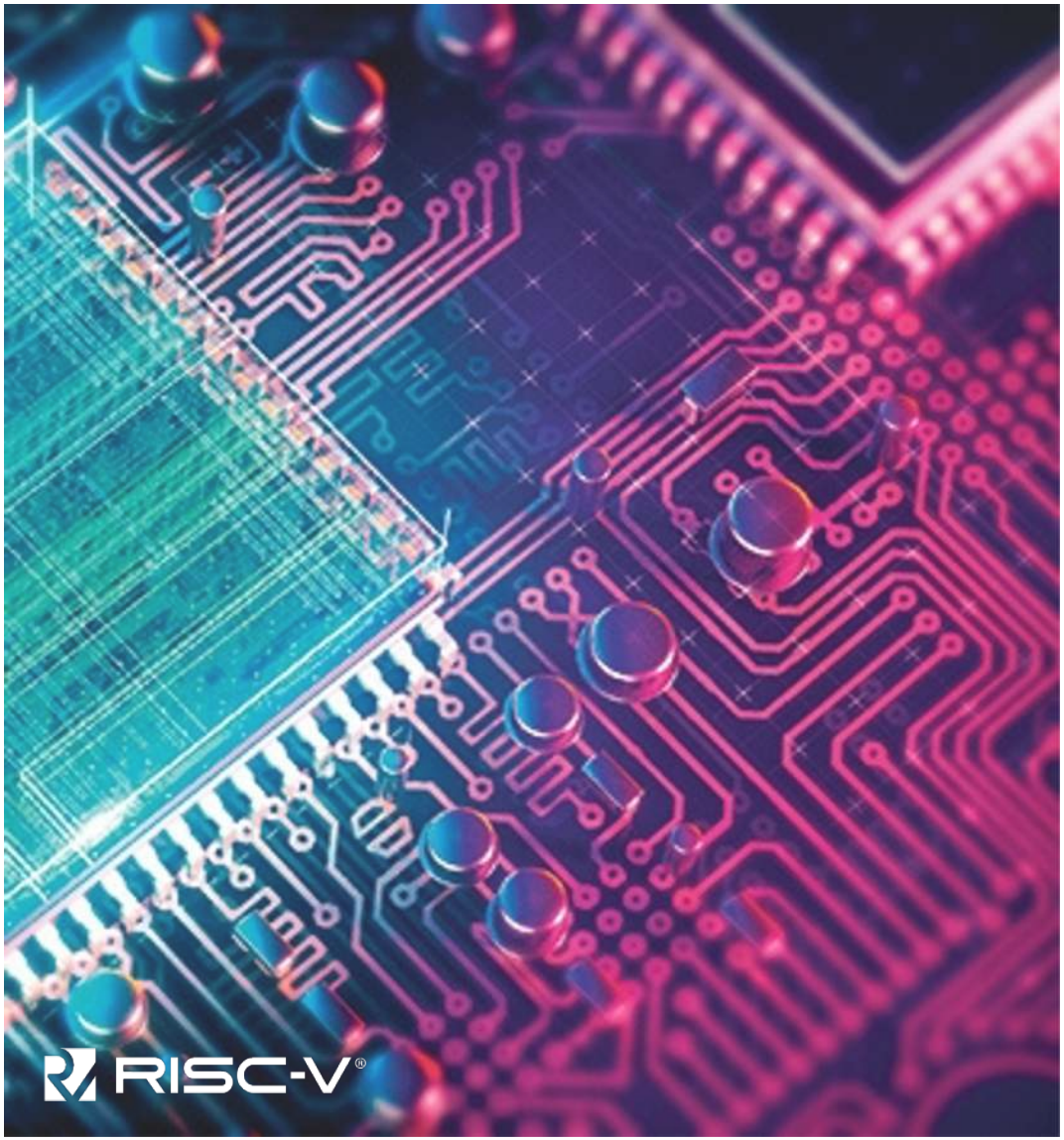


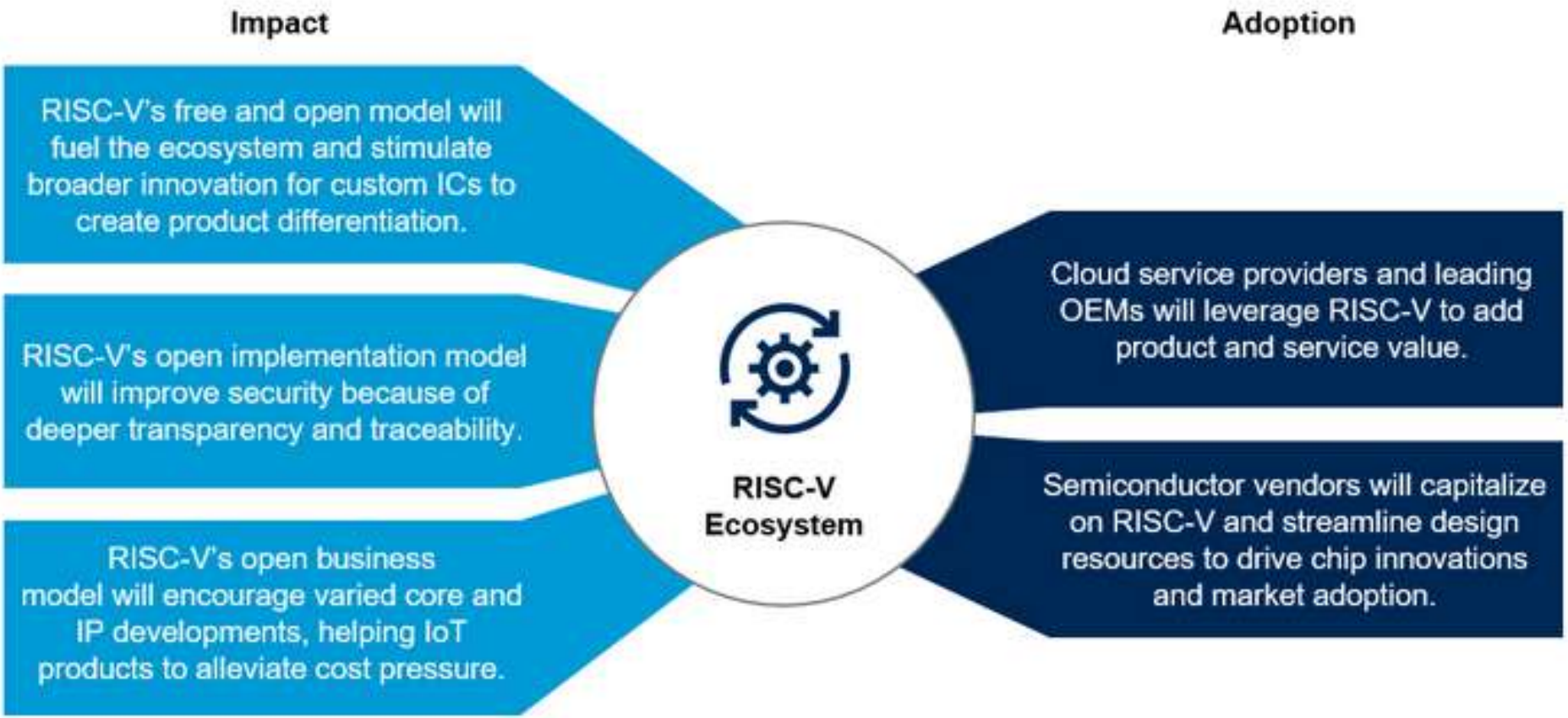
By 2025, 40% of application-specific integrated circuits (ASICs) will be designed by OEMs, up from around 30% today.

Custom ICs Based on RISC-V Will Enable Cost-Effective IoT Product Differentiation

Gartner, June 2020

Source: Gartner

Impact and Adoption of Open ISA RISC-V



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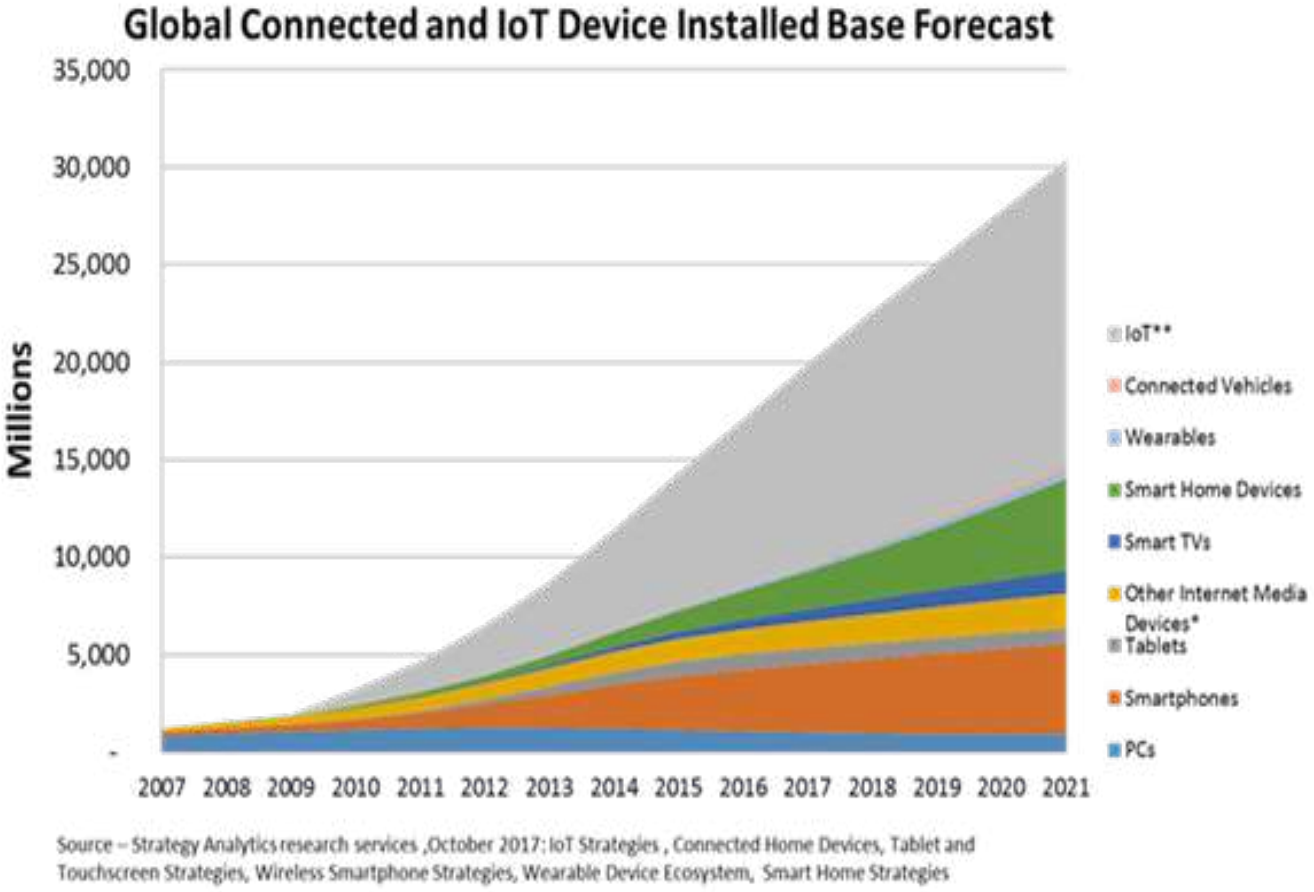
Source: Gartner
ID: 46523_C

30 billion connected and IoT devices

demand security and custom processors



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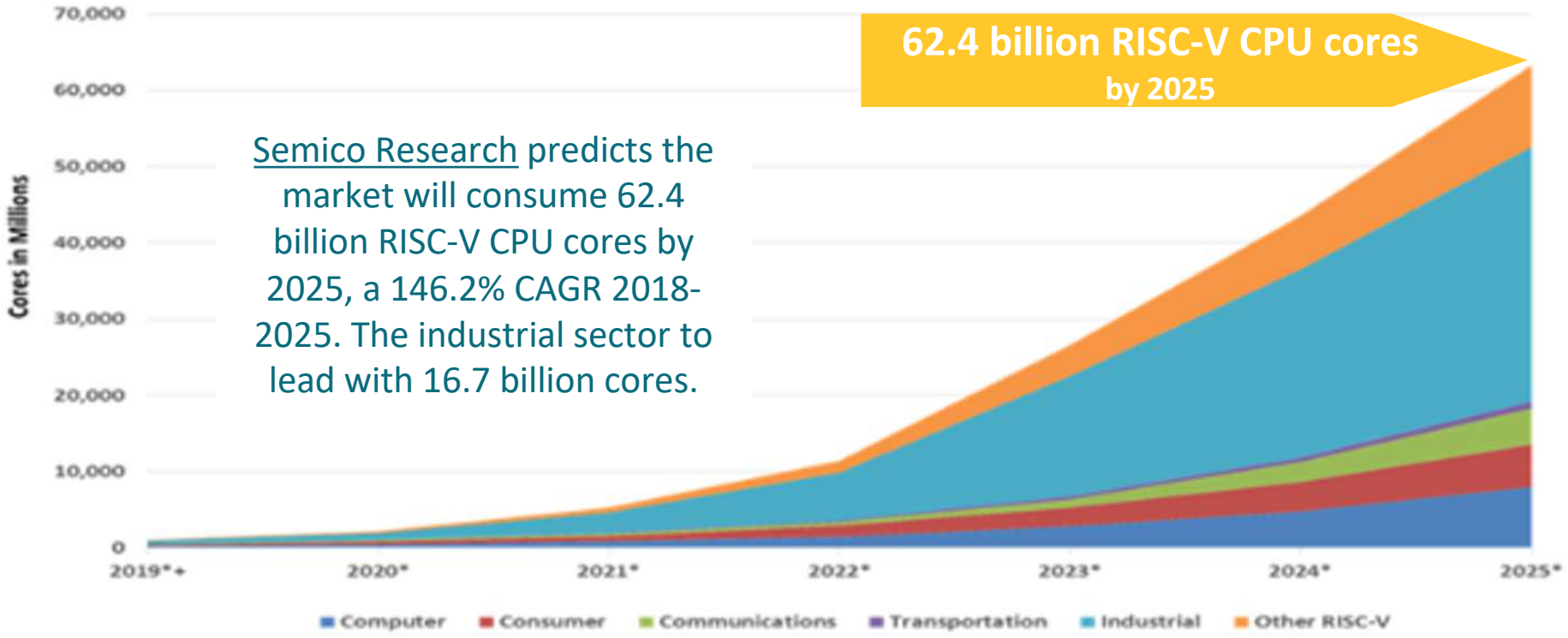
Source: Strategy Analytics

Rapid RISC-V growth over next five years led by industrial



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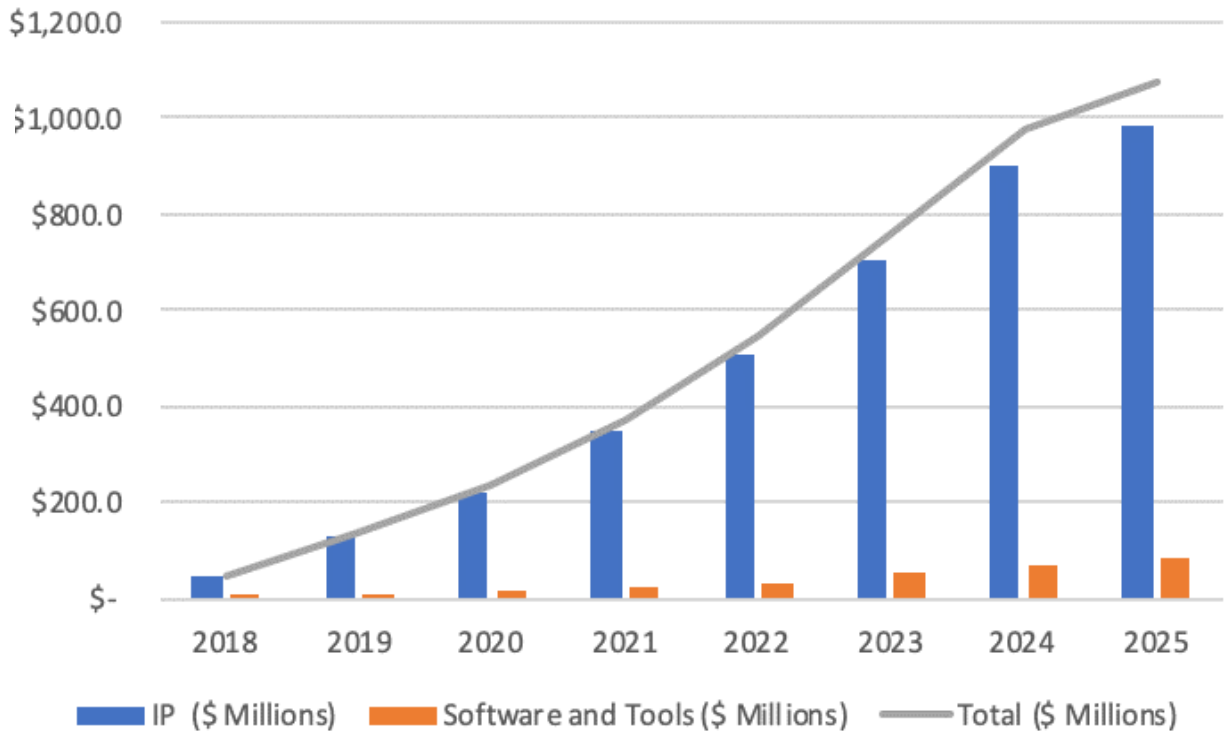
Source: Semico Research Corp

RISC-V IP, SW, and Tools build momentum

The total market for RISC-V IP and Software is expected to grow from to $1.07 billion by 2025 at a CAGR of 54.1%



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Source: Tractica

RISC-V adoption spans industries and workloads

Cloud and data center top providers like Amazon and Alibaba are designing their own chips.

Automotive is transforming from autonomous vehicles to infotainment to safety, the whole vehicle relies on innovative electronics.

Industrial IoT incorporating artificial intelligence in manufacturing and industrial processes.

Mobile and wireless continue rapid evolution with each generation of hardware and increased capability.

Consumer and IoT devices bring incredible innovation and volume with billions of connected devices in the next 5-10 years.

Memory was the largest semiconductor category by sales with $158 billion in 2018, and the fastest-growing.

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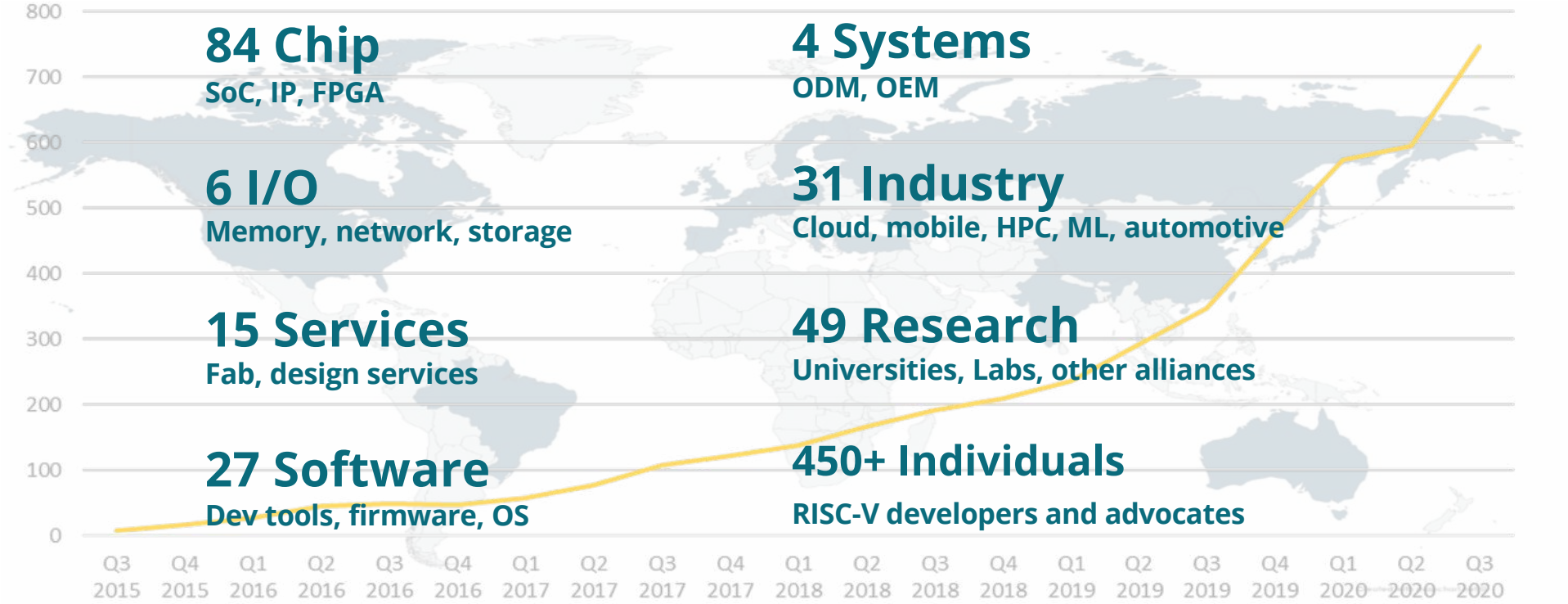
More than 700 RISC-V Members

across 50 Countries



84 Chip
SoC, IP, FPGA

6 I/O
Memory, network, storage

15 Services
Fab, design services

27 Software
Dev tools, firmware, OS

4 Systems
ODM, OEM

31 Industry
Cloud, mobile, HPC, ML, automotive

49 Research
Universities, Labs, other alliances

450+ Individuals
RISC-V developers and advocates

So far in 2020, RISC-V membership has grown by more than 50%

RISC-V Japan members

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Dedicated Community

Services Fab, design services

I/O Memory, network, storage

Software Dev tools, firmware, OS

Press and Analysts

Individual Advocates

Chip SoC, IP, FPGA

Universities and Research

Industry cloud, mobile, HPC, ML, automotive

Investors and Funding sources

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Japan industry momentum

NSITEXE, Kyoto Microcomputer and Codeplay Bringing Open Standards Programming to RISC-V Vector Processor

October 2020

Codeplay announced that HPC and AI RISC-V embedded software developers will leverage open standards from The Khronos Group, thanks to Japan's NEDO project in which NSITEXE and Kyoto are participating.

Renesas Selects Andes RISC-V 32-Bit CPU Cores for its First RISC-V Implementation of ASSPs

October 2020

Renesas selected the Andes Technology cores to embed into its new application-specific standard products to begin customer sampling in the second half of 2021.

RENESAS

ANDES TECHNOLOGY

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More momentum!

NSITEXE Selects Imperas RISC-V and Vectors Reference Model

September 2020

Imperas confirmed selection by NSITEXE for development and verification of the next generation automotive processor IP based on RISC-V with vector instruction extension.

NSI-TEXE

imperas

ArchiTek Select SiFive and DTS-Insight To Enable Next-Generation AI Solution Development

November 2019

SiFive announced a partnership with ArchiTek in collaboration with DTS-Insight to enable ArchiTek to design a new embedded, low-cost, high-performance SoC for AI.

ArchiTek

DTS INSIGHT
Our insight, your value

SiFive

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Japan University news

[RVSoC Offers a Lightweight Linux-Capable RISC-V Core in Just 5,000 Lines of Verilog]

February 2020

A Tokyo Institute of Technology team developed a portable and Linux-capable RISC-V SoC design in just 5,000 lines of Verilog and pledges to release it to all.

[Quick Boot of Trusted Execution Environment With Hardware Accelerators]

March 2020

Paper on a RISC-V system compatible with TEEs featuring security algorithm accelerators. Collaboration of UEC, AIST, and TRASIO.

[Bypassing Isolated Execution on RISC-V with Fault Injection]

September 2020

Paper by Mitsubishi and Tohoku University on RISC-V physical memory protection to prevent malicious software from accessing protected memory regions by providing a TEE.

[Out-of-Order Superscalar RSD RISC-V Design]

December 2019

Kyushu University, University of Tokyo, Nagoya University and National Institute of Informatics paper on a new out-of-order superscalar high performance RISC-V design for FPGAs.

RISC-V driving industry change

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In 2020...

... **1,800+ individuals in 43 RISC-V work groups** and committees, nearly double the RISC-V groups and 40% increase in participation

... **63% growth in 24 local meetup** groups

... We're in the news! We've **added 5,000+ followers on social media** and have participated in **80+ news articles** along with amplifying RISC-V community news 300+ times.

2020 Technical Progress

- Development process and deliverables are done with transparency.
- Technical Steering Committee brings industry best practice governance.
- Ratified two more specifications
- Set up a security response process
- Initiated compliance framework and test
- Launched the legal committee
- Welcomed Mark Himelstein, RISC-V CTO

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2020 Visibility Progress

- 38 events ranging from HPC and Embedded World in Europe to DAC and Open Source Summit in North America, to regional events in China and Taiwan.
- 378 blogs, announcements, and press briefings generating 9,244 mentions in the press.
- 220 RISC-V solutions online including cores, SoCs, software, tools and developer boards.
- Launched RISC-V Ambassador to support engineering leadership with 7 Ambassadors around the world.
- Welcomed Kim McMahon, RISC-V Director of Marketing.

RISC-V Learn

- Connecting **universities** with 30 contributed labs, lectures, and materials to invigorate RISC-V in university curriculum.
- RISC-V **Training Partner program** together with our first four partners around the world to offer professional RISC-V training in a multitude of formats.
- RISC-V **online learning** to offer broad as well as deep technical knowledge to accelerate the developer experience

Technical Deliverables

Guard against fragmentation
Build technical deliverables
Work groups

Compliance + Verification

Testing and compliance suites
Compliance tests

Visibility

Constant drumbeat through press, media, and original content
Industry and regional events
Dedicated RISC-V events

Learning + Talent

Multi-level online learning
Connecting universities with labs, tests, and curricula
RISC-V Training Partners

Advocacy

Technical advocate program
Local developer groups and events
RISC-V Ambassadors
Geo and industry alliances

Marketplace Exchange

Online marketplace of providers, products, and services
Technical developer forums

RISC-V delivers incredible member support

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Benefit of joining RISC-V

Accelerate technical traction and insight

Contribute technical priorities, approaches, and code

Gain strategic and technical advantage

Increase visibility, leadership, and market insight

Fill and increase engineering skills, retain and attract talent

Build innovation partner network and customer pipeline

Deepen, engage, and lead in local and industry developer network

Showcase RISC-V products, services, training, and resources

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RISC-V is a community of passionate, dedicated, and invested stakeholders

As individuals
As companies
As universities
As public institutions and non-profits
As nations

As one Global, connected movement

Build RISC-V into your company strategy, and your personal mission

www.riscv.org

@risc_v

@Calista_Redmond

risc-v-international
calistaredmond

Membership options

Premier Member Benefits

- Community level benefits plus…
- Board seat and Technical Steering Committee seat included for $250k level
- Technical Steering Committee seat included for $100k level
- Summit speaker session
- Solution provider listing
- 2 blogs per month
- 2 social media spotlights per month
- Spotlight member profile
- Inclusion in event promotions

Strategic Member Benefits

- Community level benefits plus…
- Use of RISC-V Trademark for commercialization
- 3 Board reps elected for tier, includes Premier members that do not otherwise have a board seat.
- Eligible to lead workgroup and/or committee
- Solution provider listing
- 1 blog per month
- 1 social media spotlight per month

Community Member Benefits

- Accelerated development, reduced risk through open source, ratified ISA.
- Eligible to participate in workgroups, influence strategy and adoption
- 6 support programs in Technical Deliverables, Compliance, Visibility, Learning, Advocacy, and Marketplace
- 1 voting Academic Board rep, 1 non-voting Community Board rep
- Member logo / name listing in website
- Event registration discount

Premier Requirements

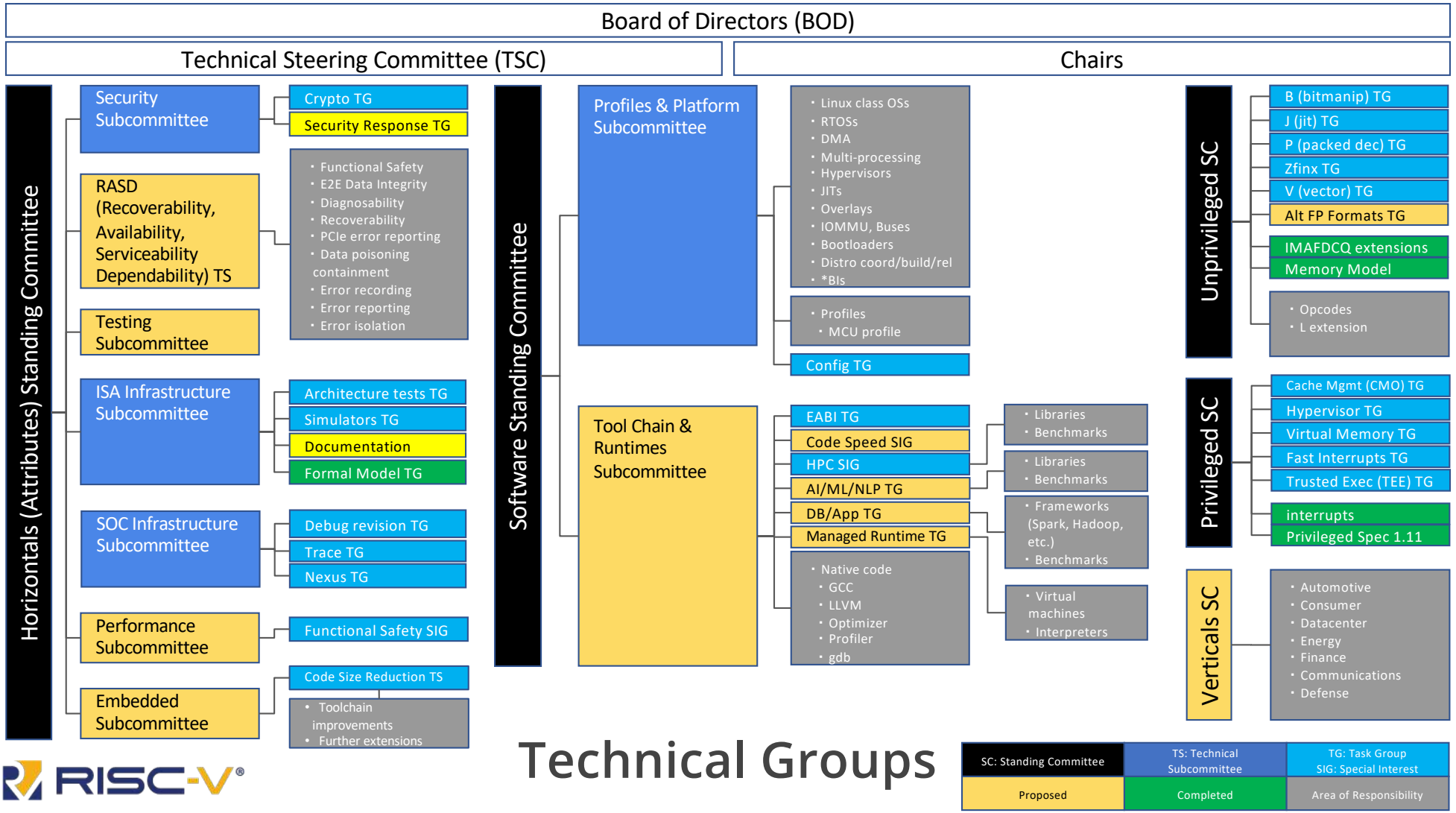
- Membership open to any type of legal entity, not open to individual members
- $250k Annual membership fee that includes Board seat and TSC seat
- $100k Annual membership fee that includes TSC seat

Strategic Member Requirements

- Membership open to any type of legal entity, not open to individual members
- Annual membership fee based on employee size
  - 5,000+ employees $35k
  - 500-5,000 employees $15k
  - <500 employees $5k

Community Requirements

- Membership open to academic institutions, non-profits, and individuals not representing a legal entity
- No annual membership fee


Board of Directors (BOD)
Technical Steering Committee (TSC)
Chairs
Horizontals (Attributes) Standing Committee
Security Subcommittee
Crypto TG
Security Response TG
RASD (Recoverability, Availability, Serviceability Dependability) TS
Functional Safety
E2E Data Integrity
Diagnosability
Recoverability
PCIe error reporting
Data poisoning containment
Error recording
Error reporting
Error isolation
Testing Subcommittee
ISA Infrastructure Subcommittee
Architecture tests TG
Simulators TG
Documentation
Formal Model TG
SOC Infrastructure Subcommittee
Debug revision TG
Trace TG
Nexus TG
Performance Subcommittee
Functional Safety SIG
Embedded Subcommittee
Code Size Reduction TS
Toolchain improvements
Further extensions
Software Standing Committee
Profiles & Platform Subcommittee
Linux class OSs
RTOSs
DMA
Multi-processing
Hypervisors
JITs
Overlays
IOMMU, Buses
Bootloaders
Distro coord/build/rel
*BIs
Profiles
MCU profile
Config TG
Tool Chain & Runtimes Subcommittee
EABI TG
Code Speed SIG
HPC SIG
AI/ML/NLP TG
DB/App TG
Managed Runtime TG
Native code
GCC
LLVM
Optimizer
Profiler
gdb
Libraries
Benchmarks
Libraries
Benchmarks
Frameworks (Spark, Hadoop, etc.)
Benchmarks
Virtual machines
Interpreters
Unprivileged SC
B (bitmanip) TG
J (jit) TG
P (packed dec) TG
Zfinx TG
V (vector) TG
Alt FP Formats TG
IMAFDCQ extensions
Memory Model
Opcodes
L extension
Privileged SC
Cache Mgmt (CMO) TG
Hypervisor TG
Virtual Memory TG
Fast Interrupts TG
Trusted Exec (TEE) TG
interrupts
Privileged Spec 1.11
Verticals SC
Automotive
Consumer
Datacenter
Energy
Finance
Communications
Defense
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Technical Groups
SC: Standing Committee
TS: Technical Subcommittee
TG: Task Group
SIG: Special Interest
Proposed
Completed
Area of Responsibility