The Open Era of Computing

Calista Redmond
CEO, RISC-V International

November 2021

RISC-V

Thank you!

Open source and collaboration are strategic to software and hardware across industries.

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Photo by THIS IS ZUN from Pexels

RISC-V is the free and open Instruction Set Architecture

- Open collaboration
- Design freedom
- Strategic future

Disruptive **Technology**

Barriers	**Legacy ISA**	**RISC-V ISA**
Complexity	1500+ base instructions Incremental ISA	47 base instructions Modular ISA
Design freedom	$$$ – Limited	Free – Unlimited
License and Royalty fees	$$$	Free
Design ecosystem	Moderate	Growing rapidly. Numerous extensions and cores. More design companies on RISC-V than any other architecture
Software ecosystem	Extensive	Growing rapidly. Easy to compile for RISC-V

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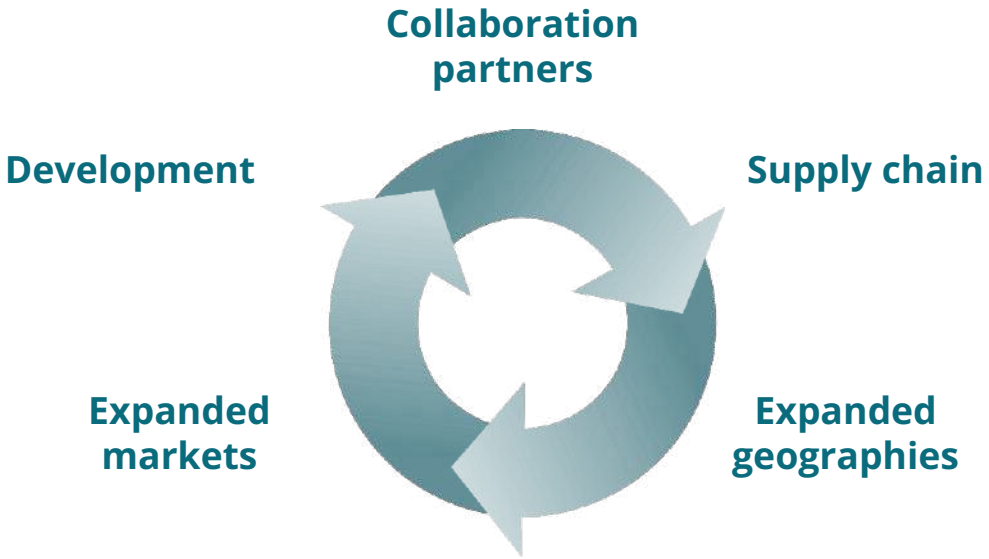
Unconstrained **Opportunity**

Barriers removed

- Design risk
- Cost of entry
- Partner limitations
- Supply chain

RISC-V Business Model



Beyond removing barriers, RISC-V fuels our community to seize growing opportunities

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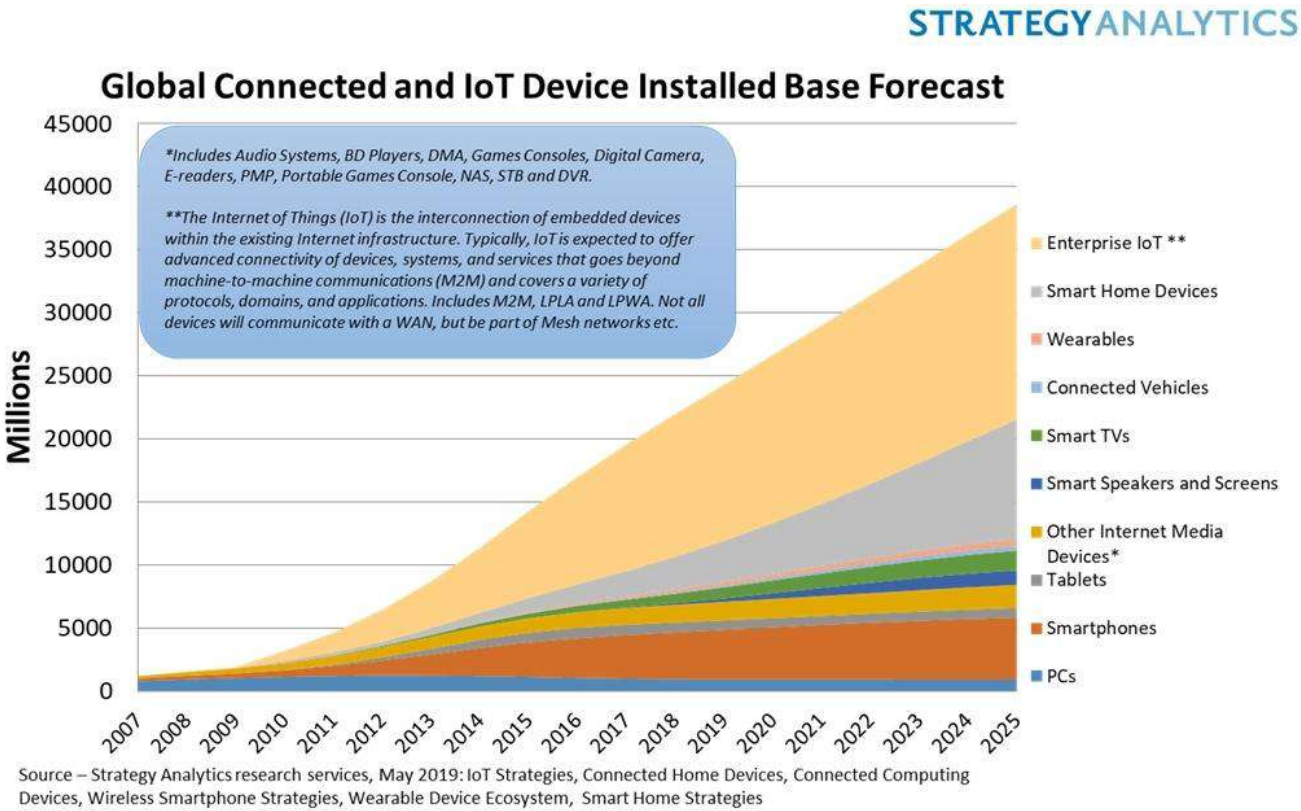
50 billion connected and IoT devices by 2030



Source: Strategy Analytics

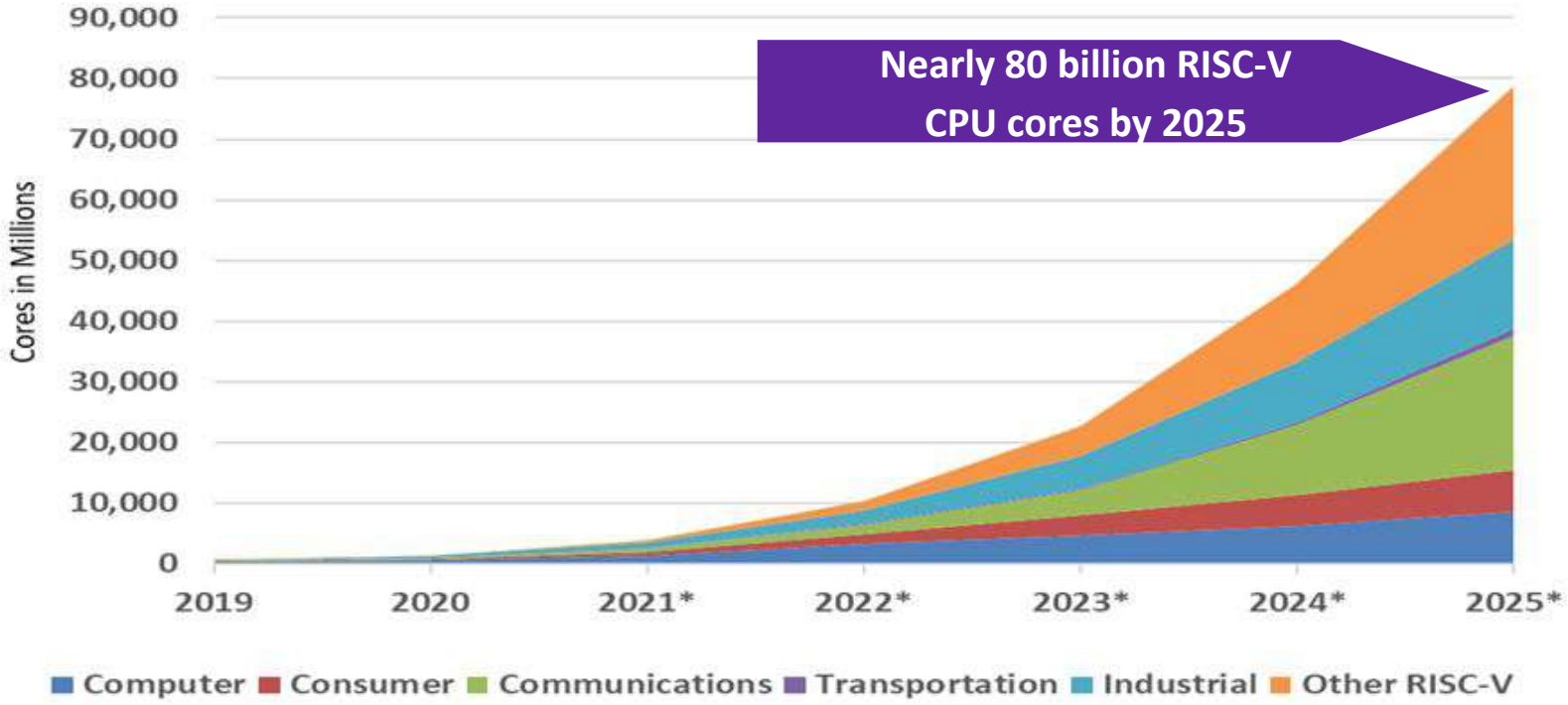
By 2025, 40% of application-specific integrated circuits (ASICs) will be designed by OEMs.

Custom ASICs Based on RISC-V Will Enable Cost-Effective IoT Product Differentiation

Gartner, June 2020

Source: Gartner

The RISC-V CPU core market will grow at 114.9% CAGR, capturing over 14% of all CPU cores by 2025



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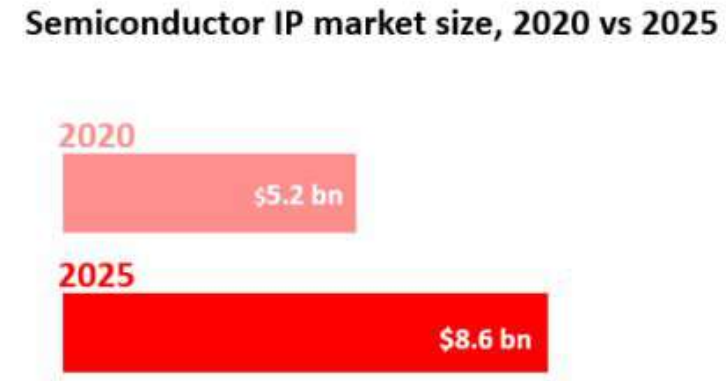
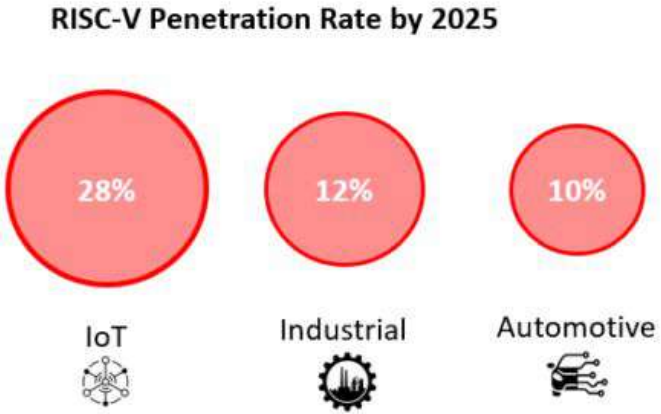
Source: Semico Research Corp, March 2021





"The rise of RISC-V cannot be ignored… RISC-V will shake up the $8.6-Billion semiconductor IP market."

-- William Li, Counterpoint Research

Source: Counterpoint Research, September 2021

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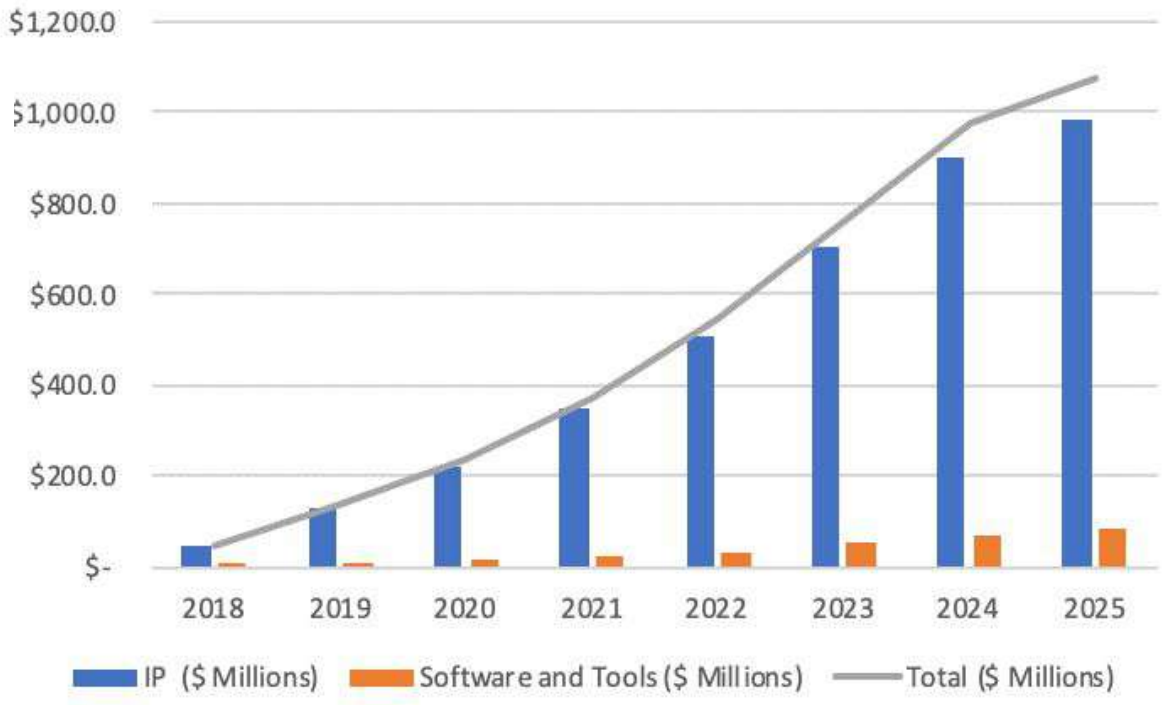
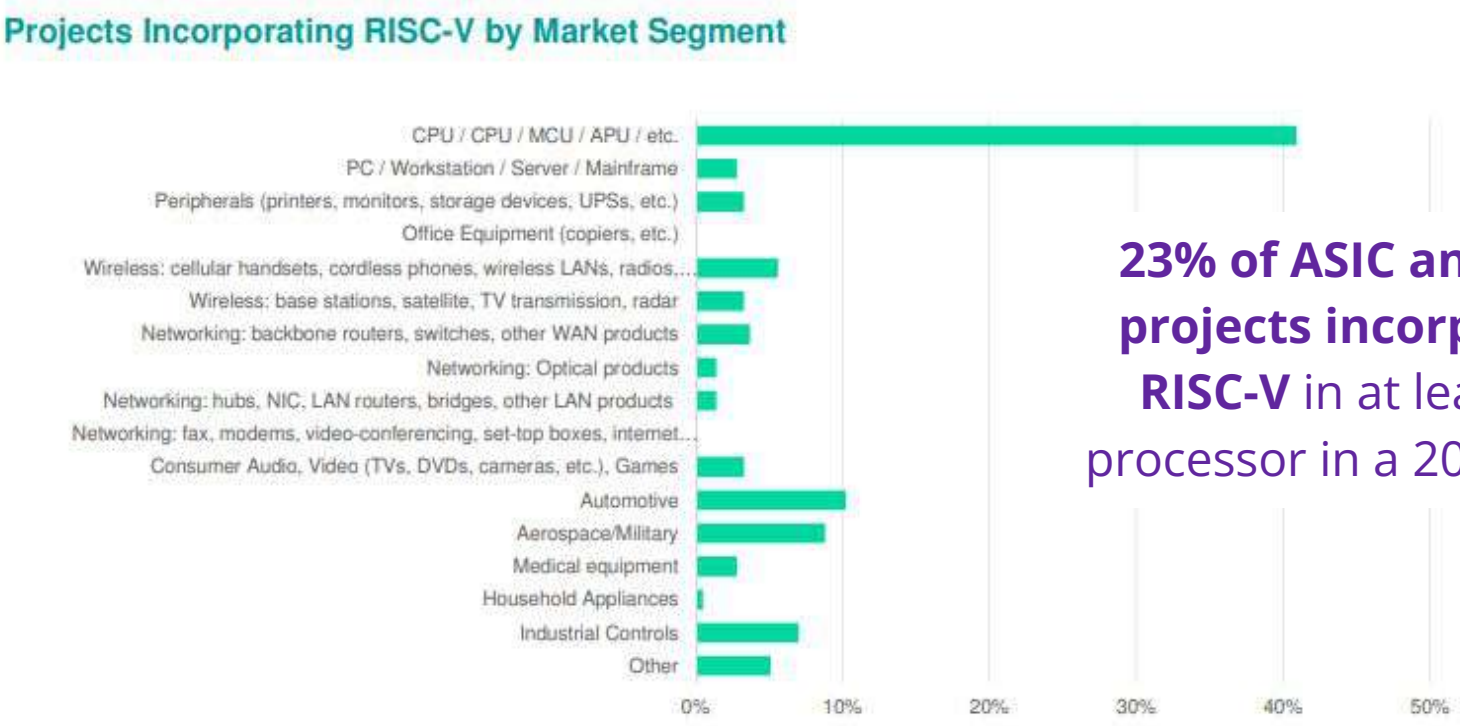
Growth in RISC-V IP, SW, and Tools is already happening

The total market for RISC-V IP and Software is expected to grow to $1.07 billion by 2025 at a CAGR of 54.1%



Source: Tractica, December 2019

Today, nearly a quarter of designs incorporate RISC-V



23% of ASIC and FPGA projects incorporated RISC-V in at least one processor in a 2020 study.

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Source: Tech Design Forum, November 2020

- **Intel** Nios processor based on RISC-V, designed for performance.
- **Alibaba** RISC-V Xuantie processor line including four open sourced processors for cloud and edge servers
- **Imagination** RISC-V CPU family, for both the discrete CPU and heterogeneous computing markets
- **Seagate** hard disk drive controller with high-performance RISC-V CPU.

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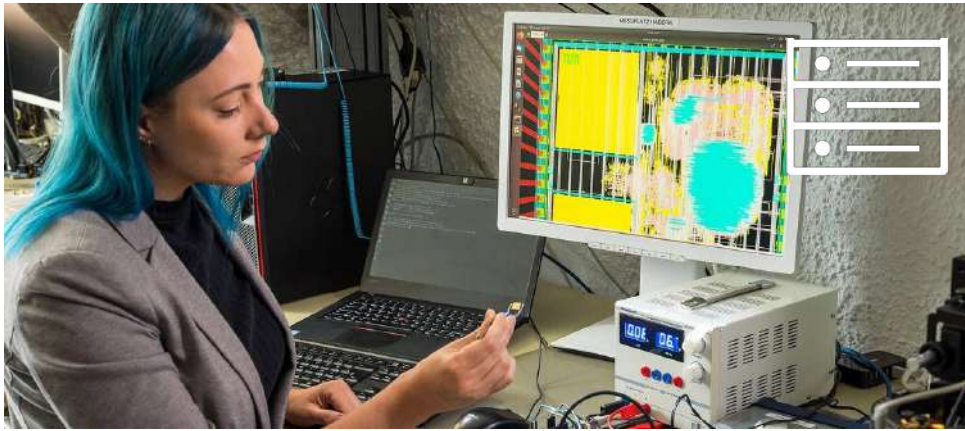
Telecom & Communications

- **Andes** 64-bit RISC-V processor has been adopted by SK Telecom for the development of AI products.
- **Alibaba** PLCT Lab has ported Android 10 onto its in-house 64-bit RISC-V core emulated in QEMU
- **Google** Pixel 6 Titan M2 in-house designed RISC-V processor, with extra speed and memory, and even more resilient to advanced attacks.

High Performance Computing

- **European Processor Initiative** RISC-V accelerator with first chip Sep 2021
- **Technical University of Munich** (TUM) quantum cryptography chip for quantum computing security demands
- **Tactical Computing Labs** HPC-centric software test suite for GCC and LLVM
- **Cortus** is developing a high-performance RISC-V Out-of-Order processor core for the European eProcessor project.
- **De-RISC** market-ready HW-SW platform for a multi-core RISC-V system-on-chip for safety critical aerospace applications



Johanna Baehr of TUM heads a team that has hidden four hardware Trojans on this chip - malicious functions that are integrated directly into the circuits.

Image: Astrid Eckert / TUM

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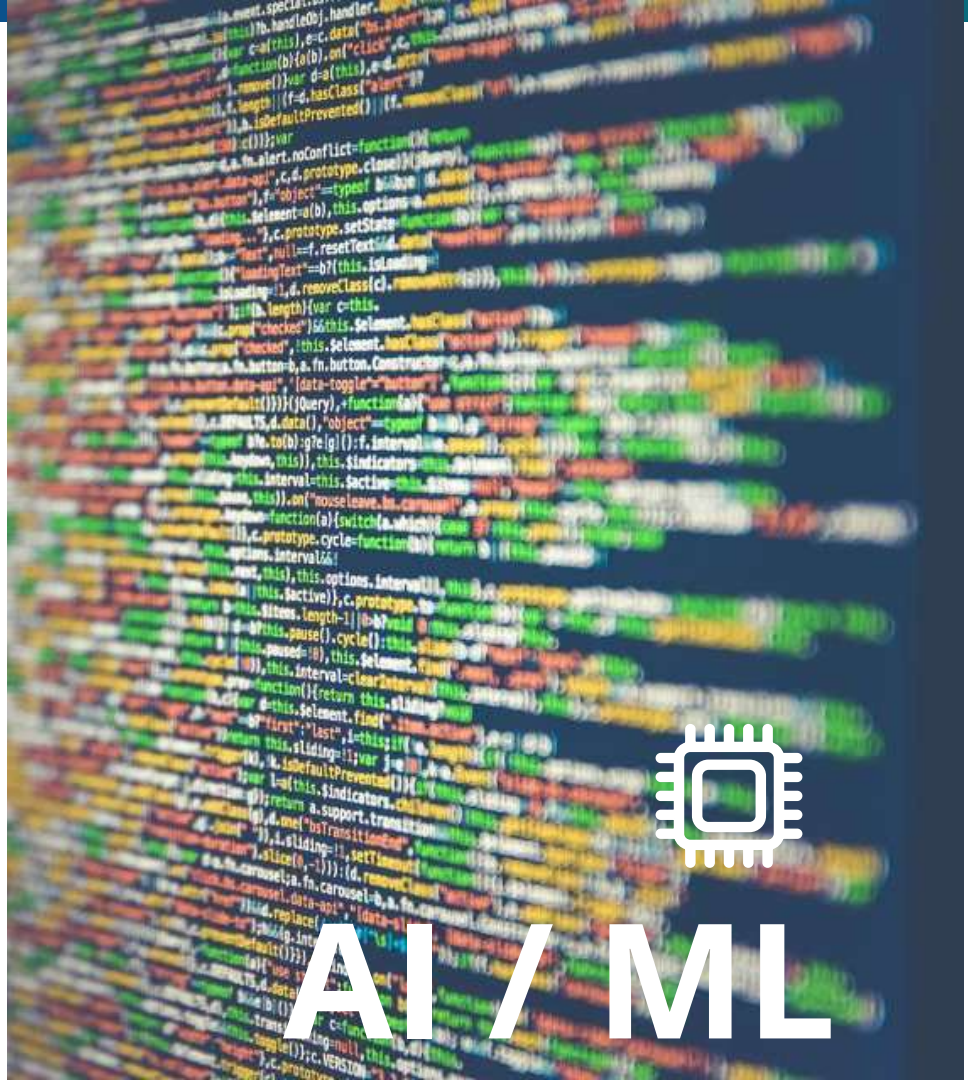
Edge Computing

A distributed, open architecture decentralizes processing power, reduces latency, and supports IoT performance in low bandwidth environments at low power.

- **Seeed Studio**'s new development, the Sipeed MAIX, a RISC-V 64 AI board for Edge Computing makes it possible to embed AI to any IoT device.
- **Micro Magic** announced an incredibly fast 64-bit RISC-V core achieving 5GHz and 13,000 CoreMarks at 1.1V.
- **Western Digital** SweRV Core enables spectrum of compute at the edge

Artificial intelligence spans many areas from Industrial IoT to financial

- **Esperanto** Emerges From Stealth With 1,000-Core RISC-V AI Accelerator.
- **StarFive** released the world's first RISC-V AI visual processing platform
- **Andes** released superscalar multicore and L2 cache controller processors.
- **NVIDIA CUDA** support on the Vortex RISC-V GPGPU enables scaling from 1-core to 32-core GPU based on RV32IMF ISA with OpenCL 1.2 graphics API support.



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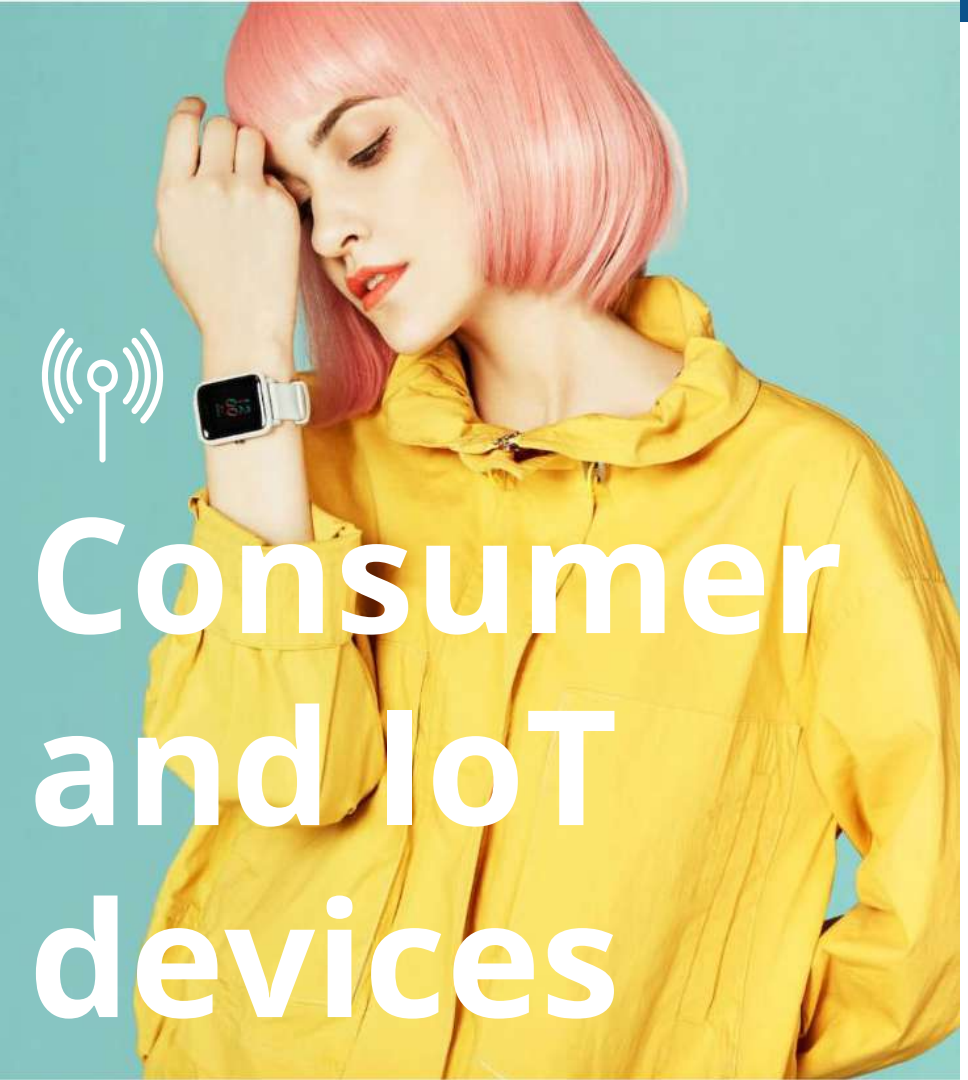

Consumer and IoT devices

- **Huawei** Hi3861 RISC-V board for Harmony OS developers for the IoT market
- **Zepp Health** / Huami wearable manufacturer OS supporting RISC-V Reference Models for RISC-V P extension
- **GreenWaves** ultra-low power GAP9 hearables platform for scene-aware and neural network-based noise reduction.
- **Microchip** released the first SoC FPGA development kit based on the RISC-V ISA.
- **RIOS Lab** announced PicoRio, an affordable RISC-V open source small-board computer.
- **SiFive** world's fastest development board for RISC-V Personal Computers.

Automotive

- **Imagination Technologies** GPU can be linked together by a RISC-V core for ASIL-B level designs with ISO26262 safety critical certification.
- **IAR Systems** extended the functional safety version of its Embedded Workbench software tool chain to the RISC-V core of Nsitexe, subsidiary of automotive leader Denso.
- **Renesas and SiFive** jointly develop next generation RISC-V SoCs for automotive
- **Renesas and NSI-TEXE** announce automotive SoC with RISC-V-based parallel co-processor
- **Europe's GaNext project** to simplify designing power converters with GaN power semiconductors while improving efficiency and compactness for systems such as electric vehicle chargers.

“The scalable range of performance, selectable safety features, and customization options provided by the Andes RISC-V core IP enables Renesas to provide innovative solutions for future application-specific standard products,”

--Sailesh Chittipeddi, EVP and GM, Renesas IoT and Infrastructure

Renesas RISC-V ASSP products use CPU cores from Andes for design differentiation from low-end products

- Renesas ASSPs equipped with Renesas firmware.
- Renesas ASSPs are dedicated devices, user can set parameters of application programs.
- Renesas plans a user interface to make it easier for users to optimize solutions to their use case.

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Partnership for Jointly Developing Next-Gen Automotive RISC-V Solutions

Renesas and SiFive partner for next generation high-end in-vehicle RISC-V SoCs and microcontrollers

- RISC-V core and AI accelerators provide Renesas performance and scalability for in-vehicle applications.
- SiFive's RISC-V cores offer trace and debugging capabilities compatible with prevailing industry tools.
- Security solution is integrated to simplify integration and migration between different models.
- SiFive RISC-V cores are silicon proven (verified to work within actual chips) and can be produced by a major Si foundry with advanced fabrication technologies.

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ArchiTek

- Combines the advantages of a CPU, GPU, and a dedicated LSI.
- Architek architecture processes AI workloads with significantly lower power and higher efficiency than general-purpose CPUs and GPUs.
- Targets AI processing for IoT edge. The chip made by TSMC 12nm process is 4.5mm by 4.5mm, and its power performance enables fan-less designs.

AI processor AiOnIc by ArchiTeK with SiFive's E3 series RISC-V processor IP in addition to the ArchiTek Intelligence® Pixel Engine (aIPE).

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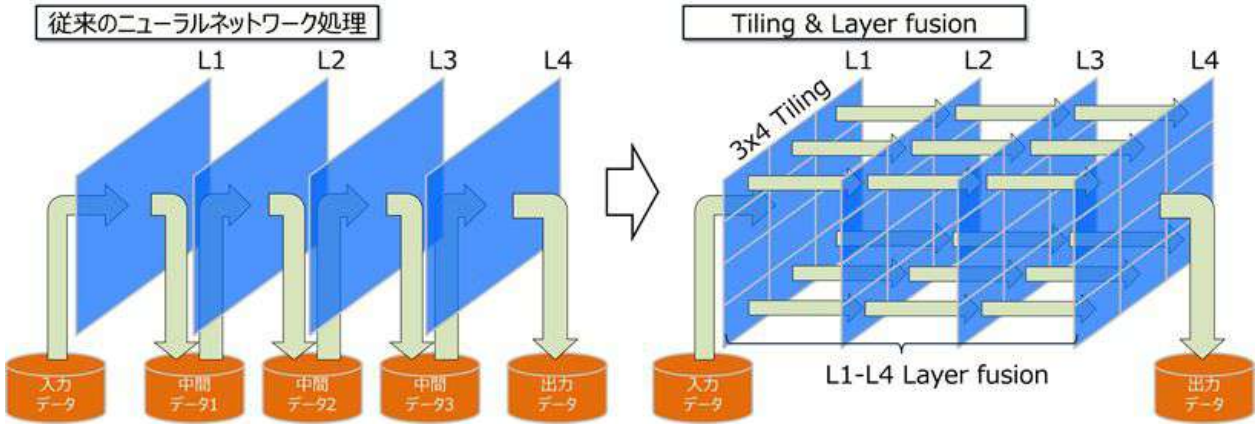
Acceleration, efficiency, reduced power.

NSITEXE AI accelerator ML041

- The AI accelerator ML041 executes Neural networks (e.g. VGG16, MobileNet, and ResNet) at power efficiency of 12TOPS / W using 7nm geometry.

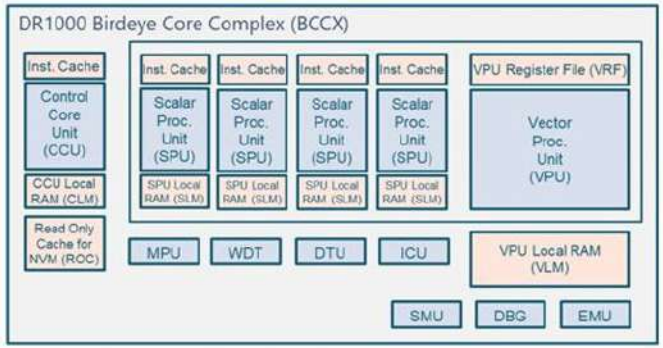
- ML041 divides input data (Tiling) and concatenates the input and output of multiple layer processing to process the intermediate data. This reduces the data transfers with the external memory improving the power performance.

- ML041 also provides a built-in diagnostic circuit to detect random hardware failures enabling AI applications in safety-critical systems.



NSITEXE DR 1000 C, a RISC-V vector processor

- NSITEXE licensed Renesas DR 1000 C, a RISC-V-based vector accelerator for arithmetic processing (e.g. model predictive control, real-time modeling, sensor data processing) to meet automotive safety-critical requirements.



MPU: Memory Protection Unit
WDT: Watch Dog Timer
DTU: Data Transfer Unit
ICU: Interrupt Controller/Request

SMU: System Management Unit
DBG: Debug Unit
EMU: Error Management Unit

SGS TÜV SAAR ASIL D READY Functional Safety www.sgs-tuev-saar.com

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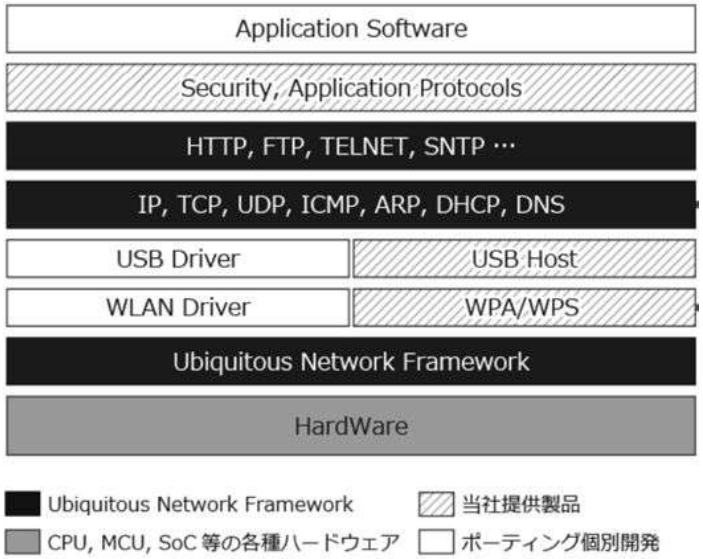
Ubiquitous AI Corporation's RISC-V Network Framework

Ubiquitous AI Corporation is creating RISC-V Middleware for implementing communication functions based on the TCP / IP stack.



Ubiquitous AI Corporation

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Dedicated Community

Services Fab, design services

Chip SoC, IP, FPGA

I/O Memory, network, storage

Universities and Research

Software Dev tools, firmware, OS

Industry cloud, mobile, HPC, ML, automotive

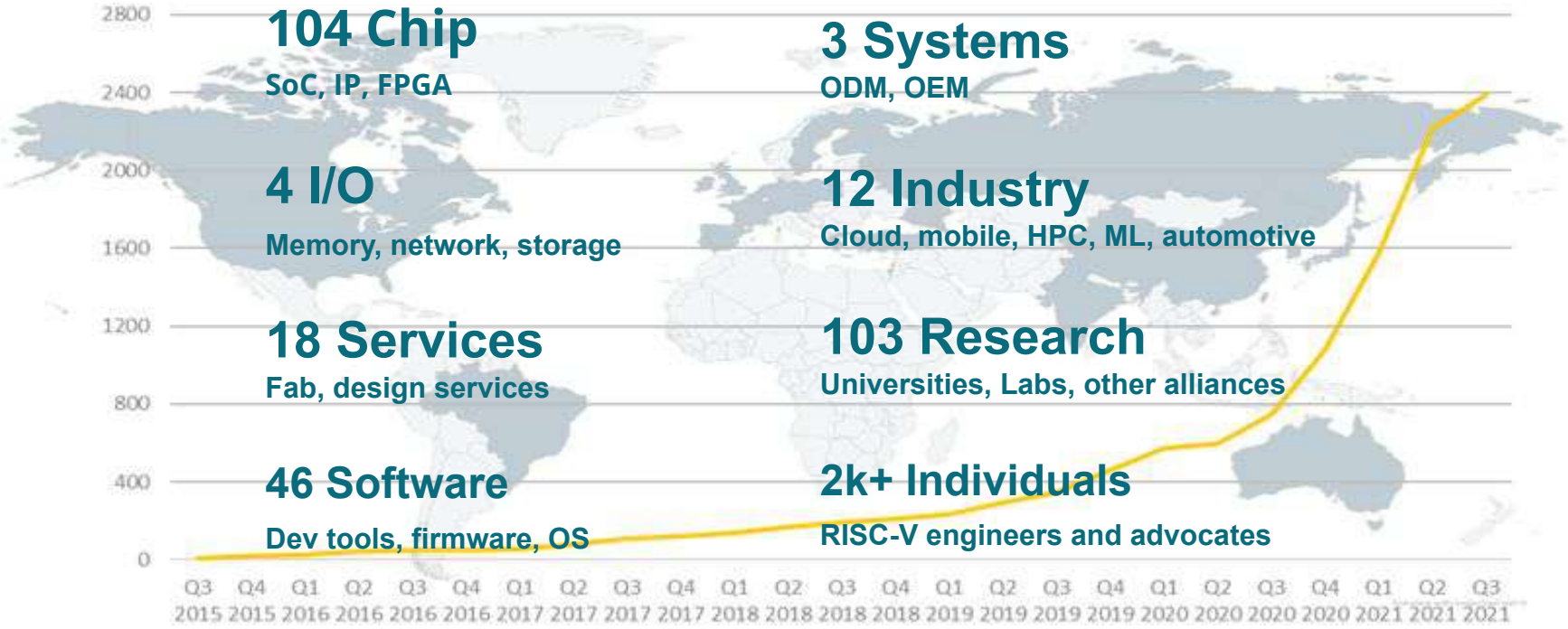
Press and Analysts

Investors and Funding sources

Individual Advocates

More than 2,400 RISC-V Members

across 70 Countries



104 Chip
SoC, IP, FPGA

3 Systems
ODM, OEM

4 I/O
Memory, network, storage

12 Industry
Cloud, mobile, HPC, ML, automotive

18 Services
Fab, design services

103 Research
Universities, Labs, other alliances

46 Software
Dev tools, firmware, OS

2k+ Individuals
RISC-V engineers and advocates

RISC-V membership grew 133% in 2020.
In 2021, RISC-V membership has already doubled.

RISC-V is the foundation of the Open era of computing

- **4k+ individuals in 60+ RISC-V work groups** and committees
- **330+ RISC-V solutions** online including cores, SoCs, software, tools, and developer boards
- **29 local RISC-V community** groups, with more than **5,400 engineers**
- We're in the news! We have **40k+ followers on social media** and across the last year, we have participated in **135+ news articles** along with amplifying RISC-V community news 450+ times.

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Technical Deliverables

Technical **governance**
Build **technical deliverables**
Work groups

Compatibility & Verification

Testing and compatibility **resources**
Compatibility **tests**

Visibility

Amplify member news, content, and success with press and analysts
Original content programs
RISC-V, industry, and regional **events**

Learning & Talent

Multi-level **online learning**
Connecting **universities** with labs, tests, and curricula
RISC-V **Training Partners**
Jobs and internships

Advocacy + Alliances

RISC-V **Ambassadors**
Geo and industry **alliances**
Local developer groups and events

Marketplace Exchange

Online marketplace of providers, products, services, and learn
Technical **developer forums**

RISC-V delivers incredible member support

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RISC-V Innovation Roadmap

2010 – 2016

Test Chips
Software tests
Linux port

ISA Definition
RISC-V Foundation

2017

Proof of Concept SoCs
Minion processors for power management, communications
Bare metal software

RV32

2018

IoT SoCs
Microcontrollers
RTOS, Firmware
Development tools
Technical Steering Committee, HPC SIG, GlobalPlatform partnership

RV32I and RV64I Base instructions: Integer, floating point, multiply and divide, atomic, and compact instructions

Priv modes, Interrupts, exceptions, memory model, protection, and virtual memory

2019

2020

AI SoCs, Application processors, Linux Drivers, AI Compilers
Dev Board program
Development Partners
RISC-V Labs, Security response process, AI SIG, Graphics SIG, Android SIG, Communications SIG

Arch compatibility framework,
Processor trace

2021

2022

Zfinx
ZiHintPause
BitManip
Vector
RISC-V Profiles & Platforms
Crypto Scalar
Virtual Memory
Hypervisor & Advanced interrupt architecture
Cache mgt ops
Code size reduction*
Trusted Execution Environment*
P (Packed SIMD)*

2023

2024

2025

RV32E and RV64E
64 bit and 128 bit addresses*
Vector Atomic and quad-widening*
Quad floating point in integer registers*
Crypto Vector*
Trusted Execution phase 2*
Jit pointer masking & I/D synch*
BitManip phase 2*
Cache management phase 2*
... and more

Industry Adoption

Proliferation of RISC-V CPUs across performance and application spectrum
RISC-V dominant in universities
Strategic and growing adoption in HPC, automotive, transportation, cloud, industrial, communications, IoT, enterprise, consumer, and other applications

Technical Deliverables

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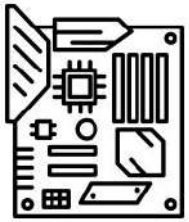
** On track, subject to change*

RISC-V Technical Programs



RISC-V Developer Boards
Available to spur innovation, provide hands-on education, and engage early adopters to test and develop.

RISC-V Development Partner
Recognizes the investment and dedication of organizations making significant technical contributions to RISC-V.

RISC-V Lab
Institutions that host a lab with RISC-V hardware for CI/testing and general availability sandboxing.

RISC-V Compatible
Architectural Tests created to help ensure that software written will run on implementations that comply with that profile. Branding available for compatibility.

RISC-V Platform
A common, reusable runtime environment that operating systems and applications can target to improve portability and reuse. Provides interoperability assurance.

RISC-V Profiles
Refers to a base ISA and one or more extensions that are specified as a group so that applications can be compiled once, run on different implementations, and get the same results.

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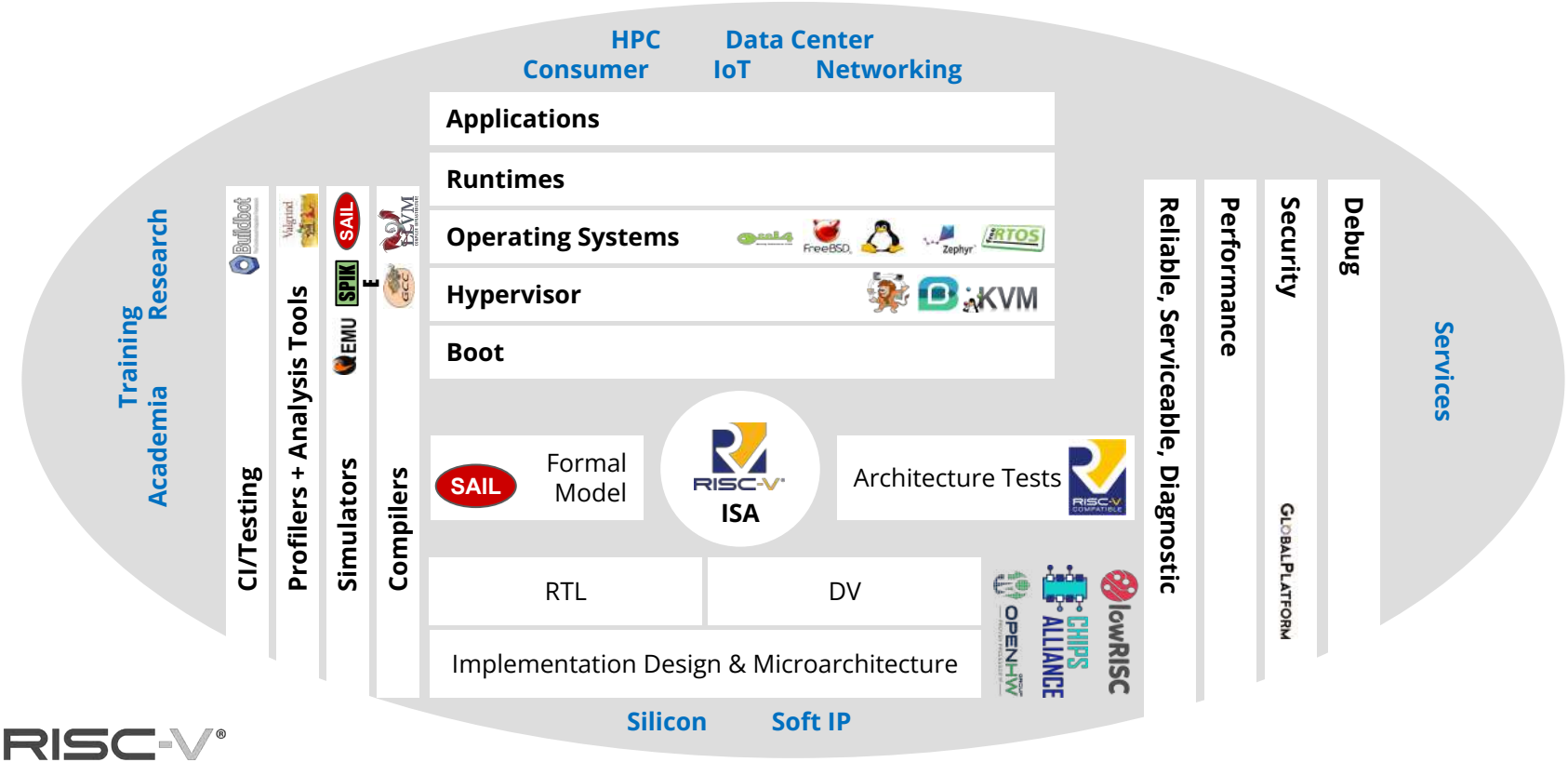
RISC-V Ecosystem



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Benefits of engaging in RISC-V

- ✔ **Accelerate technical traction** and insight
- ✔ **Contribute** technical priorities, approaches, and code
- ✔ Gain strategic and **technical advantage**
- ✔ **Increase visibility**, leadership, and market insight
- ✔ Fill and increase **engineering skills**, retain and attract talent
- ✔ Build **innovation partner** network and customer pipeline
- ✔ **Deepen, engage, and lead** in local and industry developer network
- ✔ **Showcase RISC-V products**, services, training, and resources

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Membership Options

RISC-V Membership details may be found online here

Premier Member Benefits

- Board seat and Technical Steering Committee seat included for $250k level
- Technical Steering Committee seat included for $100k level
- Eligible to lead workgroup and/or committee

- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Premier members
- Solution / Product listing highlighted on RISC-V Exchange, noted with member level
- 4 case studies a year
- 2 blogs per month
- 2 social media spotlights per month
- Spotlight member profile
- Event sponsorship discount

Strategic Member Benefits

- 3 Board reps elected for the Strategic tier, including Premier members that do not otherwise have a board seat
- Eligible to lead workgroup and/or committee

- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Strategic members
- Solution / Product listing highlighted on the RISC-V Exchange, noted with member level
- 1 case study a year
- 1 blog per month
- 1 social media spotlight per month
- Event sponsorship discount

Community Member Benefits

- Two Board representatives
- 1 Community Board representative, elected
- 1 Individual Board representative, elected

- Member logo / name listing on RISC-V website, by member level
- 1 case study a year
- 1 blog per quarter
- 1 social media spotlight per quarter
- Event sponsorship discount

Premier Requirements

- Membership open to any type of legal entity
- $250k Annual membership fee that includes Board seat and TSC seat
- $100k Annual membership fee that includes TSC seat

Strategic Member Requirements

- Membership open to any type of legal entity
- Annual membership fee based on employee size
  - 5,000+ employees: $35k
  - 500-5,000 employees: $15k
  - <500 employees: $5k
  - <10 employees & company <2 yrs old: $2k

Community Requirements

- Membership open to
  - academic institutions,
  - non-profits,
  - individuals not representing a legal entity
- No annual membership fee

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"**The future depends on open source tech**, … RISC-V is gaining traction in the hardware manufacturing space throughout the world, because it lowers barriers to entry and increases chip development speed."

-- Wired

"Though the architecture was created a decade ago by university professors, **RISC-V has been building its ecosystem for years and has started to hit its stride** with big licensees like Western Digital, SiFive, and even NVIDIA itself."

-- VentureBeat

"If it succeeds, RISC-V could lower the cost of developing a new chip and help **companies of all sizes to build exactly the processors they need**."

-- Engadget

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Thank You

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