Accelerate Edge Computing with RISC-V in Efinix FPGA

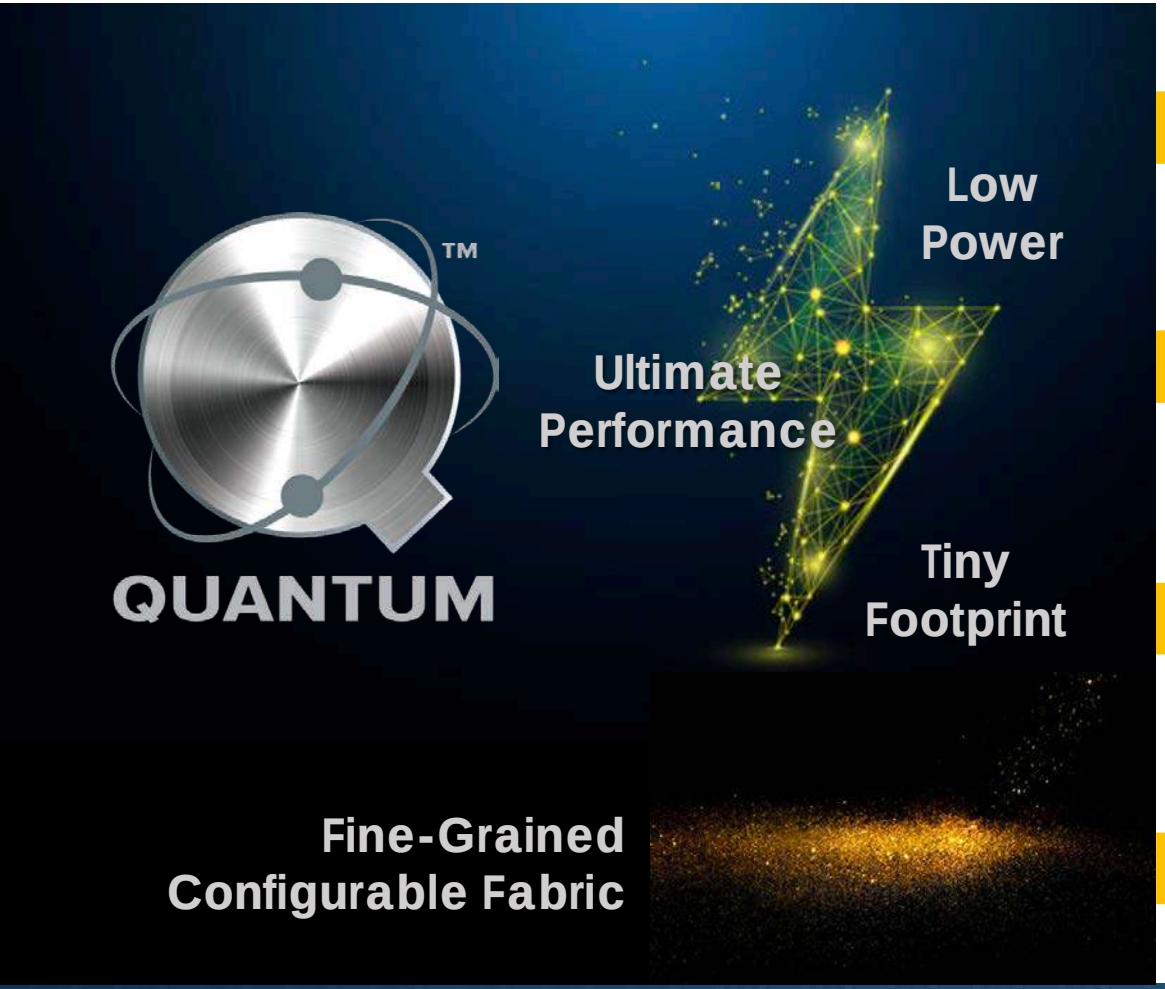
RISC-V Days Tokyo 2021 Spring (April 22nd-23rd)

Ikuo Nakanishi, Efinix Japan

What is Efinix (Company Overview)

- US based FPGA and eFPGA company, founded in October 2012
- Powered by disruptive Quantum compute technology
- Global company with offices worldwide
  - United States, China, Malaysia, Canada, Japan, Korea, Germany, and Taiwan
- 70+ employees
- Endorsed and invested by Xilinx, Samsung, Alibaba, HKX, AIM, and MAVCAP

Quantum Compute Technology



AI and Neural Networks

DSP and BRAM Tailored for **Embedded AI**

Data and Computing

Parallel Data Computing with Reconfigurable XLR

FPGA Custom Logic

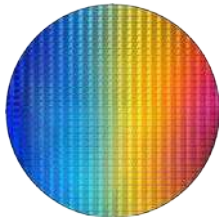
4X+ Power-Performance-Area Advantage vs FPGA Peers

RISC-V Acceleration

Software and Algorithmic Programming with **RISC-V**

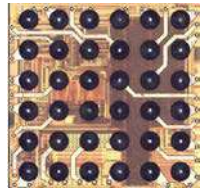
Titanium

- Ultimate Performance in a Tiny Footprint with 70% Less Power
- Secure, Reconfigurable Compute for Mainstream Applications
- One Scalable Platform to One Million LEs
- 400MHz Software Defined RISC-V
- Quantum Accelerators



TSMC 16 nm Process

Quantum Compute Accelerated



Innovative Package Options

Feature		Ti35	Ti60	Ti90	Ti120	Ti170	Ti240	Ti375	Ti550	Ti750	Ti1000
Logic Elements (LE)		36,176	62,016	89,812	119,750	169,646	236,888	370,137	533,174	727,056	969,408
10K Memory Blocks (Mb)		1.53	2.62	7.34	9.80	12.62	19.37	27.53	39.65	54.07	72.09
DSP Blocks		93	160	359	478	616	946	1,344	1,936	2,640	3,520
High-Speed I/O (HSIO)		146	146	204	204	204	172	172	268	268	268
GPIO (3.3 V)		34	34	80	80	80	80	80	80	80	80
PLLs		4	4	10	10	10	10	10	10	10	10
DDR4/LPDDR4/DDR3/LPDDR3		-	-	x32	x32	x32	x72	x72	2 x72	2 x72	2 x72
MIPI D-PHY 2.5 Gbps (Rx, TX)		-	-	(2, 2)	(2, 2)	(2, 2)	(3, 3)	(3, 3)	(3, 3)	(3, 3)	(3, 3)
16 Gbps Serdes		-	-	x8	x8	x8	x12	x12	x16	x16	x16
25.8 Gbps Serdes		-	-	-	-	-	-		x8	x8	x8
PCI Express Gen 4 (16G)		-	-	x4	x4	x4	2 x4	2 x4	2 x8	2 x8	2 x8
Packages											
WLCSP 64	0.4 mm/3.4x3.5 mm		✓								
FBGA 100	0.5 mm/5.5x5.5 mm	✓	✓								
FBGA 225	0.5mm/8x8 mm			✓	✓	✓					
FBGA 225	0.65 mm/10x10 mm	✓	✓	✓	✓	✓					
FBGA 324	0.65 mm/12x12 mm			✓	✓	✓					
FBGA 400	0.8mm/16x16 mm			✓	✓	✓					
FBGA 484	0.65 mm/15x15 mm			✓	✓	✓	✓	✓			
FBGA 625	0.65 mm/17x17 mm						✓	✓	✓	✓	
FBGA 784	0.8 mm/23x23 mm						✓	✓	✓	✓	✓
FBGA 1,156	1.0 mm/35x35 mm								✓	✓	✓

RISC-V SoCs Solution

4/22/2021

RISC-V on FPGA

- RISC-V is a Modular, Extensible Architecture

- FPGA Implementations Preserve Flexibility to:
  - Optimize Dynamic Custom Instructions
  - Dynamically Select the Appropriate Architecture Extensions
  - Integrate Application Specific Hardware Accelerators

- FPGA retain the flexibility inherent in the RISC-V architecture even after deployment

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Efinix RISC-V SoCs

- VexRiscv based softcore, optimized to Trion / Titanium FPGAs
  - RISCV32I with M and C extensions, has five pipeline stages (fetch, decode, execute, memory, writeback)

SoC	Overview
Ruby SoC	• Cached, high-performance SoC with a DDR DRAM controller interface. Ideal for applications that provide real-time system controls and perform image signal processing.
Jade SoC	• Cached, general-purpose SoC that blends performance with a smaller footprint. Ideal for applications that use communications protocols, such as command and control, industrial automation or data logging.
Opal SoC	• Cacheless, compact SoC with a small resource footprint. Ideal for applications that require embedded compute capability such as system monitoring or remote configuration and control.

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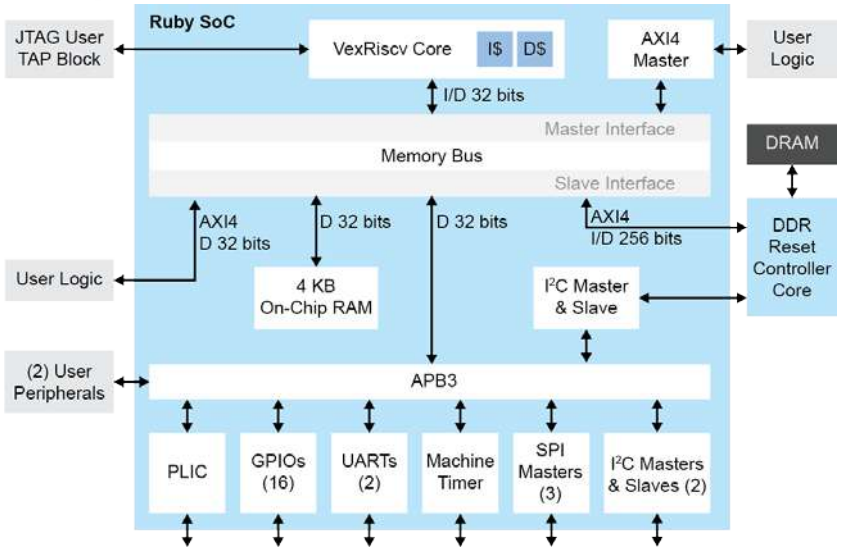
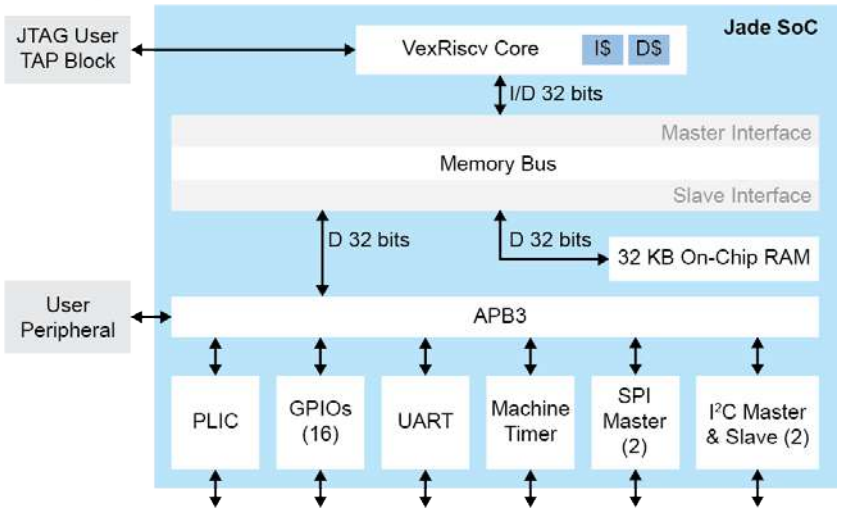
Ruby SoC



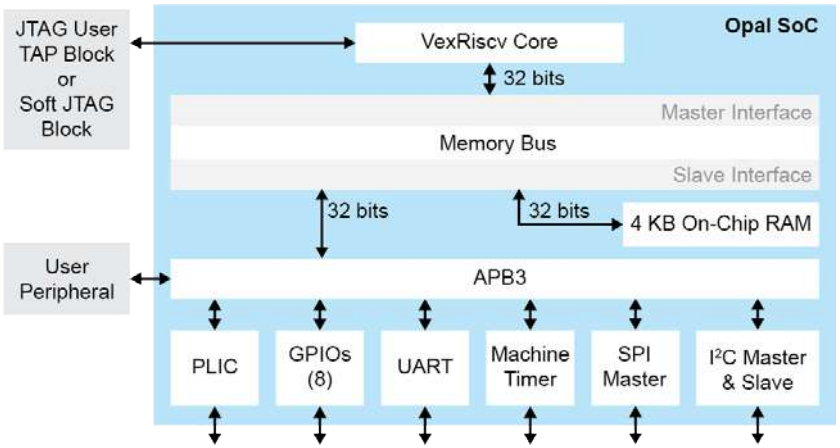
16 GPIOs
Timer
PLIC
3 SPI masters
3 I2C masters/slaves
2 UARTs
AXI4 user peripheral
2 APB3 user peripheral
AXI4 DDR memory access

Jade SoC



16 GPIOs
Timer
PLIC
SPI master
2 I2C masters/slaves
UART
APB3 user peripheral

Opal SoC

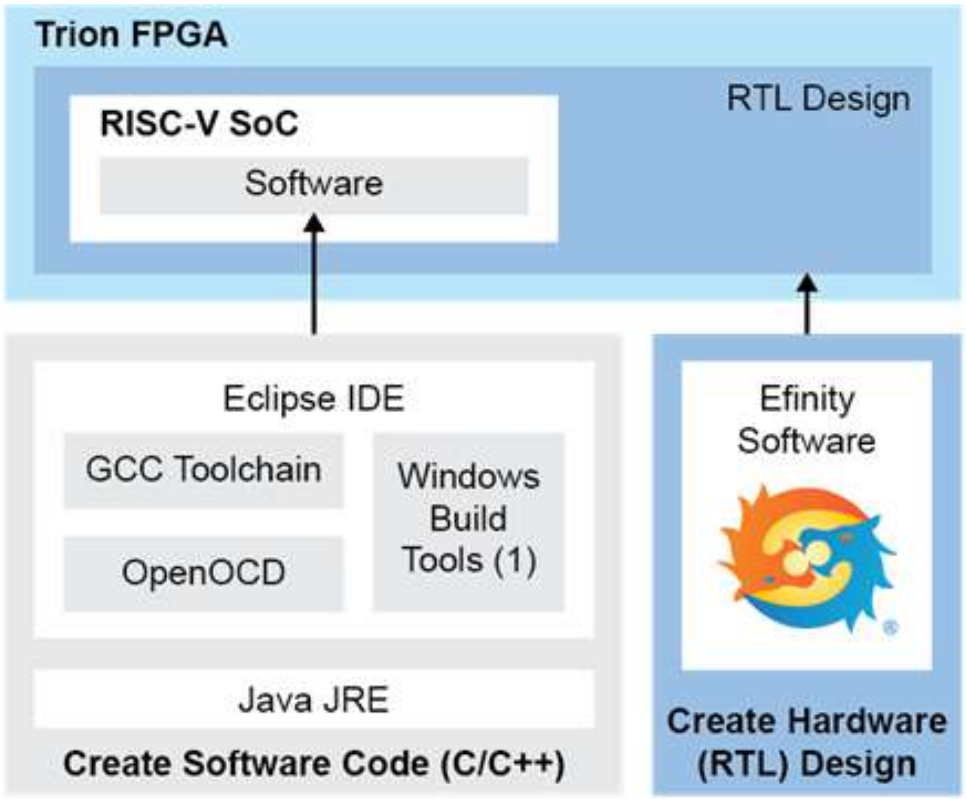


8 GPIOs
Timer
PLIC
SPI master
I2C master/slave
UART
APB3 user peripheral

A Complete Hardware & Software Package

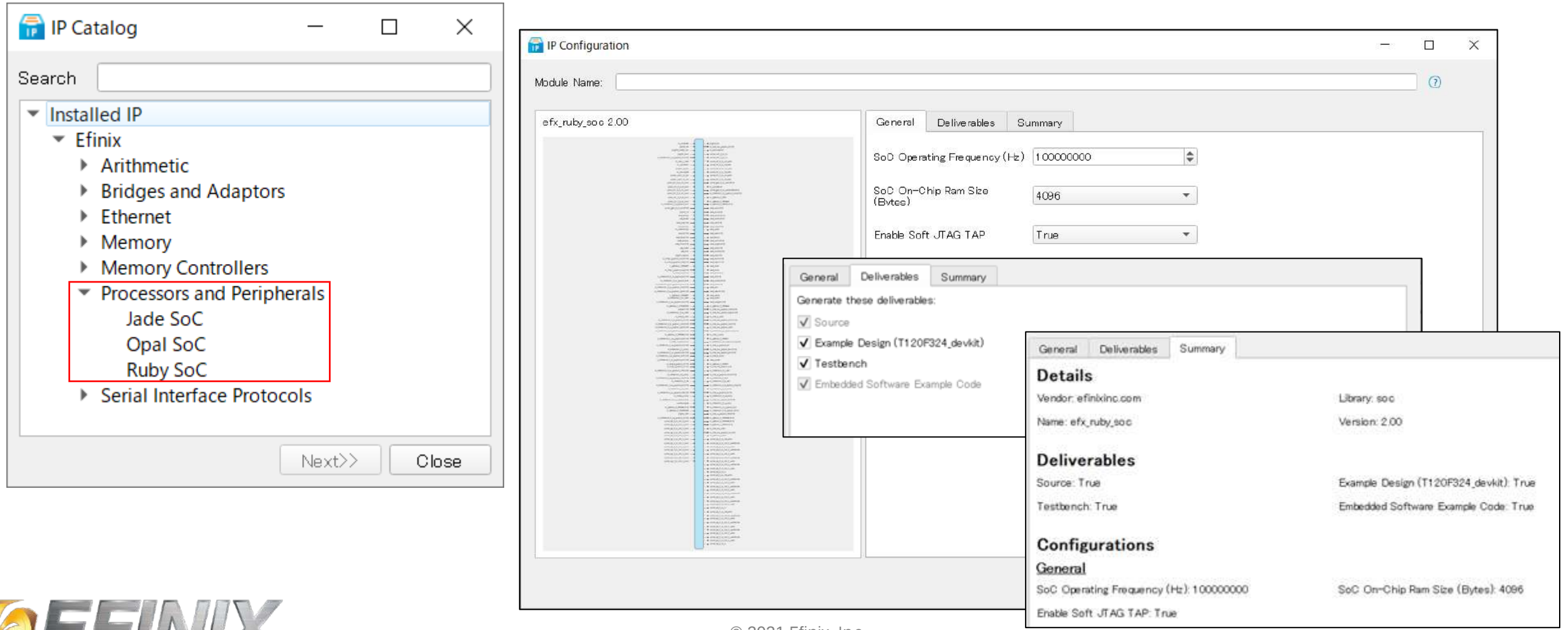
- Hardware Design (FPGA)
  - Efinity IDE Tool
    - SoC Core RTL Source
    - SoC Core Testbench
    - Dev. board example designs
    - Software examples
- Software Design (RISC-V)
  - RISC-V SDK
    - Eclipse IDE Tool
    - RISC-V GCC Compiler
    - RISC-V GDB Debugger
    - OpenOCD Debugger
    - Windows Build Tools*

* For Windows platforms



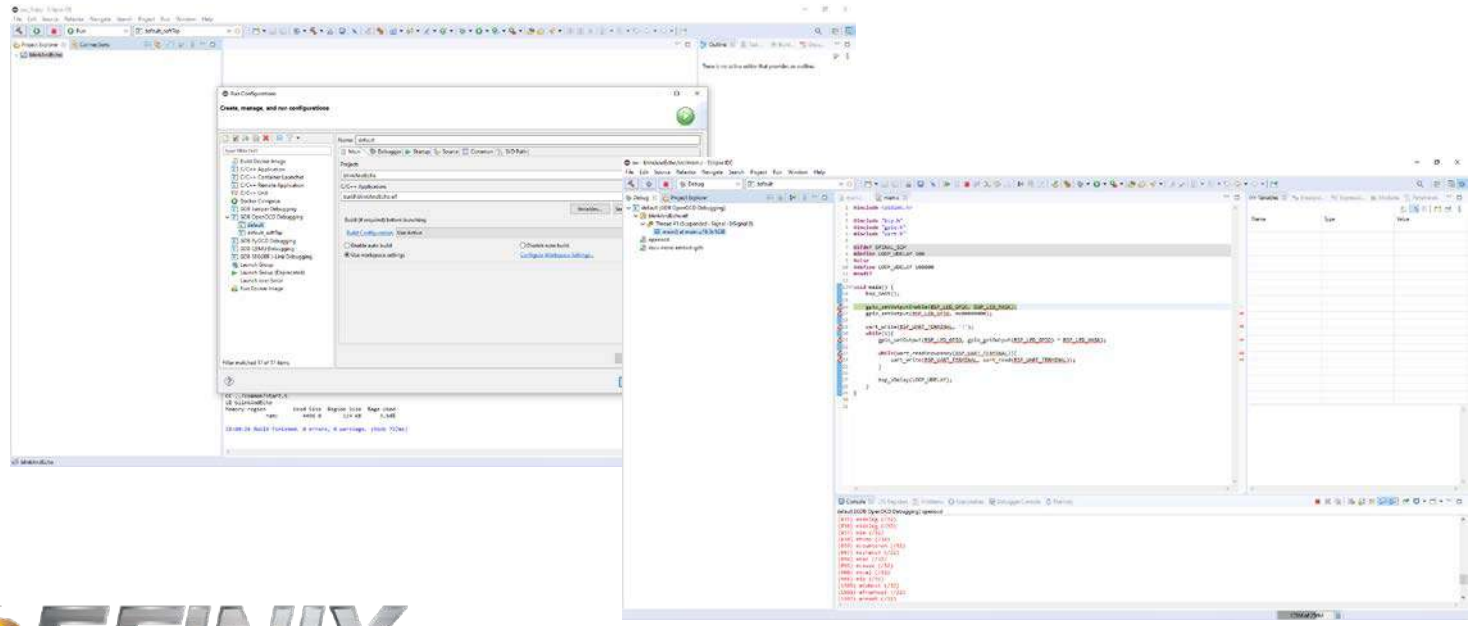
1. Windows build tools required on Windows platforms only.

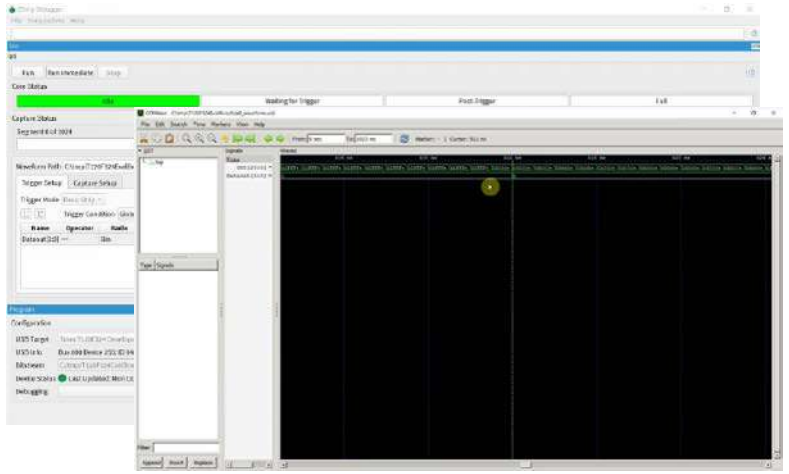
Easy to generate RISC-V SoC core by IP Manager in Efinity IDE



RISC-V SoC FW Development Flow

- Eclipse based SDK – to build your code
- OpenOCD Debugger – to download your binary, to debug your code
- Efinity Debugger – to debug RISC-V hardware (FPGA)



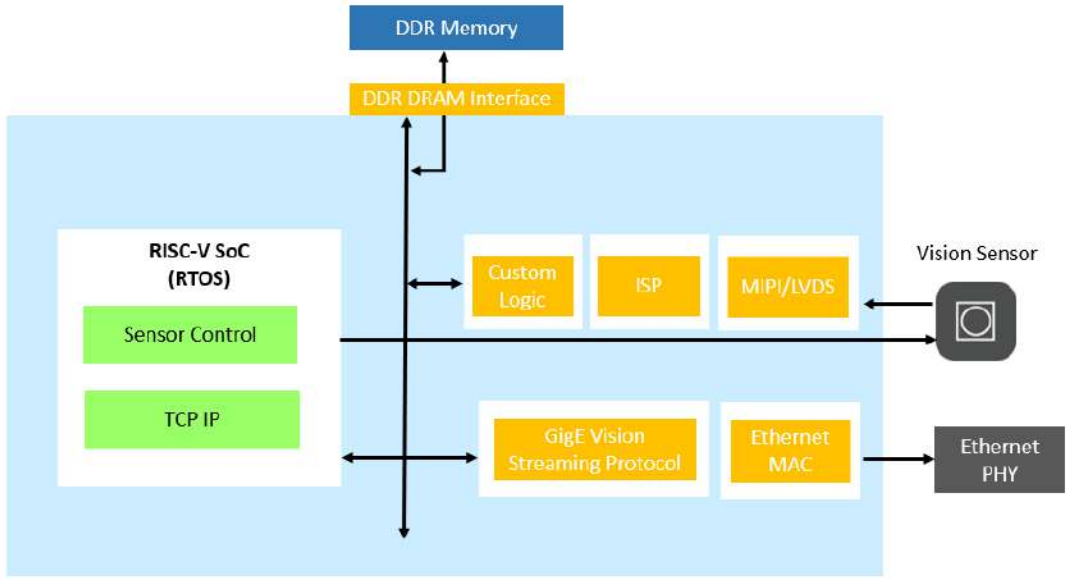


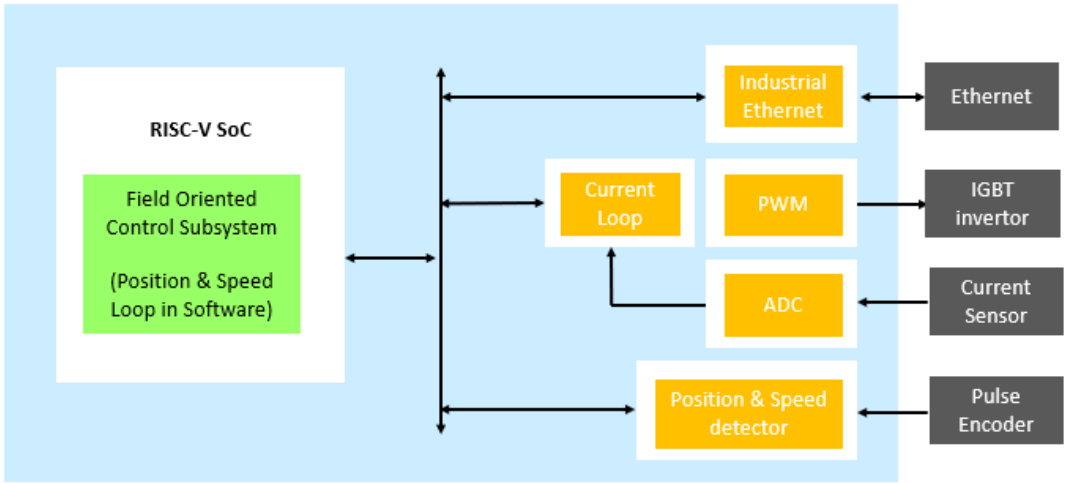
RISC-V SoC FW examples

- Easy to use and test with Efinix FPGA development kit
  - RubySoc with Free RTOS
  - RubySoc with Free RTOS + Triple-speed Ethernet IP
  - UART Demo
  - SPI flash bootloader Demo
  - I2C Demo
  - SPI Demo
  - Interrupt Demo
  - User Apb3 Demo
  - User AXI4 Demo
  - Memory Test Demo
  - Dhrystone Demo
  - Timer and GPIO Demo

RISC-V SoC Use Cases

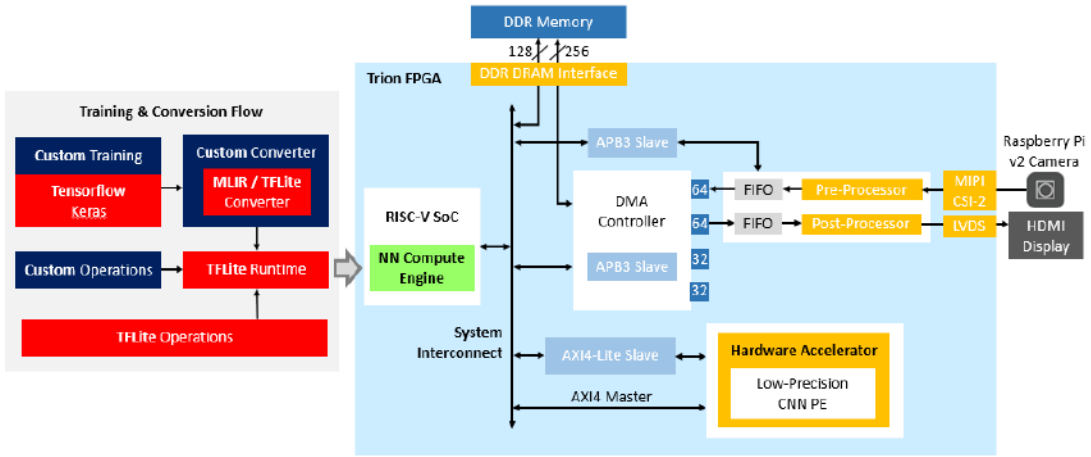
- Machine Vision
  - RISC-V running RTOS, for Sensor configuration and TCP IP
- Servo Motor
  - RISC-V running position and speed loops, while current control loop in the FPGA





RISC-V SoC Use Cases (cont.)

- AI inference on FPGA
  - RISC-V for data flow control, image pre-, post processing, and part of the NN layer



RISC-V SoCs Resource & Performance

RISC-V SoC		Ruby	Jade	Opal
Logic Elements (*)		~12,000 LEs	~7,000 LEs	~5,000 LEs
RAM Blocks (*)		78	93	16
FPGA Speed	Titanium	~400 MHz	~400 MHz	~400 MHz
	Trion	~100+ MHz	~100+ MHz	~100+ MHz
DMIPS/MHz		1.16	1.2	0.98
OS Support		FreeRTOS / Linux	N/A	N/A
Delivery		Free / No Royalty	Free / No Royalty	Free / No Royalty

* Trion based LEs and Memorks incl. basic peripherals

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Efinix RISC-V SoC Near Term Plan

Planned Items

- Titanium Support
- Enable custom instruction acceleration
- Enable Linux Buildroot
- Enable SoC configuration through IP-Manager

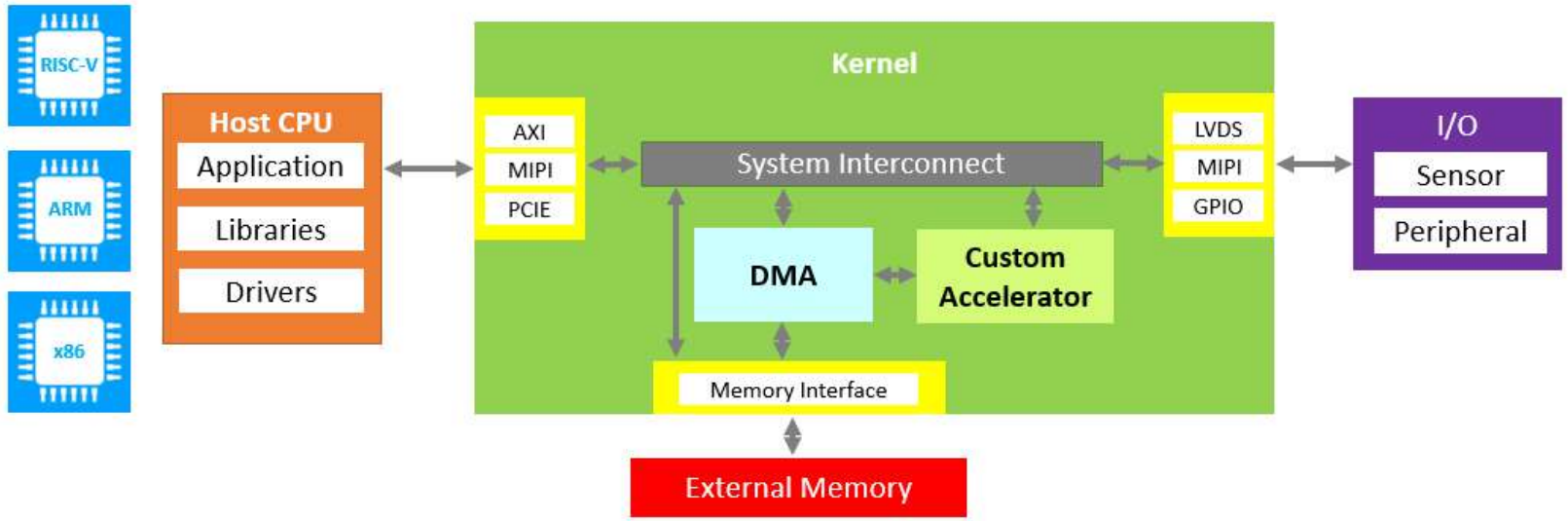
Ballpark Items

- Multi-core Support
- 64-bit core Support
- …

Efinix Quantum Accelerator

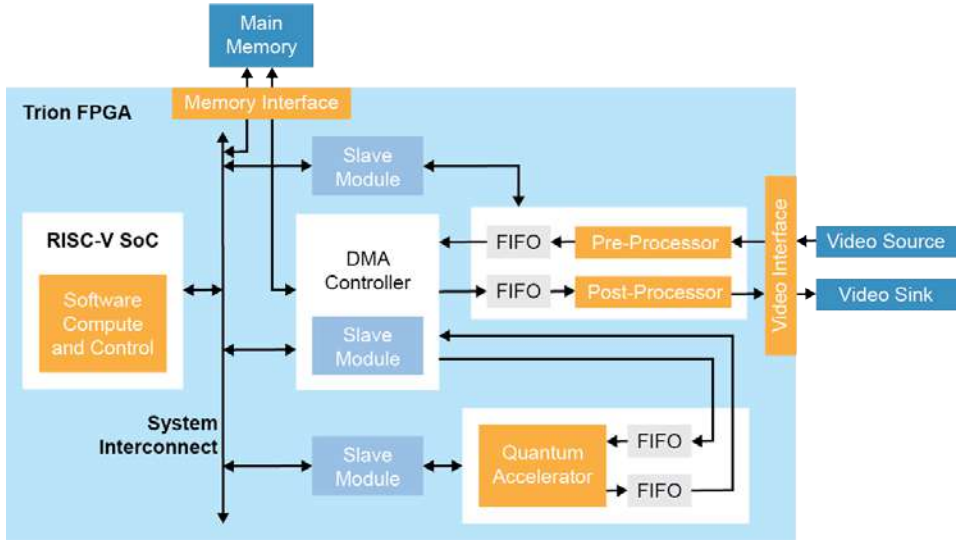
Quantum Accelerator

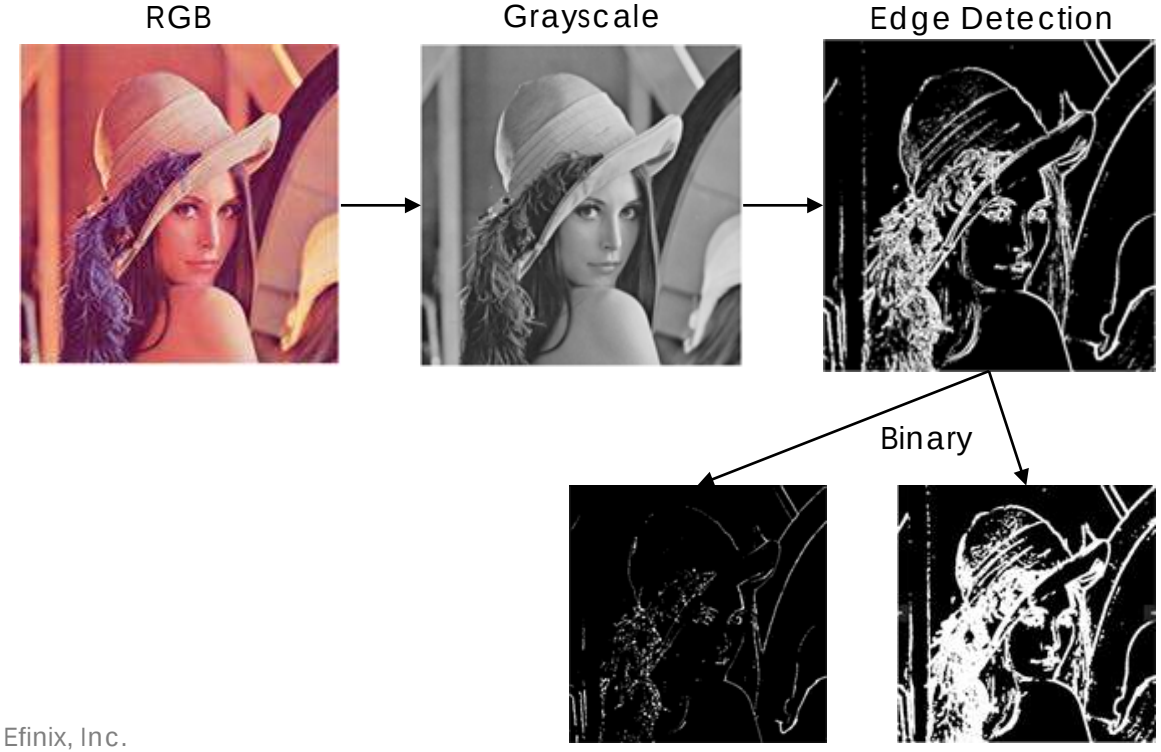
- Pre-defined, structured "containers" that streamline user's acceleration efforts
- Pre-defined sockets are provided for user to incorporate a hardware accelerator quickly and easily



Edge Vision SoC Framework

- The 1st release of Quantum Accelerator Framework
  - Facilitate Hardware/Software Partitioning and achieve the desired performance
  - Example designs for specific functions, such as video processing, AI object detection, machine learning, multi-camera fusion, etc.
  - Quick run and test on Trion T120 kit
  - Available in our website or GitHub

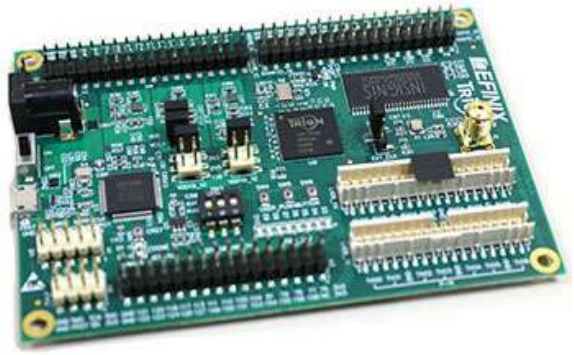




Available Development Boards

T120F324C-DK ($300)

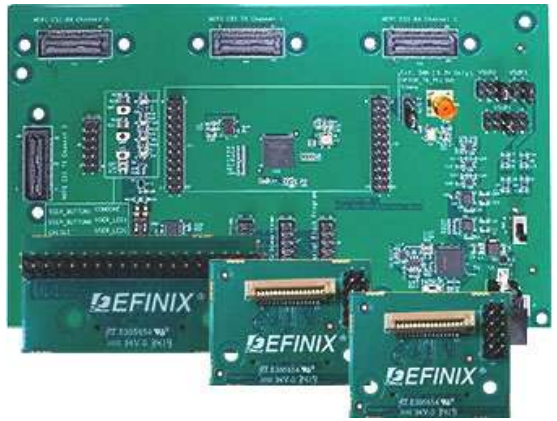
T20F256C-DK ($150)



T8F81C-DK ($100)

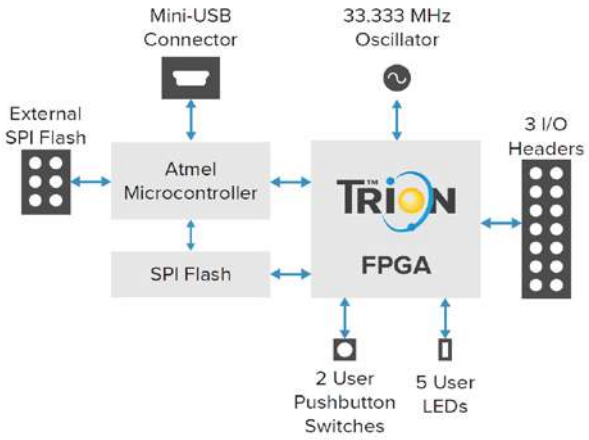
T120F576C-DK ($350)

T20MIPI-DK ($150)



Trion T8 Development Kit Promotion

- Trion T8 Development Kit 50% Discount to RISC-V Days Tokyo 2021 attendees
- T8F81C-DK
  - Trion T8 FPGA
  - 5 User LEDs, 2 User Push Button Switches
  - Type B mini-USB Port (FLASH Program, Power)
  - 3 Expansion I/O Headers
  - 33.333 MHz Oscillator
  - Efinity IDE (support All Efinix FPGAs)
- Promotion Code: **T8-RISCVTKY21S**
- For more details, contact to local sales, distributors or mail to sales-jp@efinixinc.com



Thanks