Achieving Ultimate Power Efficiency with Efinix FPGAs and the UNO Labo Single-Stage RISC-V Core

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Efinix Corporate Overview

- **Our Mission Statement**

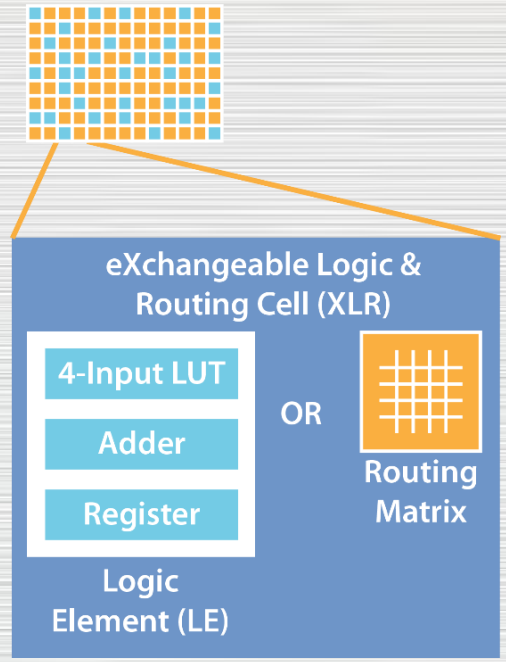
  "We Deliver Easy to Use, Low-Power, Efficient FPGA Solutions for Mainstream, High Volume Applications"

- **Efinix is**
  - Rapid growth US based FPGA company (founded in 2012)
  - Delivering Easy to Use, Low Power and Efficient FPGA Solutions through disruptive Quantum Technology
  - Global Company with Offices Worldwide
- **Products & Solutions**
  - Titanium FPGAs – mid~high LEs, high-performance, low-power FPGA w/hard blocks
  - Trion FPGAs – small~mid LEs, lower-power, cost-effective FPGA with stable delivery
  - RISC-V SoCs – Easy to Use, Soft-define CPU (***500+ downloads in 2021 from 50+ in 2020***)
  - Efinity IDE – Providing a complete RTL-to-bitstream flow

The Efinix XLR Advantage

QUANTUM™

Quantum™ XLR



The XLR Can Be Used As Logic Or Routing

Architectural Efficiency

- *Flexible & Fine-Grained FPGA*
- *Removes Traditional FPGA Routing*
- *Ideal Logic/Routing Ratio for Every Design*

Efinix Advantage

- *100% Utilization Ratios*
- *Small Size and Low Cost*
- *Low Power and High Efficiency*

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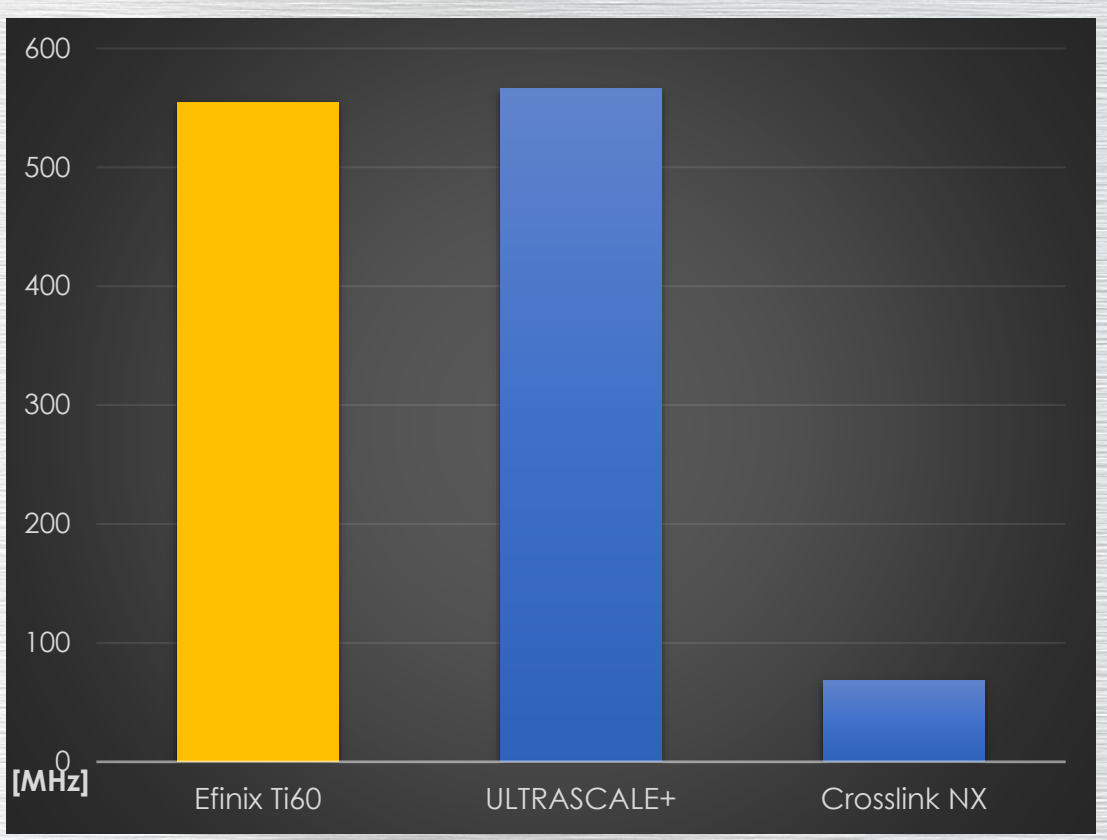
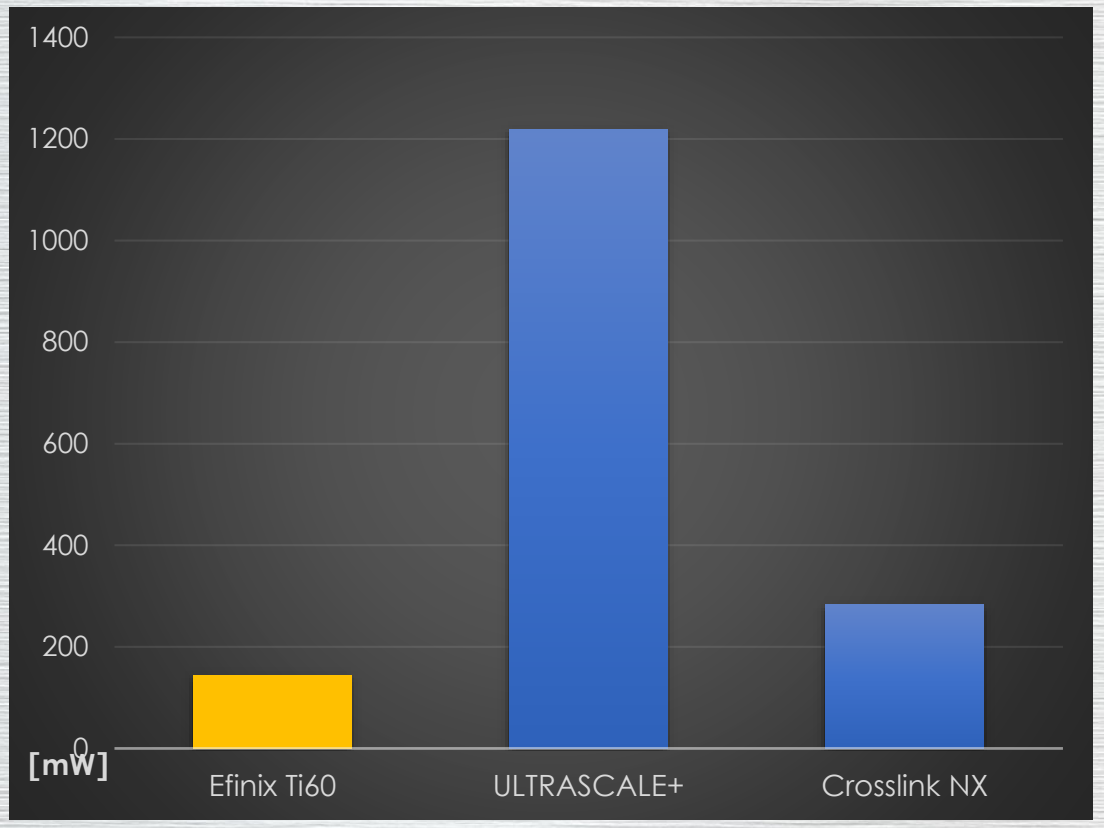
Titanium™ FPGA Benchmark

Performance Comparison



Power Comparison



Benchmark design: Gaussian Noise Generator (https://github.com/liuguangxi/gng)

Titanium™

- mid~high LEs FPGA with 16nm process
- 35,000 ~ 1,000,000 LEs
- Security
- SEU
- 2.5Gbps MIPI D-PHY
- 16Gbps/25.8Gbps Serdes
- PCI Express Gen 4 (16G)
- LPDD4 Memory Controller

Feature	Ti35	Ti60	Ti90	Ti120	Ti180	Ti240	Ti375	Ti550	Ti750	Ti1000
Logic Elements (LEs)	36,176	62,016	92,534	123,379	176,256	236,888	370,137	533,174	727,056	969,408
10K RAM Blocks (Mb)	1.53	2.62	6.88	9.80	13.11	19.37	27.53	39.65	54.07	72.09
DSP Blocks	93	160	336	448	640	946	1,344	1,936	2,640	3,520
High-Speed I/Os (HSIOs)	146	146	232	232	232	172	172	268	268	268
GPIOs (3.3 V)	34	34	80	80	80	80	80	80	80	80
PLLs	4	4	10	10	10	10	10	10	10	10
DDR4/LPDDR4/DDR3/LPDDR3	-	-	x32	x32	x32	x72	x72	2 x72	2 x72	2 x72
MIPI D-PHY 2.5 Gbps (Rx, TX)	-	-	(4, 4)	(4, 4)	(4, 4)	(3, 3)	(3, 3)	(3, 3)	(3, 3)	(3, 3)
16 Gbps Serdes	-	-	x8	x8	x8	x12	x12	x16	x16	x16
25.8 Gbps Serdes	-	-	-	-	-	-		x8	x8	x8
PCI Express Gen 4 (16G)	-	-	1 x4	1 x4	1 x4	2 x4	2 x4	2 x8	2 x8	2 x8
Automotive Support	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Trion™

- middle LEs FPGA with 40nm process
- 4,000 ~ 120,000 LEs
- 1.5Gbps MIPI D-PHY + CSI-2 Controller
- DDR3 Memory Controller
- 6M+ shipping in WW
- High Quality

Feature	T4	T8	T13	T20	T35	T55	T85	T120
Logic Elements (LE)	3,888	7,384	12,828	19,728	31,680	54,195	84,096	112,128
MPM (Mask Programmable Memory)	✓	✓	✓	✓	-	-	-	-
5K RAM Blocks (kb)	77	123	727	1,044	1,475	2,765	4,055	5,407
18x18 Multiplier Blocks	4	8	24	36	120	150	240	320
Maximum GPIOs	55	97	195	230	230	278	278	278
PLLs	1	5	5	7	7	8	8	8
DDR3/LPDDR3/LPDDR2	-	-	x32	x32	x32	x72	x72	2 x72
MIPI D-PHY + CSI-2 (Rx, TX)	-	-	(4, 4)	(4, 4)	(4, 4)	(3, 3)	(3, 3)	(3, 3)
Automotive Support	-	-	✓	✓	-	-	-	-

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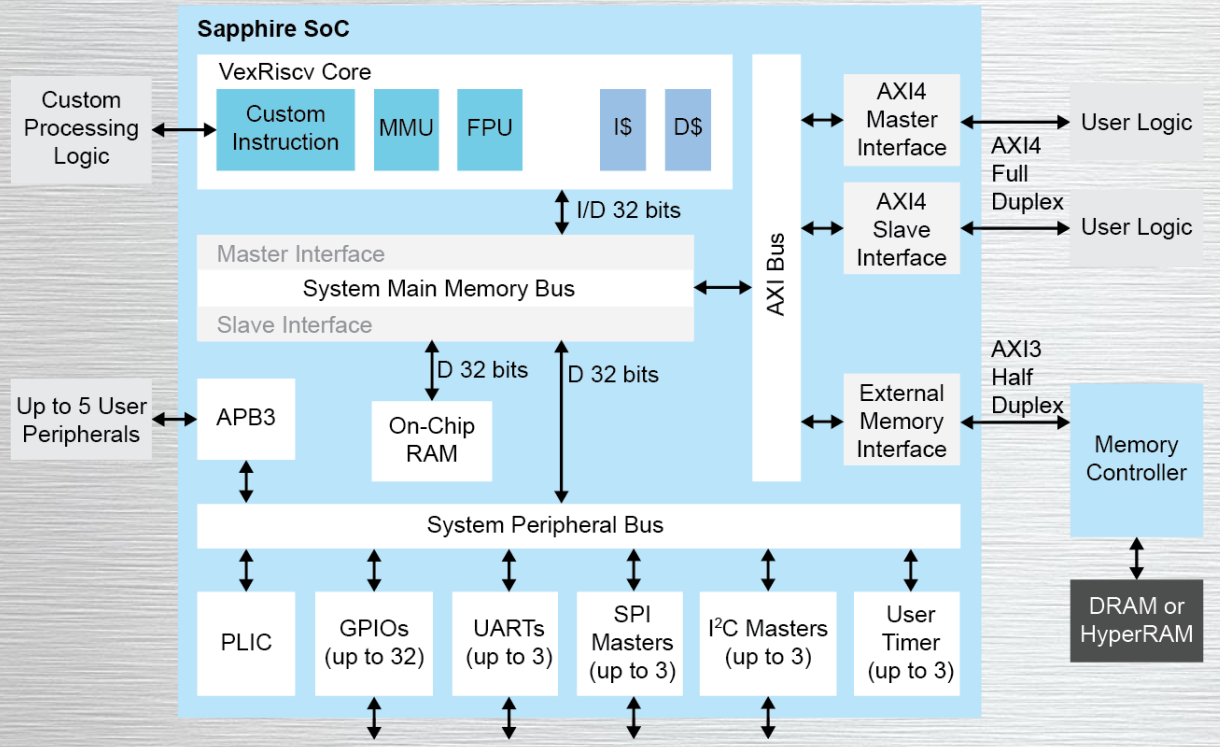
Efinix Sapphire RISC-V SoC

Sapphire RISC-V SoC

- **User configurable** RISC-V SoC based on the **VexRiscv** core, which is a **32-bit CPU** with **six pipeline stages** and a **configurable feature set**.



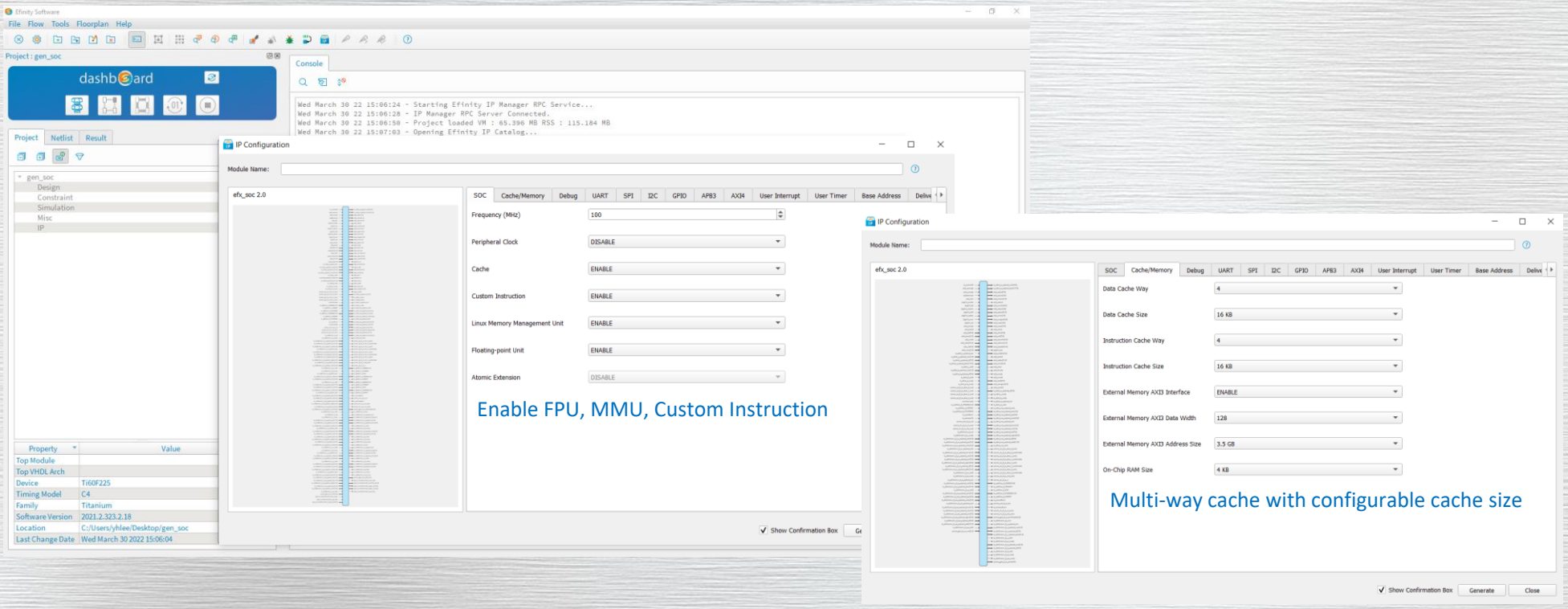
Best Features

- **Most configurable Risc-V SoC** with **Custom Instruction Extension**, take best advantage of Risc-V ISP architecture on Efinix programmable hardware

	Efinix Sapphire SoC	Intel NIOS-V/m	Microchip Mi-V	Lattice RiscV MC
RISC-V Base Architecture	RV32IM	RV32IA	RV32IAMF	RV32I
Pipeline Stage	**6 Stages**	5 Stages	5 Stages	5 Stages
Optional Extension	**A-、F-、D-、C-**	-	-	C-
Data & Instruction Cache	**User Configurable**	4KB、4KB	8KB、8KB	4KB、4KB
On-Chip RAM	**User Configurable**	-	-	-
Multi-way Cache Controller	✓	-	-	✓
Custom Instruction Extension	✓	-	-	-
Floating Point Unit	**Single & Double Precision**	-	Single Precision	-
MMU	✓	-	-	-
Multi-Core	✓	-	-	-
OS	**FreeRTOS Linux Buildroot**	uC/OS-II	-	-

Ease of Use

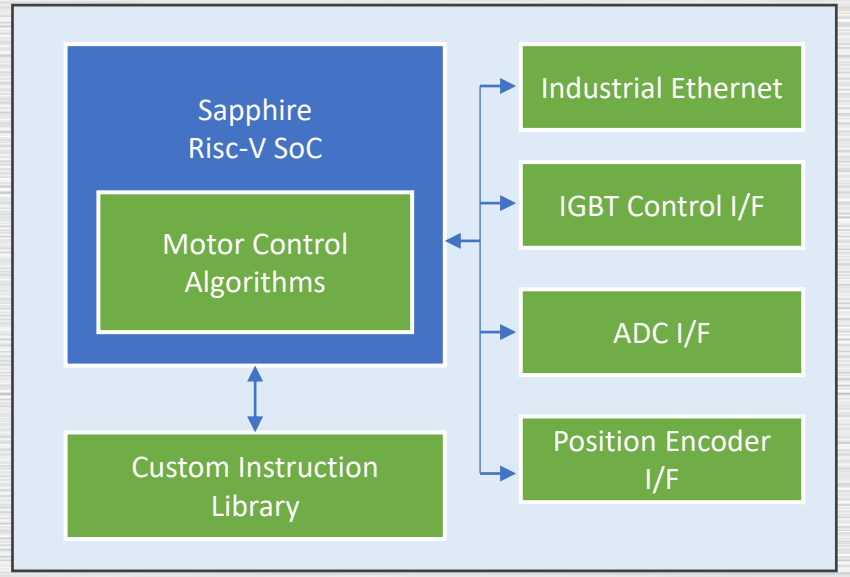
- **Push button SoC generation** from Efinity IP-Manager. Total design package includes RTL, embedded software, example design, and testbench generated automatically, no need to design in separate SoC design tool.



FPGA is the best choice for Custom Instruction Extension

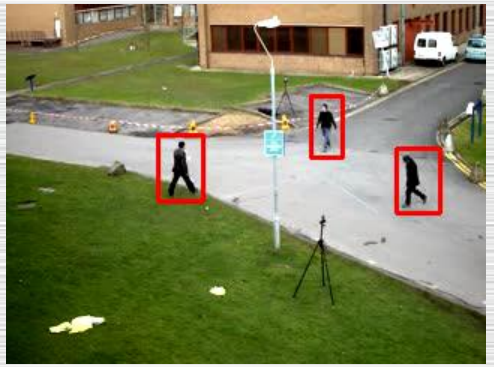
- **Custom Instruction Advantage**
  - middle point to resolve hardware-software design trade-offs.
  - Provide notable speed-up with less RTL design effort (straightforward interface).
  - Ease of use for software-level users.
- **FPGA – Highly flexible**
  - User to define & implement custom instructions based on application need.
  - **Easy to reconfigure & update instruction as required.**
  - **Suitable for quick changing, state-of-the-art applications.**
  - Facilitate invention and innovation in industry & academia.
- **ASIC – Pre-defined & Specific**
  - ASIC chip designer defines a set of custom instructions at development stage.
  - Targeting specific processing or operations of a particular application domain.

- **Use Case: Industrial Servo Motor Control**
  - Custom Instruction Extension to accelerate Motor Control Algorithms
  - **Platform based design**, develop list of acceleration libraries to cover >100 of different version of products

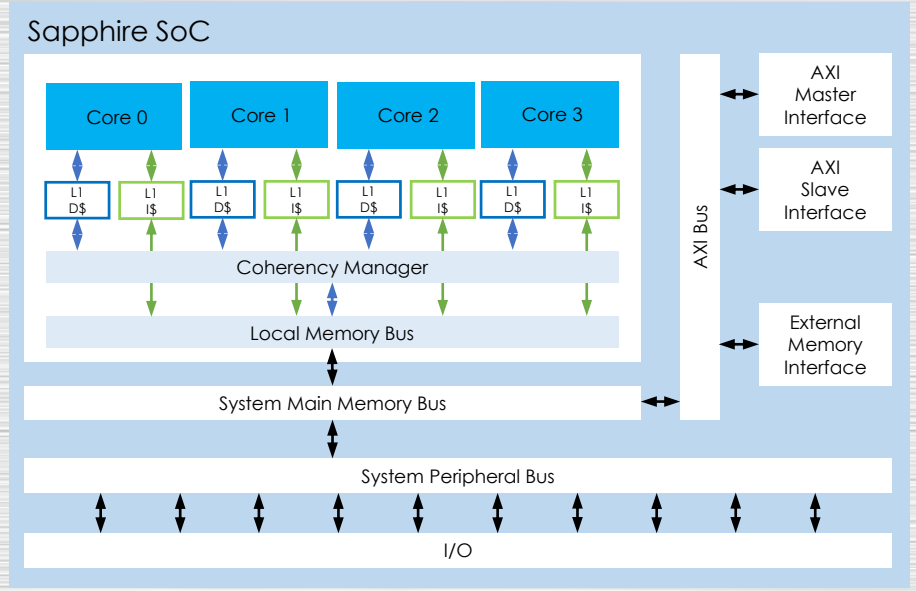


Efinix RISC-V SoCs near term milestone

- **Linux Buildroot**
  - Sapphire SoC support Linux Buildroot in 2022.1
  - Release under Efinix Github
  - Running Open-CV on Linux
    - Ease of design in software environment with rich **open-source library**

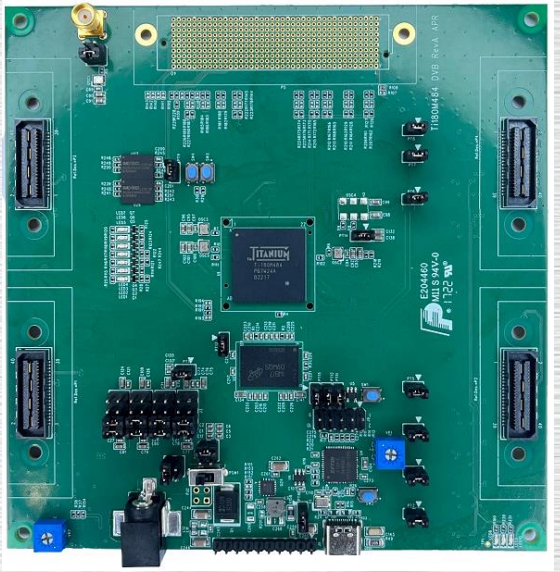


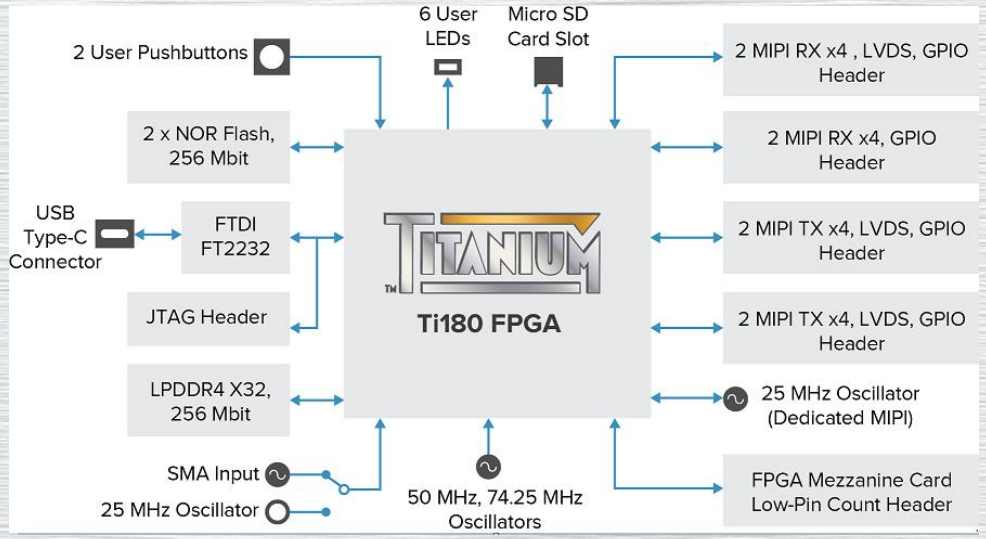
- **(Symmetric) Multi-Processor**
  - Sapphire SoC support Symmetric Multi-Processor in 2022.1
    - Offer next level of performance scaling



Ti180M484 Development Board

- Main Features
  - Ti180 FPGA in a 484-ball FineLine BGA package
  - 256 Mbit, x32 data width LPDDR4 SDRAM, 1866 MHz maximum clock rate, and up to 3733 Mbps double-data rate
  - 2x 256Mb SPI NOR flash memories
  - Four MIPI, LVDS, and GPIO high-speed connectors to attach daughter cards
  - FMC LPC connector
  - Micro-SD card slot
  - USB Type-C connector for programming the flash or Ti180 FPGA using the Efinity® software
  - 6 User LEDs
  - 2 User pushbutton switches
  - 25 MHz, 50 MHz, and 74.25 MHz oscillators for PLL input
  - 25 MHz oscillator for MIPI clock
  - 12.0 V power supply connector
  - Estimated Resale Price: $850





Join Live Demonstration

- Efinix will demonstrate “Bio-Power Comparison”, “Edge Vision”, and “Object Tracking AI” with Trion and Titanium FPGAs
- May 31st, 16:00～17:00、18:00～19:00
  - https://us02web.zoom.us/j/85452121727?pwd=VFV3N0FXN3hLRldCOFpXNGdSQXNsdz09
  - Zoom Meeting room: 854 5212 1727　　Password: 020850
- Jun 1st, 10:00～11:00、12:00～13:00、17:00～18:00
  - https://us02web.zoom.us/j/84675344541?pwd=K3NKYVl5Tm9la2NwbkJRZWVGdkVMQT09
  - Zoom meeting room: 846 7534 4541　　Password: 619686
- Jun 2nd, 11:00～12:00、13:00～14:00、16:00～17:00
  - https://us02web.zoom.us/j/81080829017?pwd=Zk1LQ1V5ZUZuN1plc3FsSmlxSlMyZz09
  - Zoom meeting room: 810 8082 9017　　Password: 669906

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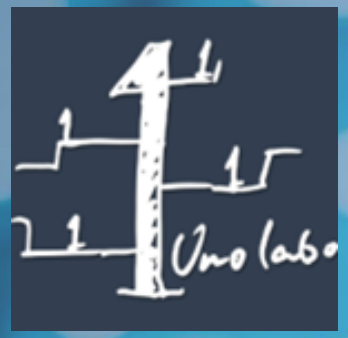


Achieving Ultimate Power Efficiency with Efinix FPGAs and the UNO Labo Single-Stage RISC-V Core

UNO Laboratories, Ltd.
https://www.unolabo.co.jp

Company Profile：UNO Laboratories, Ltd.

＊ Established in 2017

＊ Started joint research on micro-architecture of embedded processors with Hirosaki University in 2018

Development of the highly efficient Single-Stage RISC-V processor

Single-Stage RISC-V (RV32IM) core optimizes operations by removing instruction read time, making one instruction cycle into one stage, which can be processed in one clock cycle.
This ensures energy-efficient operation with no processing waste.

To reduce reading time of instructions by eliminating IR (instruction register) and directly connecting the instruction memory to the instruction decoder.
⇒ Mitigating the Neumann Bottleneck

Application

- Embedded in IoT devices such as sensor nodes that must operate continuously in locations where battery replacement is difficult
- Embedded in a variety of monitoring devices, including those for healthcare applications
- Edge computing for image processing

Example implementation of Single-Stage RISC-V core with patented technology

【1】FPGA

① Xilinx Artix-7 (100T) * Joint research with Hirosaki University

- The power consumption (J) of 512,000 loops of the Dhrystone benchmark using Arty A7 is 6.4% of that of Micro Blaze with 5-stages pipeline.
- It has also been demonstrated that Single-Stage RISC-V core can be implemented in the Arty-A7 to continuously measure the oxygen saturation of human tissues for more than two days with a single AA NiMH rechargeable battery.

※ Paper presented at GCCE 2021 Title: An Energy Efficient Processor Applicable to Continuous SPO2 Monitoring

② Efinix Trion T20 BGA256 / Titanium Ti60 F225

③ Efinix RISC-V SoC (Sapphire SoC)

*VexRiscv core replaced by Single-Stage core.

【2】ASIC (Joint research with Hirosaki University)

① ASIC prototypes with ROHM 180 nm have been completed. (February 2022)

② ASIC prototypes using **Renesas Electronics SOTB 65nm** to be completed. (August 2022)

Comparison of operation between 1-stage and 5-stages

【 Architecture Comparison Diagram 】

Eliminate IF

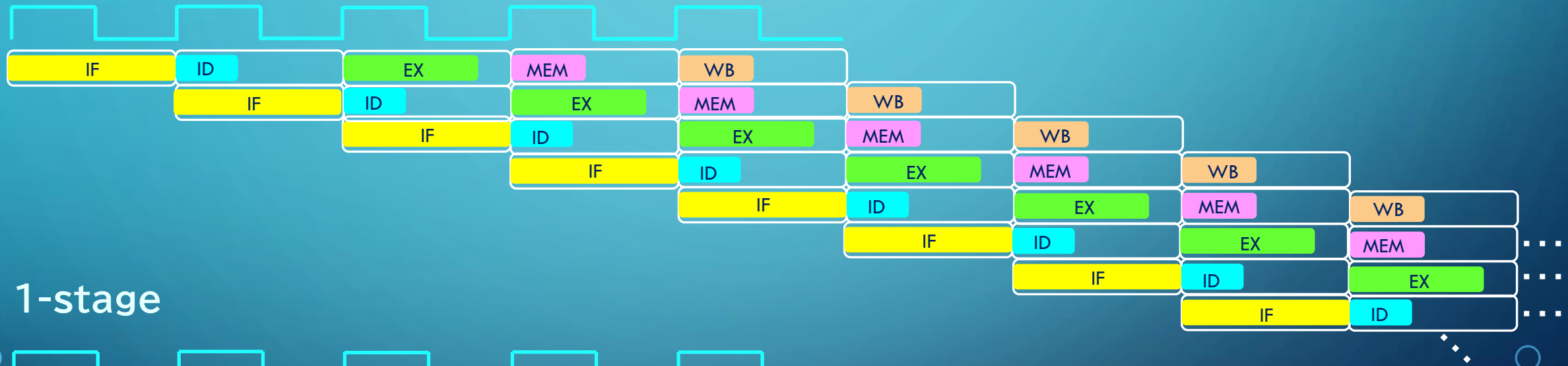
- Patented technology eliminates Instruction Fetch stage (IF).
- One instruction cycle can be processed in one stage with one clock.

※Although the critical path becomes longer as the amount of processing per clock increases, the processing efficiency is higher than the pipeline at the same frequency.

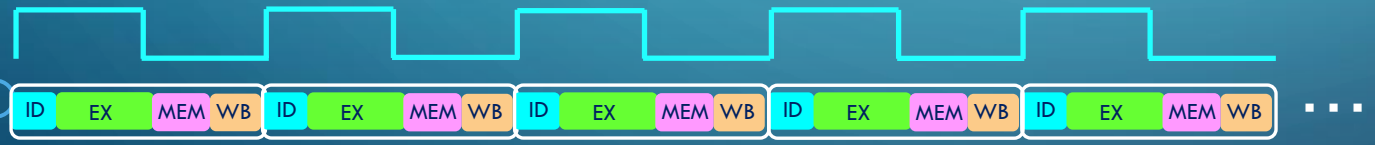
※Since Single-Stage core operates with instruction memory directly connected to the instruction decoder, its greatest strength is in executing programs of relatively compact size without waste.
It is not suitable for storing programs as large as Windows/Linux OS, but it can store RTOS.

Comparison of operation between 1-stage and 5-stages pipeline

5-stages Pipeline



1-stage



Single-Stage architecture returns to the original program on the next clock cycle after branch or interrupt completes, eliminating the need to discard the loaded program or reload the program as in pipelined processing, thus preventing operational delays. This improved operation results in highly efficient operation.

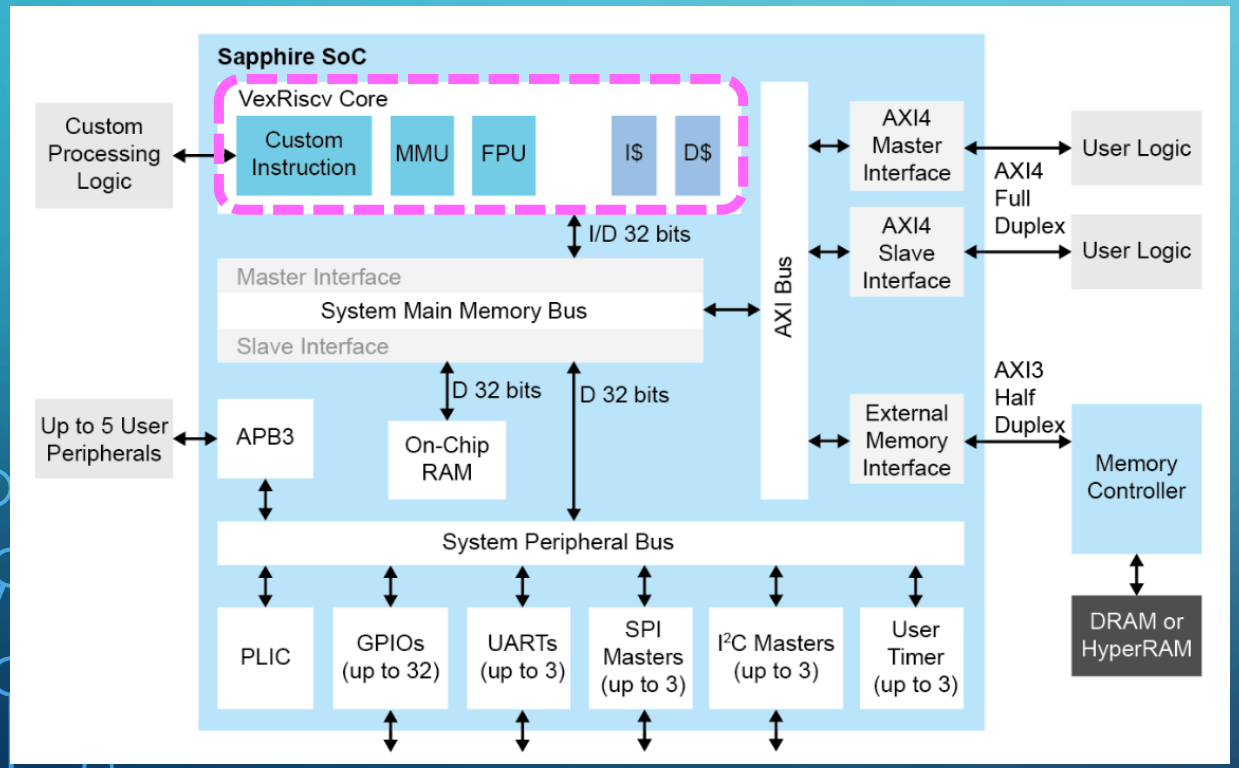
Integration of 1-stage/2-stages RISC-V cores and Efnix Sapphire SoC

To be released under GitHub

2-stages core with emphasis on power efficiency will also be released.
(No instruction readout in 2-stages core as well as 1-stage core)

Replaced 6-stages pipeline VexRiscv core with 1-stage/2-stages cores

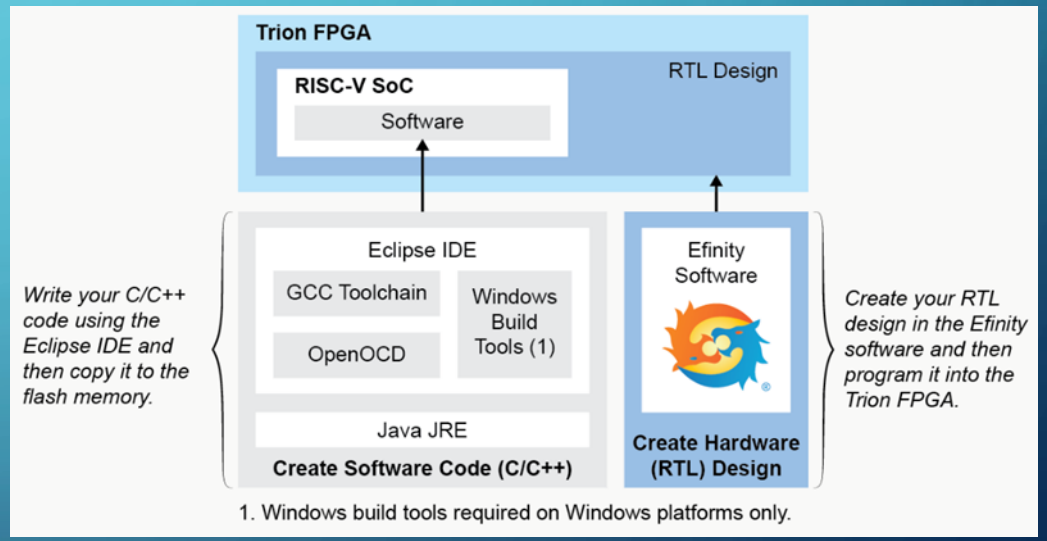
※Plans to apply to Edge Vision SoC



Sapphire SoC block diagram

RISC-V SDK can be used for software development of 1-stage/2-stages cores.

Sapphire SoC Design Flow



-Eclipse IDE
-RISC-V GCC
-RISC-V GDB
-Open OCD

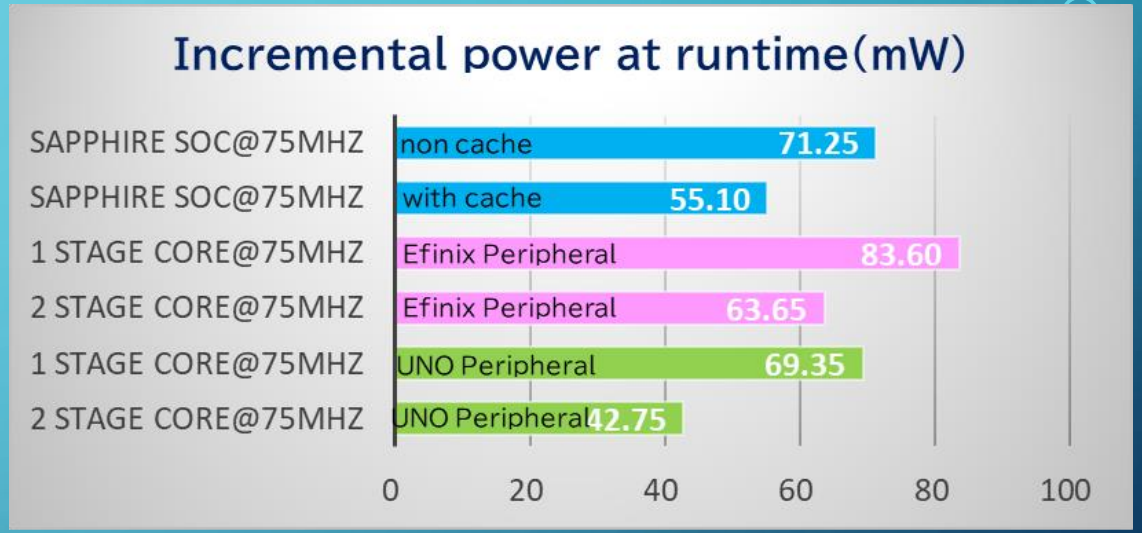
Reference URL: Efinix, Inc. (efinixinc.com)

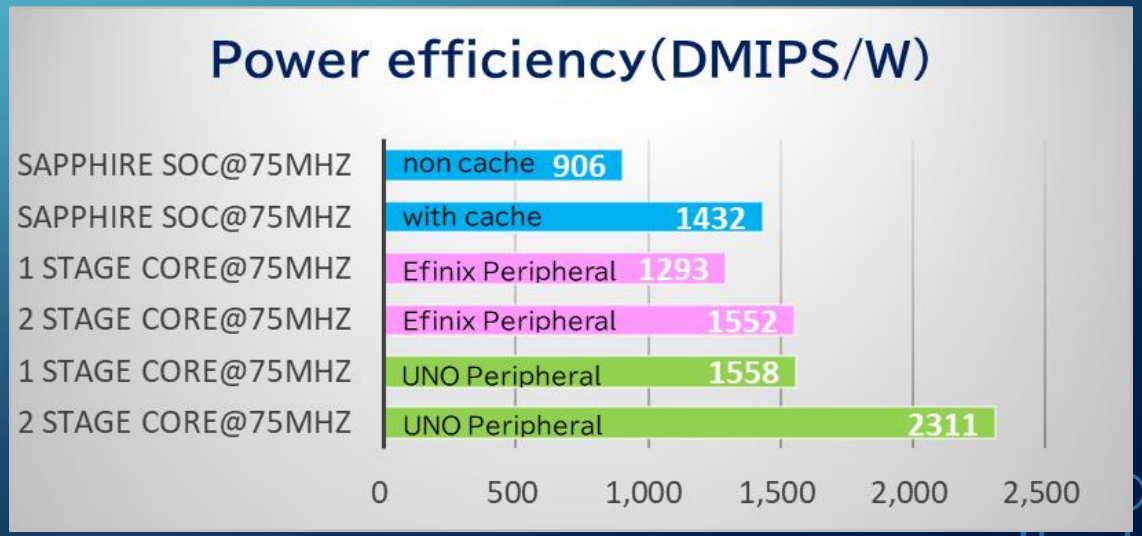
Power Efficiency Comparison
Titanium Ti60 F225

Dhrystone Benchmark Results
*512,000 loops

Efinix FPGA	Titanium Ti60 F225 IMEM:32KB DMEM:32KB 75MHz			
	1-stage non cache	2-stages non cache	Sapphire (6-stages) non cache	Sapphire (6-stages) with cache
DMIPS/MHz	1.44	1.32	0.86	1.05
DMIPS/W *SoC (Efinix Peripheral)	1293	1552	906	1432
※Reference DMIPS/W *non SoC (UNO Peripheral)	1558	2311		

*Comparison in our company
*no cache required for 1-stage/2-stages cores





Logic Resource Usage Comparison
Titanium Ti60 F225

Titanium Ti60 F225 IMEM:32KB DMEM:32KB		CPU Core		
		FFs	LUTs	RAMs
Sapphire SoC	non cache	1616	2506	68
Sapphire SoC	with cache	1941	2872	80
1-stage Core *SoC (Efinix Peripheral)	non cache	2028	4948	64
2-stages Core *SoC (Efinix Peripheral)	non cache	1182	3201	68
*Reference 1-stage Core *non SoC (UNO Peripheral)	non cache	1862	4739	64
*Reference 2-stages Core *non SoC (UNO Peripheral)	non cache	1013	3128	68

*Comparison in our company
*no cache required for 1-stage/2-stages cores

Future Plans

【Scheduled for release】

● **Free version** 1-stage/2-stage RISC-V core for implementation on Efinix Sapphire SoC
※Free version with encryption and 1-hour usage limit *T20BGA256, Ti60F225
※Release under unolabo Github https://github.com/unolabo.

● **Paid version** 1-stage/2-stage RISC-V core for implementation on Efinix Sapphire SoC
※No 1-hour usage limit
※UNO Peripheral version of the 1-stage/2-stages RISC-V cores will also be released.

【The Challenges of Low-Cost Normally-Off Computing】

ASIC prototype in collaboration with Hirosaki University

① ASIC prototype using **Renesas Electronics SOTB 65nm** to be completed. (August 2022)
② **Asynchronous ASIC** prototype that take advantage of 1-stage operation will be planed.
<Advantages of an asynchronous ASIC implementing 1-stage RISC-V core>
＊Near-zero standby power
＊No asynchronous circuit design tools required, **synchronous design tools can be used.**

We aim to contribute to energy harvesting in IoT devices by developing processors that reduce energy consumption.