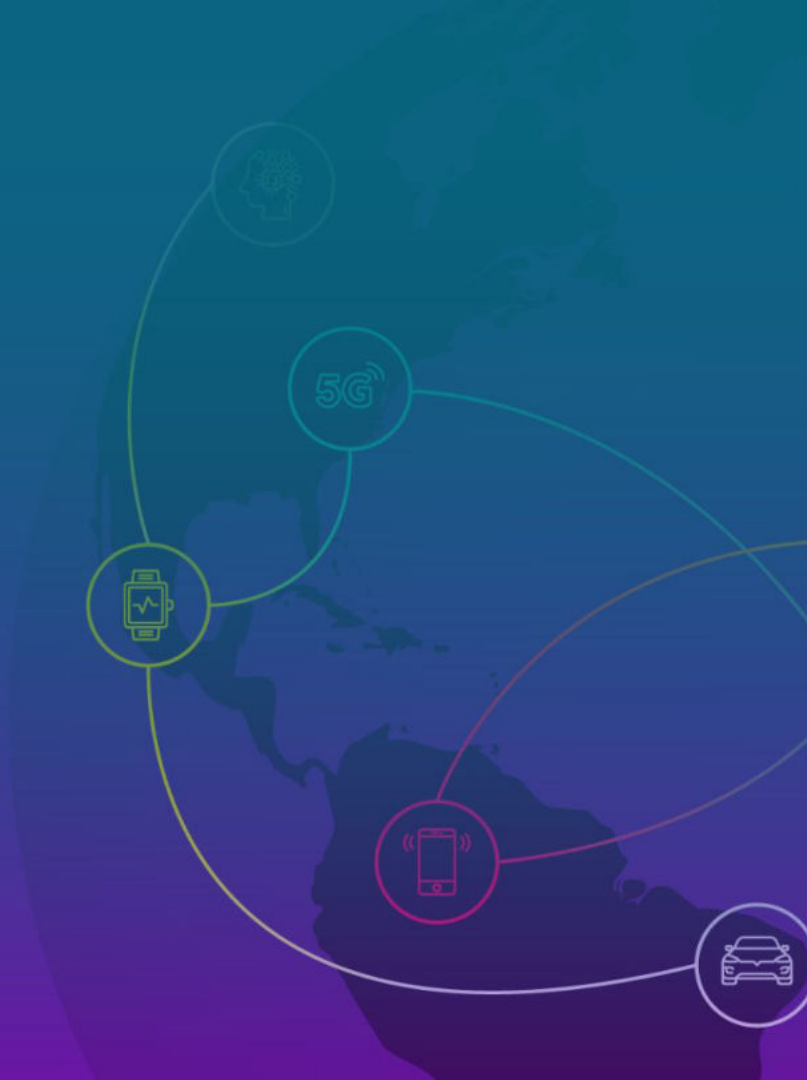
RISC-V® Everywhere

Calista Redmond
CEO, RISC-V International

November 2022



Open standards and collaboration are strategic to hardware and software across industries and geographies.

RISC-V®

RISC-V is the most prolific and open Instruction Set Architecture in history

- RISC-V is inevitable
- RISC-V enables the best processors
- RISC-V is rapidly building the strongest ecosystem

RISC-V is inevitable

RISC-V Mission:
RISC-V is the industry standard ISA across computing

>10 Billion RISC-V cores already shipped.

- Innovation and adoption moving rapidly across all domains
- Demand at every performance level (low to ludicrous)
- Shared investment is driving the fastest growing ecosystem

Leverage a community ISA spec development model

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Current ISA Business Models

Business Model	Chips?	Architecture License	Commercial Core IP	Add Own Instructions	Open-Source Core IP
Microprocessor	Yes, ***two*** vendors	***No***	Yes, ***one*** vendor	***No***	***No***
Proprietary ISA	Yes, ***many*** vendors	Yes, ***expensive and restricted***	Yes, ***one*** vendor	***No***, *(Mostly)*	***No***
RISC-V Open standard ISA	Yes, ***many*** vendors	Yes, ISA is an ***open standard***	Yes, ***many*** vendors	***Yes***	***Yes, many available***

RISC-V enables design freedom

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Accelerated shared investment in RISC-V

- Numerous roadmaps declared across community incl SiFive, MIPS, Alibaba,….
- $1B investment by Intel.
- Billions in government investment around the world
- >$2B in reported Venture Capital investment in start-ups
- $ Billions more in collective RISC-V community investment

intel

Intel Creates $1B Innovation Fund To Grow RISC-V Market (And Attract New Foundry Customers) … Joins RISC-V Board

February 7, 2022

European Commission

EU announced a new European Chips Act of €15 billion
This adds to €30 billion of current public investments

February 8 2022

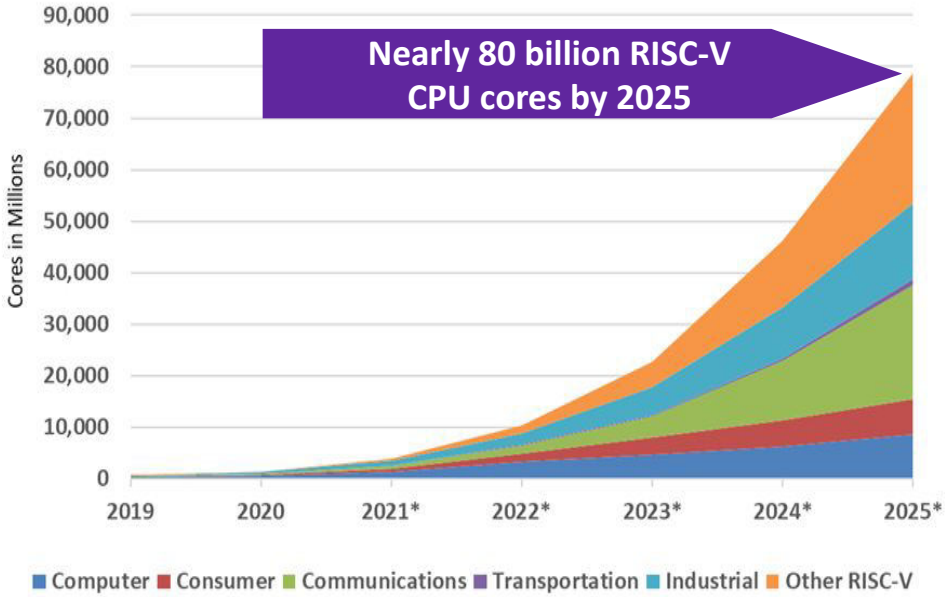
MeitY
Government of India

India Ministry for Electronics & Information Technology launched Digital India RISC-V (DIR-V) program for commercial SHAKTI & VEGA silicon.

April 27, 2022

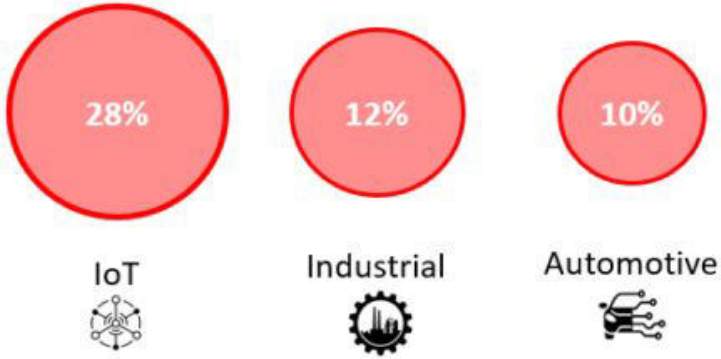
RISC-V®

RISC-V CPU core market grows 114.9% CAGR, capturing >14% of all CPU cores by 2025



Source: Semico Research Corp, March 2021

RISC-V Penetration Rate by 2025



"The rise of RISC-V cannot be ignored… RISC-V will shake up the $8.6 Billion semiconductor IP market."

-- William Li, Counterpoint Research

Source: Counterpoint Research, September 2021

"Deloitte Global predicts that

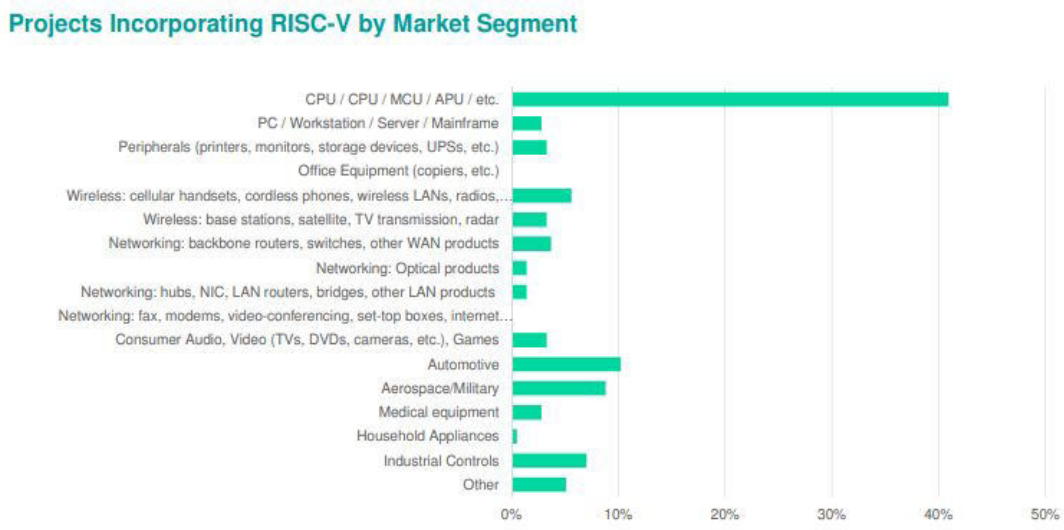
the market for RISC-V processing cores will double in 2022 from what it was in 2021, and that it will double again in 2023,

as the served addressable market available for RISC-V processing cores continues to expand."

December 2021

RISC-V®

Nearly a quarter of designs already incorporate RISC-V



Source: Tech Design Forum, November 2020

23% of ASIC and FPGA projects incorporated RISC-V in at least one processor in a 2020 study.

RISC-V enables the best processors

RISC-V

RISC-V enables profound innovation from low end to high end applications

Inherent and sustainable performance and efficiency advantage, Extensions designed simply, for easy implementation. Modular build from a clean base ISA does not carry legacy baggage.

Design flexibility and freedom afford increased innovation potential across multiple variables.

Supported by massive community, including major EDA tools as well as optimizing hardware and software co-design to provide most efficient designs scalable to the full spectrum of applications.

Disruptive **Technology**

Barriers	Proprietary	RISC-V
Standard	Controlled by single entity Limited innovation	**Open Hardware + Software Standard** driven by hardware and software community
Complexity	1500+ base instructions Incremental ISA	**Modular + Scalable** 47 base instructions, No legacy complexity
Design freedom	Complex and limited, deep investment	**Innovation and Design freedom** Extensible design on frozen base, collective investment

Opportunity	Proprietary	RISC-V
Diversity of solutions	Single vendor controlled	**Massive choice** Competition brings best solutions
Collective Investment	All Software work benefits single vendor	**Shared Investment** Software investment benefits all
Competition	Vendor lock in, forced to accept next gen solution	**Domain Specific** Targeted solution for each market

Unconstrained **Opportunity**

RISC-V®

Inherent and sustainable performance and efficiency advantage

- Extensions designed simply, for easy implementation.
- Clean base ISA does not carry legacy baggage.
- Modular design allows implementers to include only appropriate extensions for their solution.
- Reserved encoding space for alternative extensions without disrupting the base ISA / requiring a new ISA

Open interfaces are accepted practice

Field	Proprietary predecessor	Open Standard	Open Implementation	Commercial implementation on open standard
Networking	Now obsolete	Ethernet, TCP/IP	Many	Cisco, Juniper
OS	Windows	Posix	Linux, FreeBSD	Red Hat, Canonical, Suse, AIX, Zephyr
Compilers	Intel icc, ARMcc, Xcode	C	gcc, LLVM	Greenhills, IAR
Databases	Oracle 12C, DB2	SQL	MySQL, PostgresSQL	Oracle, SQLServer, DB2
Graphics	DirectX	OpenGL	Mesa3D	NVIDIA, AMD, Intel
ISA	x86, ARM, IBM360	**RISC-V**	LowRISC, other community led	Numerous RISC-V implementations

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Successful open standards, enabling multiple implementations

RISC-V Innovation Roadmap

Test Chips
Software tests
Linux port

Proof of Concept SoCs
Minion processors for power management & communications
Bare metal software

IoT SoCs
Microcontrollers
RTOS, Firmware
Development tools
Technical Steering Committee,
HPC SIG, GlobalPlatform partnership

AI SoCs, Application processors, Linux Drivers, AI Compilers

SIGS: Security Response, AI, Graphics, Android, Embedded, Datacenter/Cloud, Blockchain, Simulators, Managed Runtimes, Android, Functional Safety

Programs: Dev Board Seed, Development Partners, RISC-V Labs

SIGS: Vector, Perf Modeling, Perf Analysis, Trusted Computing, Control Flow Integrity, Memory Protection, Microarchitecture Side Channel, QOS, E2E Data Integrity, Error Handling, Automotive, Communications, Floating Point, Vector

Security specs; RISC-V Security Model, AP-TEE, IOPMP

Platform specs: Platforms, SEE, SBI, ABI, Discovery,Watchdog, ACPI, UEFI

SOC specs: E-Trace, Nexus, IOMMU

Ecosystem

2010-2016	2018	2019	2020	2021	2022	2023 →
ISA Definition RISC-V Foundation	RV32	RV32I and RV64I Base instructions: Integer, float,double, quad, atomic, and compressed instructions Priv modes, Interrupts, exceptions, memory model, protection, and virtual memory	Architecture Compatibility Framework Trace	Vector Crypto Scalar Bitmanip Hypervisor ePMP Cache Mgt Virtual Memory Zfh Zfinx Zihintpause	Profiles Packed SIMD Advanced Interrupts Java: ptr masking, I/D synch RV32E & RV64E Bfloat16 Vector Half-Precision Floating Point Code Size Crypto Vector Fast Interrupts SMPU Zmmul Ztso Zihintntl	Matrix Ops Crypto Gost

ISA Extensions

In performance benchmarks, RISC-V is gaining ground really fast

- Researchers Benchmark Experimental RISC-V Supercomputer
- XuanTie C906 Tops MLPerf Tiny v0.7 Benchmark
- MIPS Claims "Best-In-Class Performance" With New RISC-V eVocore CPUs
- Andes Technology RISC-V Processors Reveal Outstanding Performance and Efficiency in MLPerf Tiny
- RISC-V Powered Mango Pi Takes on Raspberry Pi Zero at Its Own Game
- SiFive RISC-V Sees Some Performance Improvements On Ubuntu 22.04
- Greenwaves top results in MLPerf Tiny for hardware acceleration

Processors in development slated to overtake current proprietary alternatives.

RISC-V is rapidly building the strongest ecosystem

RISC-V instrumented with software top of mind

- **Open standards enable software** choice. Applications keen to run on RISC-V.
- **Toolchain and OS support** required for Extension ratification
- **Single hypervisor standard** to simplify and unify application support
- **Thousands of software developers** bringing workloads to RISC-V
- **Strategic imperative and investment** by commercial sector and geographies
- **Modern design approaches** leveraged for fewer instructions

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Powerful forces fuel a unified RISC-V approach

Users: No one wants a repeat of vendor lock-in, avoid fragmentation of legacy ISAs.

Software: No one, not even a nation, can afford their own software stack. Upstream open-source projects generally only accept frozen/ratified RISC-V standards.

Fragmented Alternatives: Other architectures that enable an architecture license then do not have consistency on those implementations. In addition, there are multiple ISAs from other architectures such as A ISA, M ISA, as well as numerous versions.

- Trust zone and secure boot operate differently on different payment processing systems (credit card, Samsung/Google/Apple pay) for example depending on the manufacturer rather than a uniform approach.
- In IoT, the platform security architecture defines certification mechanisms that are implemented by third parties. Paypal is an example where the security mechanism moved to the cloud rather than the device.

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Fragmentation: Same thing done different ways

Managing Diversity for RISC-V

Raw extensions

- Base + standard extensions + custom extensions
- Full suite of options available for experimentation and specialized uses
- Massive combinatorial space of options

ISA Profiles

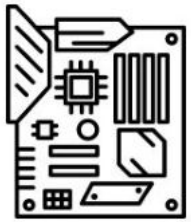
- Packages of ISA extensions for given domain
- Initial set: RVI20 (basic), RVA20/22/23 (application processor)
- Factor out common ISA combinations for use in platform standards

Platform standards

- Hardware/software standards for platforms (much more than just ISA)
- Initial focus OS-A platform for Unix-like OS (includes IOMMU, AIA, etc)

Diversity: Solving different problems

RISC-V Technical Programs



RISC-V Developer Boards
Available to spur innovation, provide hands-on education, and engage early adopters to test and develop.

RISC-V Development Partner
Recognizes the investment and dedication of organizations making significant technical contributions to RISC-V.

RISC-V Lab
Institutions that host a lab with RISC-V hardware for CI/testing and general availability sandboxing.

RISC-V Compatible
Architectural Tests created to help ensure that software written will run on implementations that comply with that profile. Branding available for compatibility.

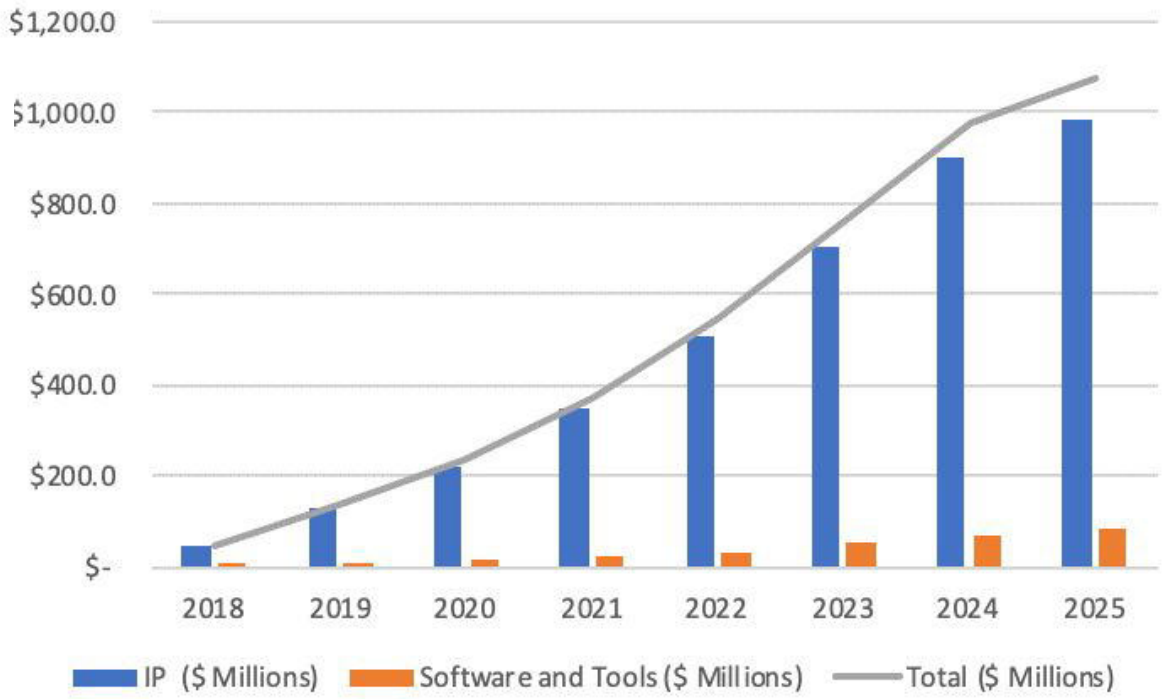
RISC-V Platform
A common, reusable runtime environment that operating systems and applications can target to improve portability and reuse. Provides interoperability assurance.

RISC-V Profiles
Refers to a base ISA and one or more extensions that are specified as a group so that applications can be compiled once, run on different implementations, and get the same results.

https://wiki.riscv.org/display/TECH

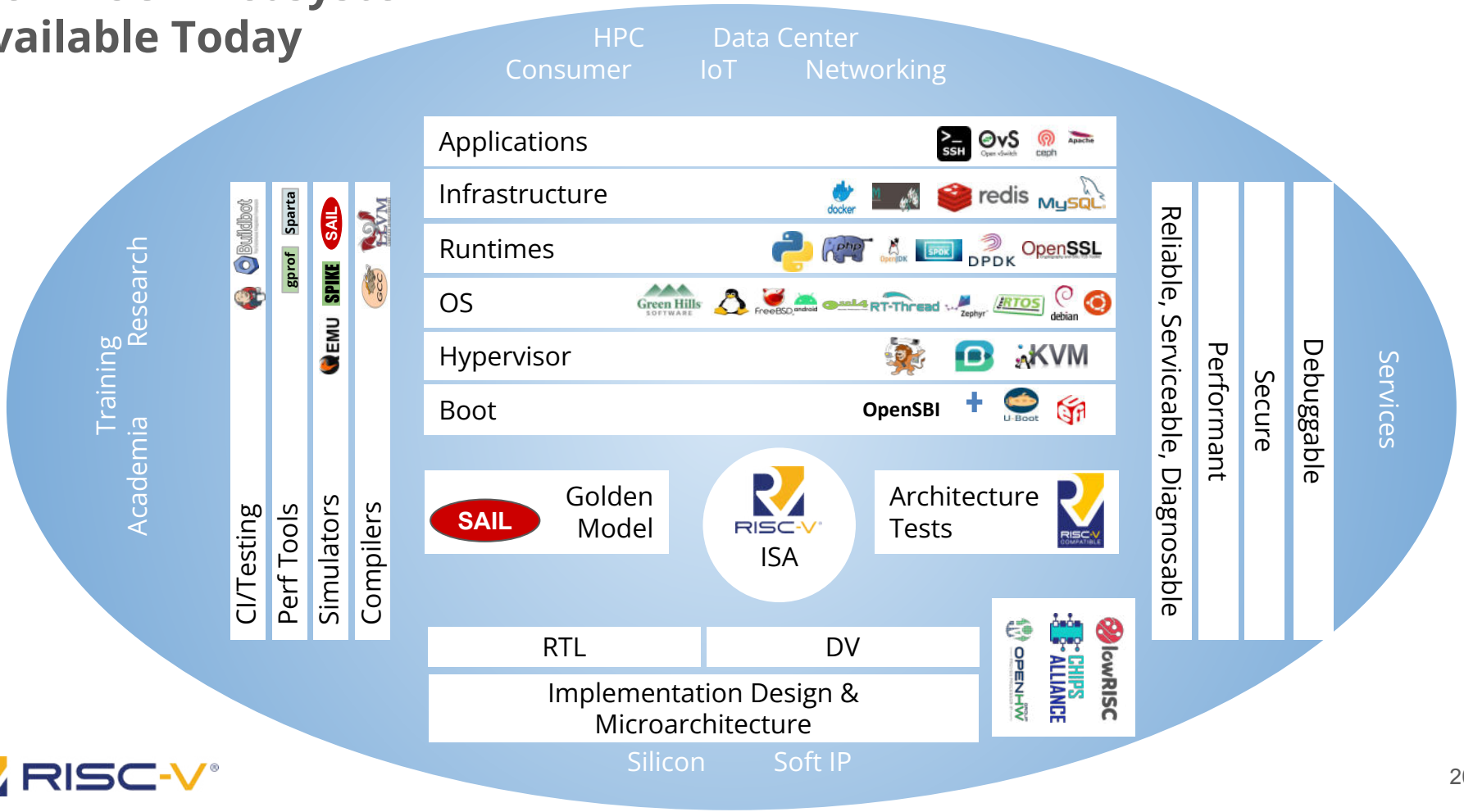
RISC-V IP, SW, and Tools build momentum

The total market for RISC-V IP and Software is expected to grow to $1.07 billion by 2025 at a CAGR of 54.1%



Source: Tractica, December 2019

Rich RISC-V Ecosystem Available Today



Investment and traction accelerate in 2022

PULP Platform HEROv2: Full-Stack Open-Source Research FPGA Platform for Heterogeneous Computing

HEROv2 for heterogeneous computing based on clusters of 32-bit RISC-V cores and an application-class 64-bit ARMv8 or RV64 host processor for sharing data between 64-bit hosts and 32-bit accelerators.

January 16, 2022

intel

Intel Corporation Makes Deep Investment in RISC-V Community to Accelerate Innovation in Open Computing

RISC-V welcomes Intel to the Board of Directors to collaborate on RISC-V IP and contribute to RISC-V software development

Intel Creates $1B Innovation Fund To Grow RISC-V Market (And Attract New Foundry Customers)

February 7, 2022

imperas NSI-TEXE

Automotive RISC-V processor functional design verification

NSITEXE selected ImperasDV for RISC-V design verification, expanding Imperas' simulation technology, models, verification IP and tools by NSITEXE for next gen 64bit RISC-V vector accelerators in AI automotive with verification for level needed to attain ISO 26262 ASIL D.

January 6, 2022

European Commission

The European Commission announced a new European Chips Act of €15 billion in additional public and private investments until 2030. This adds to €30 billion of public investments previously earmarked.

February 8 2022

intel

Intel to spend €17bn on chip mega-factory in Germany… expands manufacturing in Ireland, plus R&D and packaging across Europe

March 15, 2022

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Hot off the press 2022!

Clockwork Pi announced availability of DevTerm R-01, the first 64-bit RISC-V portable computer with retro styling and modern computing power.

March 15, 2022

MeitY
Government of India

The government of India Ministry for Electronics & Information Technology launched Digital India RISC-V (DIR-V) program with aggressive milestones for commercial silicon of SHAKTI & VEGA.

April 27, 2022

MIPS

MIPS Pivots to RISC-V with Best-In-Class Performance and Scalability

eVocore P8700 high performance for deep pipeline with multi-issue Out-of-Order (OOO) execution and multi-threading. Scales to 64 clusters, 512 cores and 1,024 harts/threads. Available in Q4 2022.

eVocore I8500 – power efficiency: in-order multiprocessing with best-in-class power efficiency for SoC applications.

May 10, 2022

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Momentum headlines in 2022

Spain Approves €12.25b Semiconductor Investment Plan
President Sanchez met CEOs of MicronTech Intel & Qualcomm at WEF22 on Spain's €12 billion strategy in global semiconductor industry with RISC-V lab at BSC, and Investment in Spain

May 25, 2022

Università di Bologna, CINECA and E4 "Monte Cimone" Cluster, a RISC-V platform using SiFive RISC-V SoCs demonstrated remarkable software and hardware readiness and maturity - first gen RISC-V HPC machines coming soon. June 11, 2022

Microchip RISC-V based PolarFire FPGAs enter mass production: Microchip is writing a new chapter in the history of RISC-V with the availability of production-qualified SoC PolarFire devices.
June 8, 2022

Esperanto TECHNOLOGIES

Accelerating ML Recommendation With Over 1,000 RISC-V/Tensor Processors on Esperanto's ET-SoC-1 Chip June 17, 2022

Alibaba Cloud

XuanTie C906 Tops MLPerf Tiny v0.7 Benchmark
June 13, 2022

antmicro

Antmicro Renode 1.13 for improved machine learning and pre-silicon development
June 17, 2022

Imagination

Imagination Technologies announces RTXM-2200 real-time embedded RISC-V CPU, a highly scalable 32-bit embedded solution with a flexible design for networking solutions, packet management, storage controllers, and sensor management for AI cameras and smart metering. June 21, 2022

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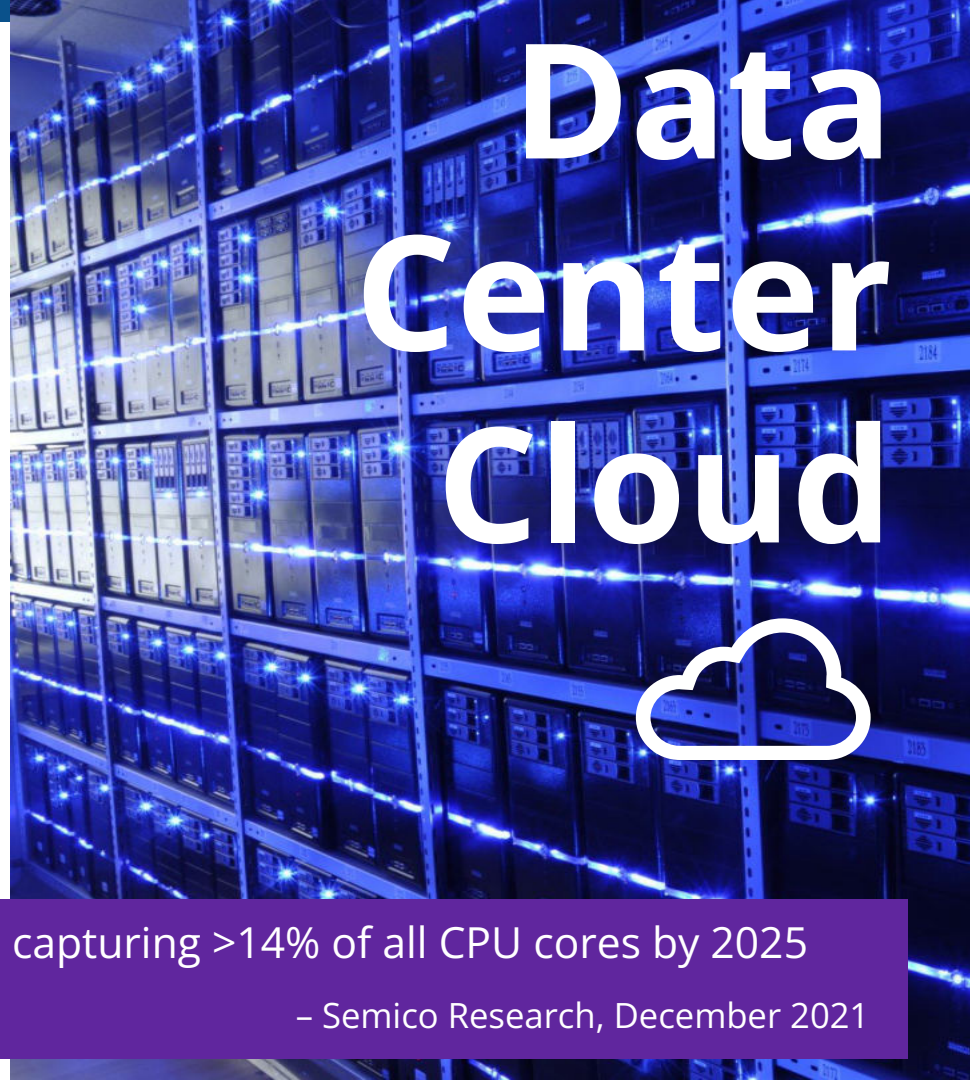
Data Center Cloud



- **Esperanto** 1,000-Core RISC-V AI accelerator.
- **Alibaba** RISC-V Xuantie processors with 4 open cloud and edge processors
- **Imagination** RISC-V CPU family, for discrete and heterogeneous computing
- **Seagate** hard disk drive controller with high-performance RISC-V CPU.
- **Ventana** performance chiplet approach to data center SoC design
- **Intel** Nios processor based on RISC-V, designed for performance.

RISC-V CPU core market will grow 115% CAGR, capturing >14% of all CPU cores by 2025

– Semico Research, December 2021

Communication AI SoC RISC-V designs will grow 21.2% CAGR from 2019-27
– Semico Research, December 2021

Telecom & Communications

- **Andes** RISC-V processor adopted by SK Telecom for AI products.
- **Alibaba** supporting Android 12 on their 64-bit RISC-V core emulated in QEMU
- **Sipeed** RISC-V chip runs Android 10, RV64 phone coming next
- **Alibaba** ported TensorFlow Lite for AI image, audio, and optical in smart devices.
- **Google** Pixel 6 Titan M2 RISC-V processor, with extra speed and memory, more resilient to advanced attacks.

Consumer, IoT devices

- **Huawei** Hi3861 RISC-V board for Harmony OS developers for IoT
- **Zepp Health** / Huami wearable manufacturer OS supporting RISC-V Reference Models for RISC-V P extension
- **GreenWaves** ultra-low power GAP9 hearables platform for scene-aware and neural network-based noise reduction.
- **RIOS Lab** announced PicoRio, an affordable RISC-V small-board computer.
- **SiFive** world's fastest development board for RISC-V Personal Computers.

RISC-V will command 28% of the IoT market by 2025

– Counterpoint Technology Market Research, September 2021

RISC-V-based AI SoCs will grow **73.6% CAGR to 25B units and $291B in revenue by 2027** – Semico Research, December 2021

- **Alibaba Cloud** tops MLPerf Tiny v0.7 Benchmark with its IOT processor
- **Esperanto** accelerating ML Recommendation With Over 1,000 RISC-V/Tensor Processors on ET-SoC-1 Chip
- **StarFive** released the world's first RISC-V AI visual processing platform
- **Andes** released superscalar multicore and L2 cache controller processors.
- **NVIDIA CUDA** support on Vortex RISC-V GPGPU enables scaling from 1-core to 32-core GPU based on RV32IMF ISA

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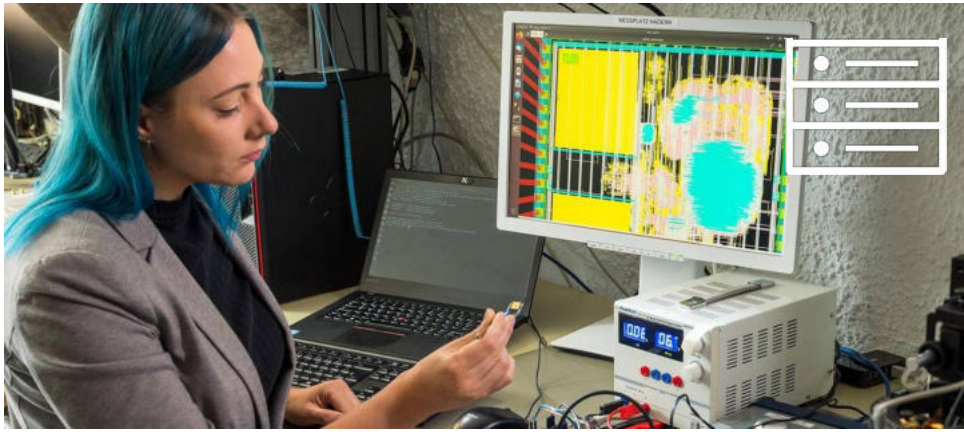
Edge Computing

- **Fraunhofer** ported Tensorflow lite to their RISC-V processor core for Edge AI applications incl sensor data evaluation, gesture control, or vibration analysis.
- **Seeed Studio**'s new Sipeed MAIX, a RISC-V 64 AI board for Edge Computing makes it possible to embed AI to any IoT device.
- **Micro Magic** announced an incredibly fast 64-bit RISC-V core achieving 5GHz and 13,000 CoreMarks at 1.1V.
- **Western Digital** SweRV Core enables spectrum of compute at the edge
- **Microchip** released the first SoC FPGA development kit based on the RISC-V ISA.

High Performance Computing

- **E4** Monte Cimone Cluster along with DEI-UNIBO contributing to architecture, software, and integration.
- **European Processor Initiative** RISC-V accelerator with first chip Sep 2021
- **Technical University of Munich** (TUM) quantum cryptography chip for quantum computing security demands
- **Tactical Computing Labs** HPC-centric software test suite for GCC and LLVM
- **Cortus** is developing a high-performance RISC-V Out-of-Order processor core for the European eProcessor project.
- **De-RISC** HW-SW platform for multi-core RISC-V SoC for safety critical aerospace



Johanna Baehr of TUM heads a team that has hidden four hardware Trojans on this chip - malicious functions that are integrated directly into the circuits.

Image: Astrid Eckert / TUM

RISC-V®

RISC-V will capture 10% of the Automotive market by 2025

– Counterpoint, September 2021

SiFive high-end applications and real-time processors for leading performance, with lowest area and power consumption in vehicles for safety, security, and performance

Andes launched safety-enhanced 32bit RISC-V CPU IP, first to be fully compliant with ISO 26262 functional safety.

IAR RISC-V Embedded Workbench for **SiFive** infotainment, connectivity, and ADAS products.

2020 RISC-V automotive opportunity 4M cores; growing to 150M cores in 2022 and 2.9B cores by 2025.

– Deloitte, December 2021

RISC-V Automotive Value Multicore SoC revenue to be $5.7B in 2022. Advanced RISC-V AI SoCs for High-End Passenger Cars to Reach $819M by 2027

- Semico Research, June 2022

MobileEye EyeQ Ultra vision advanced driver assist systems chips for 176 trillion ops per second with 12 RISC-V CPU cores.

Andes ISO 26262 Functional Safety ASIL D Dev Process Certification for RISC-V embedded safety with Andes processors

Renesas and SiFive partner on next-gen, high-end RISC-V automotive applications. SiFive licenses RISC-V core IP to Renesas.

Imagination Technologies GPU linked by a RISC-V core for ASIL-B level designs with ISO 26262 safety critical certification.

Green Hills support RISC-V RTOS targeting ISO-26262 ASIL D applications

Automotive

MIPS RISC-V eVocore processors for high-performance, real-time compute in datacenter and automotive

Fraunhofer RISC-V Processor cores for functional safety and cyber security, and engaging in GaNext program.

IAR Systems functional safety of Embedded Workbench sw tool chain for **NSI-TEXE** RISC-V core.

NSI-TEXE 64bit RISC-V vector accelerators with **ImperasDV** design verification for automotive AI with ISO 26262 ASIL D.

Europe GaNext power converters with GaN power processors with better efficiency and compactness for EV chargers.

Kneron RISC-V based AI edge chip for Automotive

Dedicated Community

Services Fab, design services

Chips SoC, IP, FPGA

I/O Memory, network, storage

Universities and Research

Software Dev tools, firmware, OS

Industries edge/IoT, automotive, HPC/data center, embedded, AI/ML

Press and Analysts

Investors and Funding sources

Individual Advocates

RISC-V collaboration in Japan

Japan RISC-V Members

Cyber Physical Security Research Center of AIST

DTS INSIGHT Corporation

Hitachi, Ltd.

NSITEXE

OTSL, Inc

PEZY Computing, K.K.

Renesas Electronics Corporation

Software Hardware & Consulting

Sony Semiconductor Solutions Corporation

The University of Electro-Communications

The University of Tokyo

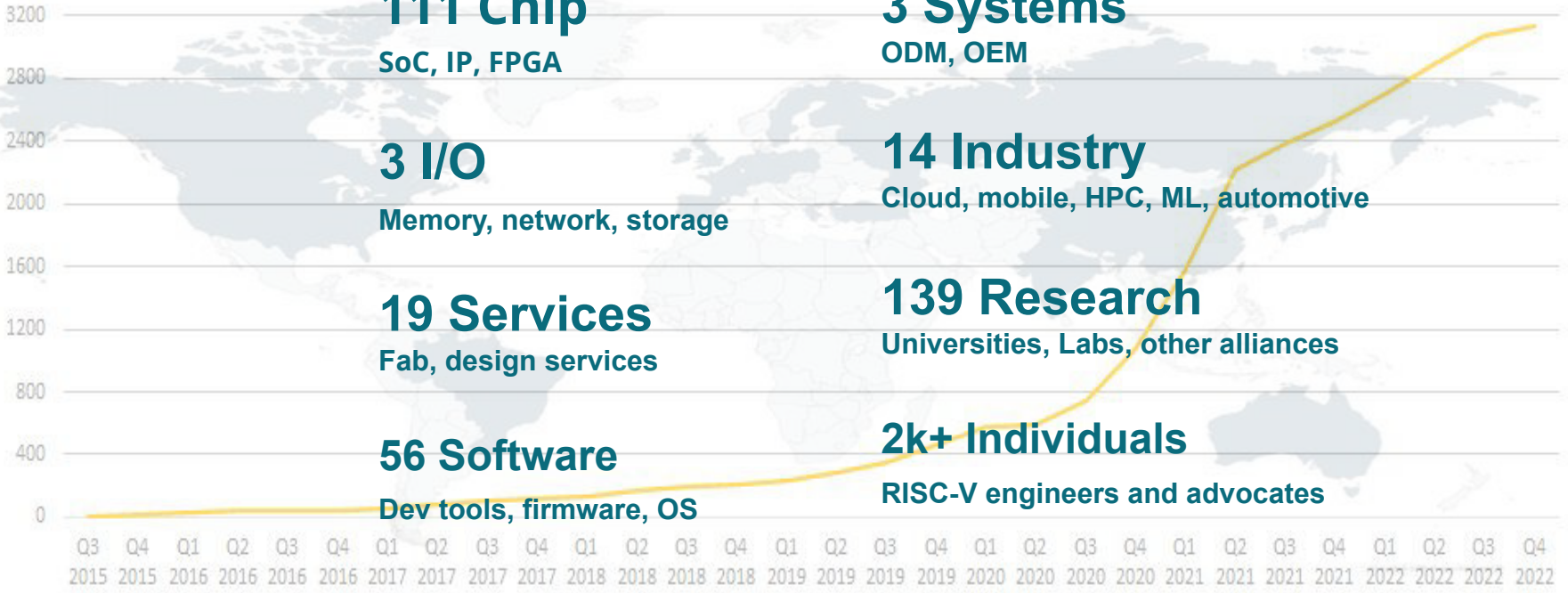
UNO Laboratories, Ltd.

"RISC-V continues to gain momentum around the world, and we plan to leverage SiFive's portfolio of automotive RISC-V products in our future automotive SoC solutions to meet the exacting demands of these global customers."

– Takeshi Kataoka, Senior VP and GM of Automotive Solution Business Unit at **Renesas**

More than 3,100 RISC-V Members

across 70 Countries



111 Chip
SoC, IP, FPGA

3 I/O
Memory, network, storage

19 Services
Fab, design services

56 Software
Dev tools, firmware, OS

3 Systems
ODM, OEM

14 Industry
Cloud, mobile, HPC, ML, automotive

139 Research
Universities, Labs, other alliances

2k+ Individuals
RISC-V engineers and advocates

Oct 2022

RISC-V®

RISC-V membership rapid growth of 134% in 2021

Technical Deliverables

Technical **governance**
Build **technical deliverables**
Guide strategic technical **Work groups**

Compatibility & Verification

Profiles & Platforms & Architecture Compatibility Tests (ACT) & Platform Compatibility Tests (PCT)

Marketing

Create brand value around RISC-V
Amplify member news, content, and success with press & analysts
Original content programs
RISC-V, industry, and regional **Events**

Learning & Talent

Multi-level **online learning**
Connecting **universities** with labs, tests, and curricula
RISC-V **Training Partners**
Jobs and internships

Advocacy + Alliances

RISC-V **Ambassadors**
Geo and industry **alliances**
Local developer groups and events

RISC-V Exchange

Online directory of providers, products,services, and learning resources
Technical **developer forums**

RISC-V delivers incredible member support

RISC-V®

Benefits of engaging in RISC-V

- ✔ **Accelerate technical traction** and insight
- ✔ **Contribute** technical priorities, approaches, and code
- ✔ Gain strategic and **technical advantage**
- ✔ **Increase visibility**, leadership, and market insight
- ✔ Fill and increase **engineering skills**, retain and attract talent
- ✔ Build **innovation partner** network and customer pipeline
- ✔ **Deepen, engage, and lead** in local and industry developer network
- ✔ **Showcase RISC-V products**, services, training, and resources

RISC-V®

RISC-V is a community of passionate, dedicated, and invested stakeholders

As individuals
As companies
As universities
As public institutions and non-profits
As nations

As one Global, connected movement

Build RISC-V into your company strategy, and your personal mission

www.riscv.org

@risc_v
@calista_redmond

WeChat

risc-v-international
calistaredmond

Thank You

Scan for Calista Contact info

RISC-V®

Membership Options

RISC-V Membership details may be found online here

Premier Member Benefits

- Board seat and Technical Steering Committee seat included at $250k level
- Technical Steering Committee seat included at $100k level
- Board level includes seat on RISC-V Legal Committee
- Eligible to lead workgroup and/or committee

- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Premier members
- Solution / Product listing highlighted on RISC-V Exchange, noted with member level
- 4 case studies a year
- 2 blogs per month
- 2 social media spotlights per month
- Spotlight member profile
- Event sponsorship discount

Strategic Member Benefits

- 3 Board reps elected for the Strategic tier, including Premier members that do not otherwise have a board seat
- Eligible to lead workgroup and/or committee

- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Strategic members
- Solution / Product listing highlighted on the RISC-V Exchange, noted with member level
- 1 case study a year
- 1 blog per month
- 1 social media spotlight per month
- Event sponsorship discount

Community Member Benefits

- Two Board representatives
- 1 Community Board representative, elected
- 1 Individual Board representative, elected

- Member logo / name listing on RISC-V website, by member level
- 1 case study a year
- 1 blog per quarter
- 1 social media spotlight per quarter
- Event sponsorship discount

Premier Requirements

- Membership open to any type of legal entity
- $250k Annual membership fee that includes Board seat and TSC seat
- $100k Annual membership fee that includes TSC seat

Strategic Member Requirements

- Membership open to any type of legal entity
- Annual membership fee based on employee size
  - 5,000+ employees: $35k
  - 500-5,000 employees: $15k
  - <500 employees: $5k
  - <10 employees & company <2 yrs old: $2k

Community Requirements

- Membership open to
  - academic institutions,
  - non-profits,
  - individuals not representing a legal entity
- No annual membership fee

RISC-V®

RISC-V Learn

Learning RISC-V is a challenging, highly rewarding activity. There are many resources available to help you on this technical journey, and we welcome new additions to these resources – please contact us at info@riscv.org with any questions or comments.

Learn Online

Online learning at beginner, intermediate, and advanced levels to increase engineering expertise and career opportunity on RISC-V across the industry.

Training Partners

Provide RISC-V training in a professional setting to extend the breadth and reach of RISC-V knowledge

University Resources

Universities that support RISC-V curriculum and other programing as well as books and other learning resources.

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Profiles and Platforms

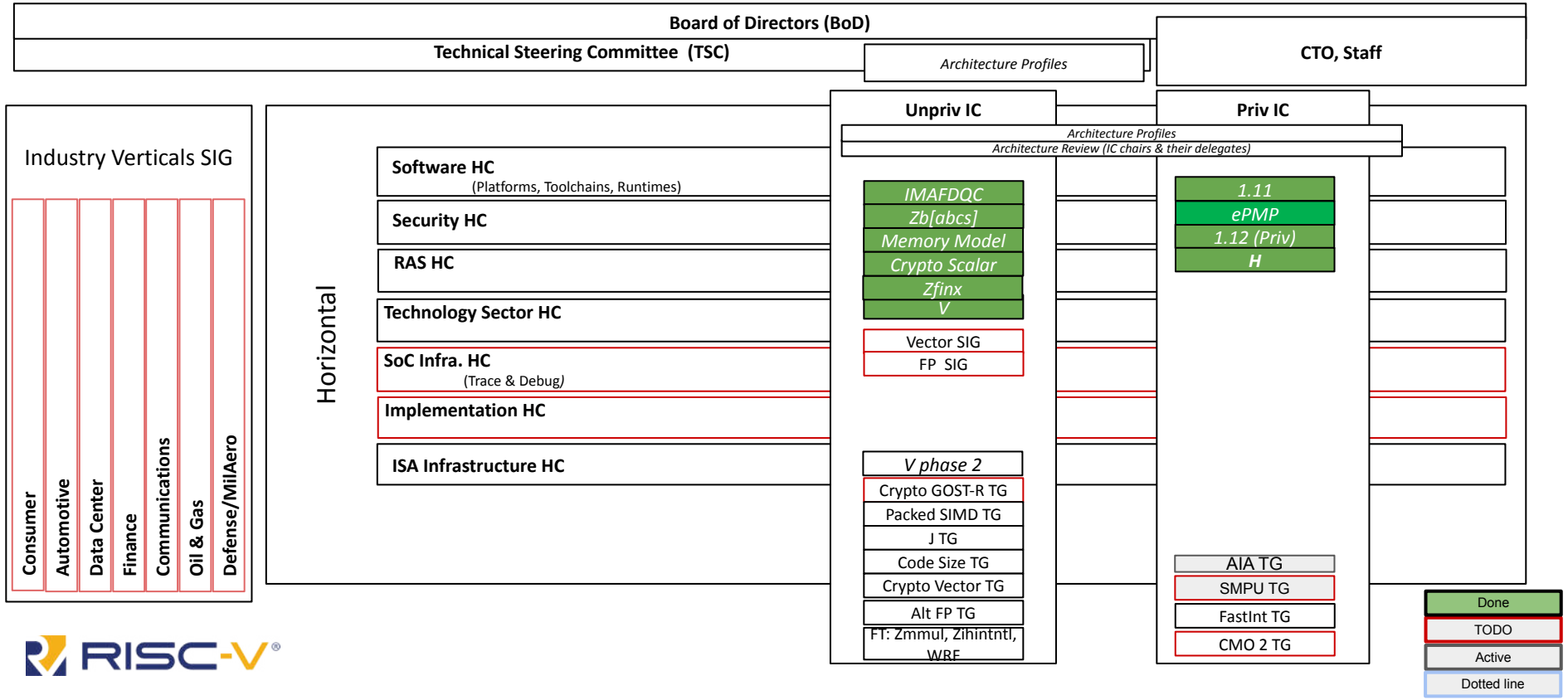
ISA Profiles

- A set of **extensions** that are compatible
- **Extension types**: required, optional, unsupported, or incompatible
- **Two profile types:**
  - **Application (RVA[yy]):** Linux-class and other embedded designs with more sophisticated ISA needs
  - **Microcontroller (RVM[yy]):** Cost-sensitive application-optimized embedded designs running bare-metal or simple RTOS environments
- Running the same sequence of instruction between implementations are **RISC-V compatible**

System Platforms

- A set of **features** that are compatible
- Includes **ISA Profiles**, software and hardware **system components**, standardized **hardware/software interfaces**, etc
- **Two Platform types**: OS/A and M (naming TBD)
- Ability to move an executable from one implementation to another and get the same results are **RISC-V Compatible**

Technical Organization



Software Horizontal Committee

AI/ML/NLP/Graphics SIG

Android SIG

Perf Modeling SIG

Perf Analysis SIG

IOMMU TG

Platform HSC

(includes platform specs)

Config TG

Hypervisors SIG

AIA TG

IOPMP TG

OS-A Platform SIG

RVM-CSI Platform TG

OS-A SEE TG

OS-A PlatformTG

OS-A PCT TG

Topics TODO:

- Linux class OSs
- RTOSs
- DMA
- Multi-processing
- JITs
- IOMMU, Buses
- Bootloaders
- Distro coordination/build/rel
- QOS
- Perf monitoring

TGs for specs underway

Toolchain & Runtimes HSC

psABI TG

Topics TODO:

- Benchmarks
- Regression test strategy
- Ecosystem changes
- Extensions needed
- Worst Case Execution Time (WCET)
- Spatial & Timing interference
- DSP
- DB & Hadoop et al
- Performance analysis
- Native code
  - GCC
  - LLVM
  - Optimizer
  - Profiler
  - gdb

Code Size TG

HPC SIG

Managed Runtimes SIG

Done

TODO

Active

Dotted line

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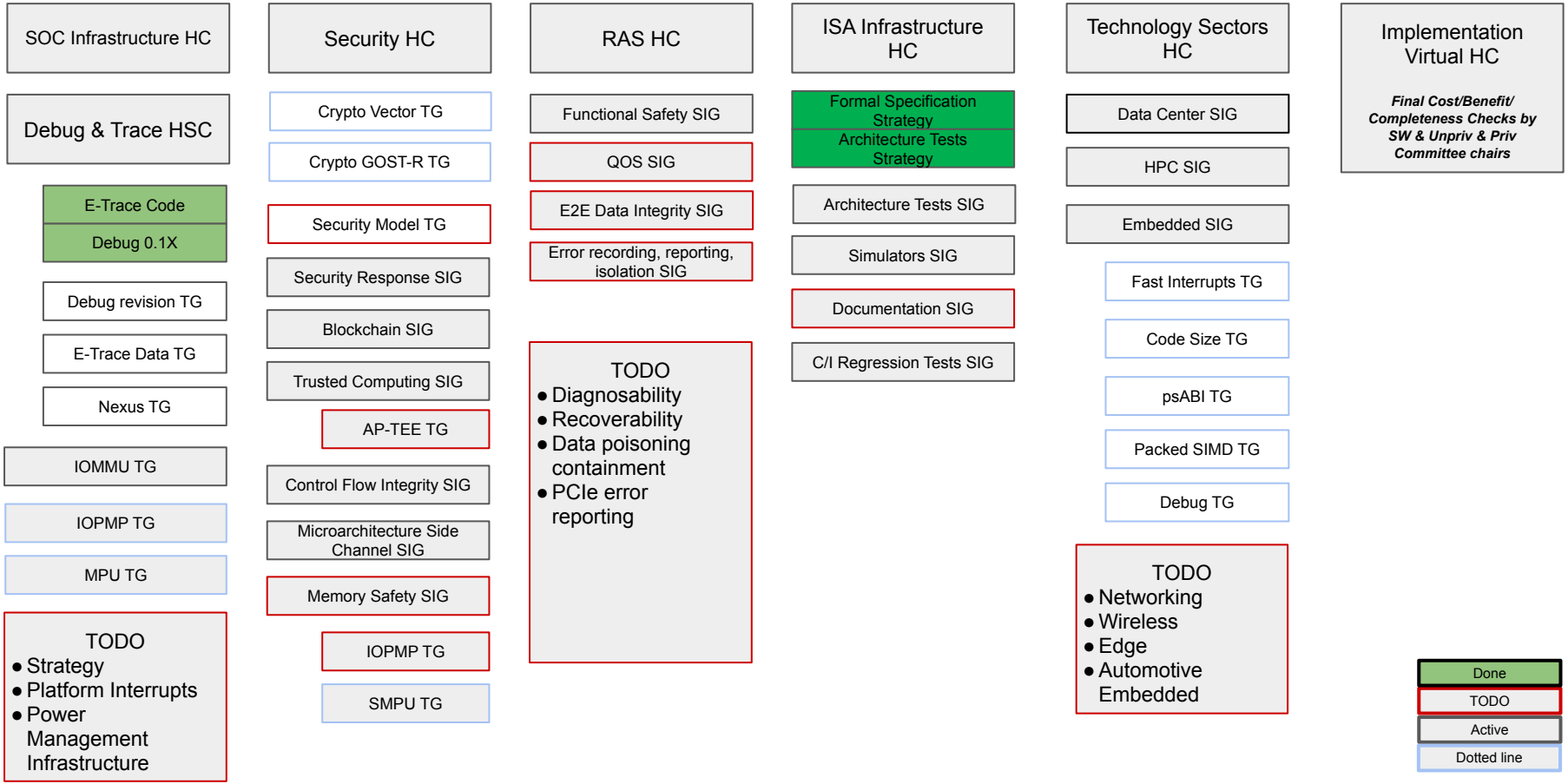
SOC Infrastructure HC
Debug & Trace HSC
E-Trace Code
Debug 0.1X
Debug revision TG
E-Trace Data TG
Nexus TG
IOMMU TG
IOPMP TG
MPU TG
TODO
• Strategy
• Platform Interrupts
• Power Management Infrastructure
Security HC
Crypto Vector TG
Crypto GOST-R TG
Security Model TG
Security Response SIG
Blockchain SIG
Trusted Computing SIG
AP-TEE TG
Control Flow Integrity SIG
Microarchitecture Side Channel SIG
Memory Safety SIG
IOPMP TG
SMPU TG
RAS HC
Functional Safety SIG
QOS SIG
E2E Data Integrity SIG
Error recording, reporting, isolation SIG
TODO
• Diagnosability
• Recoverability
• Data poisoning containment
• PCIe error reporting
ISA Infrastructure HC
Formal Specification Strategy
Architecture Tests Strategy
Architecture Tests SIG
Simulators SIG
Documentation SIG
C/I Regression Tests SIG
Technology Sectors HC
Data Center SIG
HPC SIG
Embedded SIG
Fast Interrupts TG
Code Size TG
psABI TG
Packed SIMD TG
Debug TG
TODO
• Networking
• Wireless
• Edge
• Automotive Embedded
Implementation Virtual HC
Final Cost/Benefit/ Completeness Checks by SW & Unpriv & Priv Committee chairs
Done
TODO
Active
Dotted line