Calista Redmond
CEO, RISC-V International

November 2022
Open standards and collaboration are strategic to hardware and software across industries and geographies.
The definition of open computing is RISC-V

RISC-V is the most prolific and open Instruction Set Architecture in history

- RISC-V is inevitable
- RISC-V enables the best processors
- RISC-V is rapidly building the strongest ecosystem
RISC-V is inevitable

RISC-V Mission:
RISC-V is the industry standard ISA across computing

>10 Billion RISC-V cores already shipped.

- Innovation and adoption moving rapidly across all domains
- Demand at every performance level (low to ludicrous)
- Shared investment is driving the fastest growing ecosystem

Leverage a community ISA spec development model
# Current ISA Business Models

<table>
<thead>
<tr>
<th>Business Model</th>
<th>Chips?</th>
<th>Architecture License</th>
<th>Commercial Core IP</th>
<th>Add Own Instructions</th>
<th>Open-Source Core IP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microprocessor</td>
<td>Yes, two vendors</td>
<td>No</td>
<td>Yes, one vendor</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Proprietary ISA</td>
<td>Yes, many vendors</td>
<td>Yes, expensive and restricted</td>
<td>Yes, one vendor</td>
<td>No, (Mostly)</td>
<td>No</td>
</tr>
<tr>
<td>RISC-V Open standard ISA</td>
<td>Yes, many vendors</td>
<td>Yes, ISA is an open standard</td>
<td>Yes, many vendors</td>
<td>Yes</td>
<td>Yes, many available</td>
</tr>
</tbody>
</table>

RISC-V enables design freedom
Accelerated shared investment in RISC-V

- Numerous roadmaps declared across community incl SiFive, MIPS, Alibaba,....
- $1B investment by Intel.
- Billions in government investment around the world
- >$2B in reported Venture Capital investment in start-ups
- $ Billions more in collective RISC-V community investment

Intel Creates $1B Innovation Fund To Grow RISC-V Market (And Attract New Foundry Customers) … Joins RISC-V Board

February 7, 2022

EU announced a new European Chips Act of €15 billion
This adds to €30 billion of current public investments

February 8 2022

India Ministry for Electronics & Information Technology launched Digital India RISC-V (DIR-V) program for commercial SHAKTI & VEGA silicon.

April 27, 2022
RISC-V CPU core market grows 114.9% CAGR, capturing >14% of all CPU cores by 2025

Nearly 80 billion RISC-V CPU cores by 2025

“The rise of RISC-V cannot be ignored... RISC-V will shake up the $8.6 Billion semiconductor IP market.”

-- William Li, Counterpoint Research

Source: Semico Research Corp, March 2021

Source: Counterpoint Research, September 2021
Deloitte Global predicts that the market for RISC-V processing cores will double in 2022 from what it was in 2021, and that it will double again in 2023, as the served addressable market available for RISC-V processing cores continues to expand.

Nearly a quarter of designs already incorporate RISC-V.

23% of ASIC and FPGA projects incorporated RISC-V in at least one processor in a 2020 study.

Source: Tech Design Forum, November 2020
RISC-V enables profound innovation from low end to high end applications.

**Inherent and sustainable performance and efficiency advantage**, Extensions designed simply, for easy implementation. Modular build from a clean base ISA does not carry legacy baggage.

**Design flexibility and freedom** afford increased innovation potential across multiple variables.

**Supported by massive community**, including major EDA tools as well as optimizing hardware and software co-design to provide most efficient designs scalable to the full spectrum of applications.
### Disruptive Technology

<table>
<thead>
<tr>
<th>Barriers</th>
<th>Proprietary</th>
<th>RISC-V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>Controlled by single entity</td>
<td><strong>Open Hardware + Software Standard</strong></td>
</tr>
<tr>
<td></td>
<td>Limited innovation</td>
<td>driven by hardware and software community</td>
</tr>
<tr>
<td>Complexity</td>
<td>1500+ base instructions</td>
<td><strong>Modular + Scalable</strong></td>
</tr>
<tr>
<td></td>
<td>Incremental ISA</td>
<td>47 base instructions, No legacy complexity</td>
</tr>
<tr>
<td>Design freedom</td>
<td>Complex and limited, deep investment</td>
<td><strong>Innovation and Design freedom</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Extensible design on frozen base, collective investment</td>
</tr>
</tbody>
</table>

### Opportunity

<table>
<thead>
<tr>
<th>Proprietary</th>
<th>RISC-V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diversity of solutions</td>
<td><strong>Massive choice</strong></td>
</tr>
<tr>
<td></td>
<td>Competition brings best solutions</td>
</tr>
<tr>
<td>Collective Investment</td>
<td><strong>Shared Investment</strong></td>
</tr>
<tr>
<td></td>
<td>Software investment benefits all</td>
</tr>
<tr>
<td>Competition</td>
<td><strong>Domain Specific</strong></td>
</tr>
<tr>
<td></td>
<td>Targeted solution for each market</td>
</tr>
</tbody>
</table>

**Collective Investment**
- All Software work benefits single vendor

**Shared Investment**
- Software investment benefits all

**Domain Specific**
- Targeted solution for each market
Inherent and sustainable performance and efficiency advantage

● Extensions designed simply, for easy implementation.
● Clean base ISA does not carry legacy baggage.
● Modular design allows implementers to include only appropriate extensions for their solution.
● Reserved encoding space for alternative extensions without disrupting the base ISA / requiring a new ISA
Open interfaces are accepted practice

<table>
<thead>
<tr>
<th>Field</th>
<th>Proprietary predecessor</th>
<th>Open Standard</th>
<th>Open Implementation</th>
<th>Commercial implementation on open standard</th>
</tr>
</thead>
<tbody>
<tr>
<td>Networking</td>
<td>Now obsolete</td>
<td>Ethernet, TCP/IP</td>
<td>Many</td>
<td>Cisco, Juniper</td>
</tr>
<tr>
<td>OS</td>
<td>Windows</td>
<td>Posix</td>
<td>Linux, FreeBSD</td>
<td>Red Hat, Canonical, Suse, AIX, Zephyr</td>
</tr>
<tr>
<td>Compilers</td>
<td>Intel icc, ARMcc, Xcode</td>
<td>C</td>
<td>gcc, LLVM</td>
<td>Greenhills, IAR</td>
</tr>
<tr>
<td>Databases</td>
<td>Oracle 12C, DB2</td>
<td>SQL</td>
<td>MySQL, PostgreSQL</td>
<td>Oracle, SQLServer, DB2</td>
</tr>
<tr>
<td>Graphics</td>
<td>DirectX</td>
<td>OpenGL</td>
<td>Mesa3D</td>
<td>NVIDIA, AMD, Intel</td>
</tr>
<tr>
<td>ISA</td>
<td>x86, ARM, IBM360</td>
<td></td>
<td>RISC-V</td>
<td>LowRISC, other community led</td>
</tr>
</tbody>
</table>

Successful open standards, enabling multiple implementations.
## RISC-V Innovation Roadmap

<table>
<thead>
<tr>
<th>Test Chips</th>
<th>Software</th>
<th>Linux port</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proof of Concept SoCs</td>
<td>IoT SoCs</td>
<td>Bare metal software</td>
</tr>
<tr>
<td>Minion processors for power management &amp; communications</td>
<td>Microcontrollers</td>
<td>RTOS, Firmware</td>
</tr>
<tr>
<td>Bare metal software</td>
<td>Development tools</td>
<td>Technical Steering Committee, HPC SIG, GlobalPlatform partnership</td>
</tr>
</tbody>
</table>

### 2010-2016
- ISA Definition
- RISC-V Foundation

### 2018
- RV32
- RV32I and RV64I
- Base instructions: Integer, float, double, quad, atomic, and compressed instructions
- Priv modes, Interrupts, exceptions, memory model, protection, and virtual memory
- Architecture Compatibility Framework Trace

### 2019
- Vector
- Crypto Scalar
- Bitmanip
- Hypervisor
- ePMP
- Cache Mgt
- Virtual Memory
- Zfh
- Zfinx
- Zihintpause

### 2020
- ISA Extensions
- Profiles
- Packed SIMD
- Advanced Interrupts
- Java: ptr masking, I/D synch
- RV32E & RV64E
- Bfloat16
- Vector Half-Precision Floating Point
- Code Size
- Crypto Vector
- Fast Interrupts
- SMPU
- Zmmul
- Ztso
- Zihintntl

### 2023
- Matrix Ops
- Crypto Gost

### SIGS: Security
- Response, AI, Graphics, Android, Embedded, Datacenter/Cloud, Blockchain, Simulators, Managed Runtimes, Android, Functional Safety

### Programs: Dev Board Seed, Development Partners, RISC-V Labs

### Ecosystem

### ISA Extensions

### Platforms specs:
- Platforms, SEE, SBI, ABI, Discovery, Watchdog, ACPI, UEFI

### SOC specs:
- E-Trace, Nexus, IOMMU

### SIGs:
- Programs: Dev Board Seed, Development Partners, RISC-V Labs
- Ecosystem

### ISA Extensions
- Profiles
- Packed SIMD
- Advanced Interrupts
- Java: ptr masking, I/D synch
- RV32E & RV64E
- Bfloat16
- Vector Half-Precision Floating Point
- Code Size
- Crypto Vector
- Fast Interrupts
- SMPU
- Zmmul
- Ztso
- Zihintntl
In performance benchmarks, RISC-V is gaining ground really fast

- Researchers Benchmark Experimental RISC-V Supercomputer
- XuanTie C906 Tops MLPerf Tiny v0.7 Benchmark
- MIPS Claims "Best-In-Class Performance" With New RISC-V eVocore CPUs
- Andes Technology RISC-V Processors Reveal Outstanding Performance and Efficiency in MLPerf Tiny
- RISC-V Powered Mango Pi Takes on Raspberry Pi Zero at Its Own Game
- SiFive RISC-V Sees Some Performance Improvements On Ubuntu 22.04
- Greenwaves top results in MLPerf Tiny for hardware acceleration

Processors in development slated to overtake current proprietary alternatives.
RISC-V is rapidly building the strongest ecosystem

RISC-V instrumented with software top of mind

- **Open standards enable software choice.** Applications keen to run on RISC-V.
- **Toolchain and OS support** required for Extension ratification
- **Single hypervisor standard** to simplify and unify application support
- **Thousands of software developers** bringing workloads to RISC-V
- **Strategic imperative and investment** by commercial sector and geographies
- **Modern design approaches** leveraged for fewer instructions
Powerful forces fuel a unified RISC-V approach

Users: No one wants a repeat of vendor lock-in, avoid fragmentation of legacy ISAs.

Software: No one, not even a nation, can afford their own software stack. Upstream open-source projects generally only accept frozen/ratified RISC-V standards.

Fragmented Alternatives: Other architectures that enable an architecture license then do not have consistency on those implementations. In addition, there are multiple ISAs from other architectures such as A ISA, M ISA, as well as numerous versions.

- Trust zone and secure boot operate differently on different payment processing systems (credit card, Samsung/Google/Apple pay) for example depending on the manufacturer rather than a uniform approach.
- In IoT, the platform security architecture defines certification mechanisms that are implemented by third parties. Paypal is an example where the security mechanism moved to the cloud rather than the device.

Fragmentation: Same thing done different ways
Managing Diversity for RISC-V

Raw extensions
- Base + standard extensions + custom extensions
- Full suite of options available for experimentation and specialized uses
- Massive combinatorial space of options

ISA Profiles
- Packages of ISA extensions for given domain
- Initial set: RVI20 (basic), RVA20/22/23 (application processor)
- Factor out common ISA combinations for use in platform standards

Platform standards
- Hardware/software standards for platforms (much more than just ISA)
- Initial focus OS-A platform for Unix-like OS (includes IOMMU, AIA, etc)

Diversity: Solving different problems
RISC-V Technical Programs

RISC-V Platform
A common, reusable runtime environment that operating systems and applications can target to improve portability and reuse. Provides interoperability assurance.

RISC-V Profiles
Refers to a base ISA and one or more extensions that are specified as a group so that applications can be compiled once, run on different implementations, and get the same results.

RISC-V Developer Boards
Available to spur innovation, provide hands-on education, and engage early adopters to test and develop.

RISC-V Development Partner
Recognizes the investment and dedication of organizations making significant technical contributions to RISC-V.

RISC-V Lab
Institutions that host a lab with RISC-V hardware for CI/testing and general availability sandboxing.

RISC-V Compatible
Architectural Tests created to help ensure that software written will run on implementations that comply with that profile. Branding available for compatibility.

https://wiki.riscv.org/display/TECH
The total market for RISC-V IP and Software is expected to grow to $1.07 billion by 2025 at a CAGR of 54.1%
Rich RISC-V Ecosystem
Available Today

- **Applications**
- **Infrastructure**
- **Runtimes**
- **OS**
- **Hypervisor**
- **Boot**

- **Reliable, Serviceable, Diagnosable**
- **Performant**
- **Secure**
- **Debuggable**

- **HPC**
- **Data Center**
- **IoT**
- **Networking**

**Services**
- Training
- Research
- Academia
- CI/Testing
- Perf Tools
- Simulators
- Compilers

** ISA**
- Golden Model
- Architecture Tests

**Implementation Design & Microarchitecture**
- RTL
- DV

**Silicon**
- Soft IP

**RISC-V**
- SPIKE
- SAIL
- OpenSBI
- KVM
- OpenSSL
- DPDK
- OpenSBI
Investment and traction accelerate in 2022

PULP Platform HEROv2: Full-Stack Open-Source Research FPGA Platform for Heterogeneous Computing

HEROv2 for heterogeneous computing based on clusters of 32-bit RISC-V cores and an application-class 64-bit ARMv8 or RV64 host processor for sharing data between 64-bit hosts and 32-bit accelerators.

January 16, 2022

Intel Corporation Makes Deep Investment in RISC-V Community to Accelerate Innovation in Open Computing

RISC-V welcomes Intel to the Board of Directors to collaborate on RISC-V IP and contribute to RISC-V software development

Intel Creates $1B Innovation Fund To Grow RISC-V Market (And Attract New Foundry Customers)

February 7, 2022

The European Commission announced a new European Chips Act of €15 billion in additional public and private investments until 2030. This adds to €30 billion of public investments previously earmarked.

February 8, 2022

Automotive RISC-V processor functional design verification

NSITEXE selected ImperasDV for RISC-V design verification, expanding Imperas’ simulation technology, models, verification IP and tools by NSITEXE for next gen 64bit RISC-V vector accelerators in AI automotive with verification for level needed to attain ISO 26262 ASIL D.

January 6, 2022

Intel to spend €17bn on chip mega-factory in Germany… expands manufacturing in Ireland, plus R&D and packaging across Europe

March 15, 2022
We're thrilled to be featured on the @Nasdaq video wall this morning to celebrate our historic moment: a $2.5B valuation from our Series F round! #RISCV #NoLimits

Clockwork Pi announced availability of DevTerm R-01, the first 64-bit RISC-V portable computer with retro styling and modern computing power.

The government of India Ministry for Electronics & Information Technology launched Digital India RISC-V (DIR-V) program with aggressive milestones for commercial silicon of SHAKTI & VEGA.

MIPS Pivots to RISC-V with Best-In-Class Performance and Scalability


eVocore I8500 – power efficiency: in-order multiprocessing with best-in-class power efficiency for SoC applications.
Imagination Technologies announces RTXM-2200 real-time embedded RISC-V CPU, a highly scalable 32-bit embedded solution with a flexible design for networking solutions, packet management, storage controllers, and sensor management for AI cameras and smart metering. June 21, 2022

Spain Approves €12.25b Semiconductor Investment Plan President Sanchez met CEOs of MicronTech Intel & Qualcomm at WEF22 on Spain's €12 billion strategy in global semiconductor industry with RISC-V lab at BSC, and Investment in Spain May 25, 2022

Università di Bologna, CINECA and E4 “Monte Cimone” Cluster, a RISC-V platform using SiFive RISC-V SoCs demonstrated remarkable software and hardware readiness and maturity - first gen RISC-V HPC machines coming soon. June 11, 2022

Microchip RISC-V based PolarFire FPGAs enter mass production: Microchip is writing a new chapter in the history of RISC-V with the availability of production-qualified SoC PolarFire devices. June 8, 2022

Accelerating ML Recommendation With Over 1,000 RISC-V/Tensor Processors on Esperanto’s ET-SoC-1 Chip June 17, 2022

Antmicro Renode 1.13 for improved machine learning and pre-silicon development June 17, 2022

XuanTie C906 Tops MLPerf Tiny v0.7 Benchmark June 13, 2022

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Antmicro Renode 1.13 for improved machine learning and pre-silicon development June 17, 2022

XuanTie C906 Tops MLPerf Tiny v0.7 Benchmark June 13, 2022
- **Esperanto** 1,000-Core RISC-V AI accelerator.
- **Alibaba** RISC-V Xuantie processors with 4 open cloud and edge processors
- **Imagination** RISC-V CPU family, for discrete and heterogeneous computing
- **Seagate** hard disk drive controller with high-performance RISC-V CPU.
- **Ventana** performance chiplet approach to data center SoC design
- **Intel** Nios processor based on RISC-V, designed for performance.

RISC-V CPU core market will grow 115% CAGR, capturing >14% of all CPU cores by 2025

– Semico Research, December 2021
Communication AI SoC RISC-V designs will grow 21.2% CAGR from 2019-27
– Semico Research, December 2021

- **Andes** RISC-V processor adopted by SK Telecom for AI products.
- **Alibaba** supporting Android 12 on their 64-bit RISC-V core emulated in QEMU
- **Sipeed** RISC-V chip runs Android 10, RV64 phone coming next
- **Alibaba** ported TensorFlow Lite for AI image, audio, and optical in smart devices.
- **Google** Pixel 6 Titan M2 RISC-V processor, with extra speed and memory, more resilient to advanced attacks.
RISC-V will command 28% of the IoT market by 2025

- **Huawei** Hi3861 RISC-V board for Harmony OS developers for IoT
- **Zepp Health** / Huami wearable manufacturer OS supporting RISC-V Reference Models for RISC-V P extension
- **GreenWaves** ultra-low power GAP9 hearables platform for scene-aware and neural network-based noise reduction.
- **RIOS Lab** announced PicoRio, an affordable RISC-V small-board computer.
- **SiFive** world’s fastest development board for RISC-V Personal Computers.

- Consumer, IoT devices
RISC-V-based AI SoCs will grow **73.6% CAGR** to **25B units** and **$291B** in revenue by 2027

- **Alibaba Cloud** tops MLPerf Tiny v0.7 Benchmark with its IOT processor
- **Esperanto** accelerating ML Recommendation With Over 1,000 RISC-V/Tensor Processors on ET-SoC-1 Chip
- **StarFive** released the world’s first RISC-V AI visual processing platform
- **Andes** released superscalar multicore and L2 cache controller processors.
- **NVIDIA CUDA** support on Vortex RISC-V GPGPU enables scaling from 1-core to 32-core GPU based on RV32IMF ISA

– Semico Research, December 2021
• **Fraunhofer** ported Tensorflow lite to their RISC-V processor core for Edge AI applications incl sensor data evaluation, gesture control, or vibration analysis.

• **Seeed Studio**’s new Sipeed MAIX, a RISC-V 64 AI board for Edge Computing makes it possible to embed AI to any IoT device.

• **Micro Magic** announced an incredibly fast 64-bit RISC-V core achieving 5GHz and 13,000 CoreMarks at 1.1V.

• **Western Digital** SweRV Core enables spectrum of compute at the edge

• **Microchip** released the first SoC FPGA development kit based on the RISC-V ISA.
- **E4 Monte Cimone Cluster** along with DEI-UNIBO contributing to architecture, software, and integration.

- **European Processor Initiative** RISC-V accelerator with first chip Sep 2021

- **Technical University of Munich** (TUM) quantum cryptography chip for quantum computing security demands

- **Tactical Computing Labs** HPC-centric software test suite for GCC and LLVM

- **Cortus** is developing a high-performance RISC-V Out-of-Order processor core for the European eProcessor project.

- **De-RISC** HW-SW platform for multi-core RISC-V SoC for safety critical aerospace

Johanna Baehr of TUM heads a team that has hidden four hardware Trojans on this chip - malicious functions that are integrated directly into the circuits.
SiFive high-end applications and real-time processors for leading performance, with lowest area and power consumption in vehicles for safety, security, and performance.

Andes launched safety-enhanced 32bit RISC-V CPU IP, first to be fully compliant with ISO 26262 functional safety.

IAR RISC-V Embedded Workbench for SiFive infotainment, connectivity, and ADAS products.

RISC-V will capture 10% of the Automotive market by 2025
– Counterpoint, September 2021

2020 RISC-V automotive opportunity 4M cores; growing to 150M cores in 2022 and 2.9B cores by 2025.
– Deloitte, December 2021

RISC-V Automotive Value Multicore SoC revenue to be $5.7B in 2022. Advanced RISC-V AI SoCs for High-End Passenger Cars to Reach $819M by 2027
- Semico Research, June 2022
**MobileEye** EyeQ Ultra vision advanced driver assist systems chips for 176 trillion ops per second with 12 RISC-V CPU cores.

**Andes** ISO 26262 Functional Safety ASIL D Dev Process Certification for RISC-V embedded safety with Andes processors.

**Renesas and SiFive** partner on next-gen, high-end RISC-V automotive applications. SiFive licenses RISC-V core IP to Renesas.

**Imagination Technologies** GPU linked by a RISC-V core for ASIL-B level designs with ISO 26262 safety critical certification.

**Green Hills** support RISC-V RTOS targeting ISO-26262 ASIL D applications.
MIPS RISC-V eVocore processors for high-performance, real-time compute in datacenter and automotive

Fraunhofer RISC-V Processor cores for functional safety and cyber security, and engaging in GaNext program.

IAR Systems functional safety of Embedded Workbench sw tool chain for NSI-TEXE RISC-V core.

NSI-TEXE 64bit RISC-V vector accelerators with ImperasDV design verification for automotive AI with ISO 26262 ASIL D.

Europe GaNext power converters with GaN power processors with better efficiency and compactness for EV chargers.

Kneron RISC-V based AI edge chip for Automotive
Dedicated Community

**Services** Fab, design services

**I/O** Memory, network, storage

**Software** Dev tools, firmware, OS

**Chips** SoC, IP, FPGA

**Universities and Research**

**Industries** edge/IoT, automotive, HPC/data center, embedded, AI/ML

**Investors** and Funding sources

**Press and Analysts**

**Individual Advocates**
“RISC-V continues to gain momentum around the world, and we plan to leverage SiFive’s portfolio of automotive RISC-V products in our future automotive SoC solutions to meet the exacting demands of these global customers.”

– Takeshi Kataoka, Senior VP and GM of Automotive Solution Business Unit at Renesas
More than 3,100 RISC-V Members across 70 Countries

RISC-V membership rapid growth of 134% in 2021
RISC-V delivers incredible member support
Benefits of engaging in RISC-V

- Accelerate technical traction and insight
- Contribute technical priorities, approaches, and code
- Gain strategic and technical advantage
- Increase visibility, leadership, and market insight
- Fill and increase engineering skills, retain and attract talent
- Build innovation partner network and customer pipeline
- Deepen, engage, and lead in local and industry developer network
- Showcase RISC-V products, services, training, and resources
Build RISC-V into your company strategy, and your personal mission

RISC-V is a community of passionate, dedicated, and invested stakeholders

As individuals
As companies
As universities
As public institutions and non-profits
As nations

As one Global, connected movement
Membership Options

**Premier Member Benefits**
- Board seat and Technical Steering Committee seat included at $250k level
- Technical Steering Committee seat included at $100k level
- Board level includes seat on RISC-V Legal Committee
- Eligible to lead workgroup and/or committee
- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Premier members
- Solution / Product listing highlighted on RISC-V Exchange, noted with member level
- 4 case studies a year
- 2 blogs per month
- 2 social media spotlights per month
- Spotlight member profile
- Event sponsorship discount

**Premier Requirements**
- Membership open to any type of legal entity
- $250k Annual membership fee that includes Board seat and TSC seat
- $100k Annual membership fee that includes TSC seat

**Strategic Member Benefits**
- 3 Board reps elected for the Strategic tier, including Premier members that do not otherwise have a board seat
- Eligible to lead workgroup and/or committee
- Use of RISC-V Trademark for commercialization
- Member logo / name listing on RISC-V website, alphabetical with Strategic members
- Solution / Product listing highlighted on the RISC-V Exchange, noted with member level
- 1 case study a year
- 1 blog per month
- 1 social media spotlight per month
- Event sponsorship discount

**Strategic Member Requirements**
- Membership open to any type of legal entity
- Annual membership fee based on employee size
  - 5,000+ employees: $35k
  - 500-5,000 employees: $15k
  - <500 employees: $5k
  - <10 employees & company <2 yrs old: $2k

**Community Member Benefits**
- Two Board representatives
- 1 Community Board representative, elected
- 1 Individual Board representative, elected
- Member logo / name listing on RISC-V website, by member level
- 1 case study a year
- 1 blog per quarter
- 1 social media spotlight per quarter
- Event sponsorship discount

**Community Requirements**
- Membership open to
  - academic institutions,
  - non-profits,
  - individuals not representing a legal entity
- No annual membership fee

RISC-V Membership details may be found online here
RISC-V Learn

Learning RISC-V is a challenging, highly rewarding activity. There are many resources available to help you on this technical journey, and we welcome new additions to these resources – please contact us at info@riscv.org with any questions or comments.

Learn Online
Online learning at beginner, intermediate, and advanced levels to increase engineering expertise and career opportunity on RISC-V across the industry.

Training Partners
Provide RISC-V training in a professional setting to extend the breadth and reach of RISC-V knowledge.

University Resources
Universities that support RISC-V curriculum and other programming as well as books and other learning resources.
Profiles and Platforms

ISA Profiles

- A set of **extensions** that are compatible
- **Extension types**: required, optional, unsupported, or incompatible
- **Two profile types**:
  - **Application (RVA[yy])**: Linux-class and other embedded designs with more sophisticated ISA needs
  - **Microcontroller (RVM[yy])**: Cost-sensitive application-optimized embedded designs running bare-metal or simple RTOS environments
- Running the same sequence of instruction between implementations are **RISC-V compatible**

System Platforms

- A set of **features** that are compatible
- Includes **ISA Profiles**, software and hardware **system components**, standardized **hardware/software interfaces**, etc
- **Two Platform types**: OS/A and M (naming TBD)
- Ability to move an executable from one implementation to another and get the same results are **RISC-V Compatible**
Software Horizontal Committee

Platform HSC
(includes platform specs)

- Config TG
- AIA TG
- Hypervisors SIG
- IOPMP TG
- OS-A Platform SIG
- RVM-CSI Platform TG
- OS-A SEE TG
- OS-A Platform TG
- OS-A PCT TG

Topics TODO:
- Linux class OSs
- RTOSs
- DMA
- Multi-processing
- JITs
- IOMMU, Buses
- Bootloaders
- Distro coordination/build/reli
- QOS
- Perf monitoring

TGs for specs underway

Toolchain & Runtimes HSC

- psABI TG
- Code Size TG
- HPC SIG
- Managed Runtimes SIG

Topics TODO:
- Benchmarks
- Regression test strategy
- Ecosystem changes
- Extensions needed
- Worst Case Execution Time (WCET)
- Spatial & Timing interference
- DSP
- DB & Hadoop et al
- Performance analysis
- Native code
  - GCC
  - LLVM
  - Optimizer
  - Profiler
  - gdb

AI/ML/NLP/Graphics SIG
Android SIG
Perf Modeling SIG
Perf Analysis SIG
IOMMU TG

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IOPMP TG

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Perf Analysis SIG
IOMMU TG

IOPMP TG

Dotted line

Done

TODO

Active

Dotted line
TODO
- Strategy
- Platform Interrupts
- Power Management
- Infrastructure

TODO
- Diagnosability
- Recoverability
- Data poisoning containment
- PCIe error reporting

Final Cost/Benefit/Completeness Checks by SW & Unpriv & Priv Committee chairs

Data Center SIG
HPC SIG
Embedded SIG
Fast Interrupts TG
Code Size TG
psABI TG
Packed SIMD TG
Debug TG

TODO
- Networking
- Wireless
- Edge
- Automotive
- Embedded