



codasip STUDIO

codasip RISC-V PROCESSORS

弊社L30 RISC-Vコアをベースに、Codalip Studioを使用し
カスタム命令を追加する内容です（5-10分）

- ※ 事前録画したものをご覧頂きます
- ※ ライブデモでは、ございませんので、予めご承知おきください
- ※ ご来場に合わせて、都度対応させて頂く予定です

当日可能な範囲で、その他、ご相談承ります

お問い合わせは takaaki.akashi@codasip.com まで

```
22 #include "config.hcodal"
23 #include "opcodes.hcodal"
24 #include "opcodes_ext.hcodal"
25 #include "isa.hcodal"
26
27 // part of the main ISA
28 set isa += i_ext_mac;
29
30 // Immediate oriented instructions
31 @element i_ext_mac
32 {
33     use reg_any as rd, rs1, rs2;
34
35     assembly { "mac" rd ",," rs1 ",," rs2 };
36     binary { 0:bit[7] rs2 rs1 OPC_X_MAC rd };
37
38     semantics
39     {
40         uXlen val, s1, s2, s3;
41
42         // read the input variables
43         s1 = rf_gpr_read(rs1);
44         s2 = rf_gpr_read(rs2);
45         s3 = rf_gpr_read(rd);
46         // do the job
47         val = (s1 * s2) + s3;
48         // write results back
49         rf_gpr_write(rd, val);
50     };
51 };
52
```

L30 - Profiling Result

Execute: fr_xxxx
Clock Cycles: 17200
Sampling Rate: 1

Instruction Set Coverage+ Source Code Coverage Source Code

Source Code Coverage

Samples per Symbol

Symbol	Address	Instructions	Instructions Percent	Cycles	Cycles Percent
fr	1174	17110	99.4%	17110	99.4%
__call_exitprocs	1314	29	0.2%	29	0.2%
main	1140	15	0.1%	15	0.1%
exit	120c	9	0.1%	9	0.1%
__register_exitproc	12a4	0	0%	0	0%
atexit	1200	0	0%	0	0%

L30_X_2 - Prof

Execute: fr_xxxx
Clock Cycles: 1500
Sampling Rate: 1

Architecture: RV_X_2
Studio Version: 9.0.3-1215
Created: Monday, 2021-11-08 11:08:11

Instruction Set Coverage- Source Code Coverage Source Code

Instruction Set Coverage isa

Top by Usage

Instruction	Count	Percent
fr.pl reg_any, reg_any, <imm>	3800	25.3%
c.add regs, <imm>	2284	15.2%
bfu reg_any, reg_any, <imm>	1900	12.7%
mac reg_any, reg_any, reg_any	1900	12.7%
c.mv reg_any, regs	765	5.1%