



CloudBEAR

RISC-V processor IP product line

RISC-V 32/64-bit cores product line



Small and efficient MCUs

BM
series

BM-310

RV32IMCAFNBK

BM-610

RV64IMCAFDNBK

Fast and compact embedded cores

BR
series

BR-351

RV32IMCAFN

BR-651

RV64IMCAFDN

Linux capable application cores

BI
series

BI-350

RV32IMCAF

Single issue

BI-651

RV64IMCAFD

Dual issue

BI-671

RV64IMCAFDBK

Out-of-order ²

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Single issue

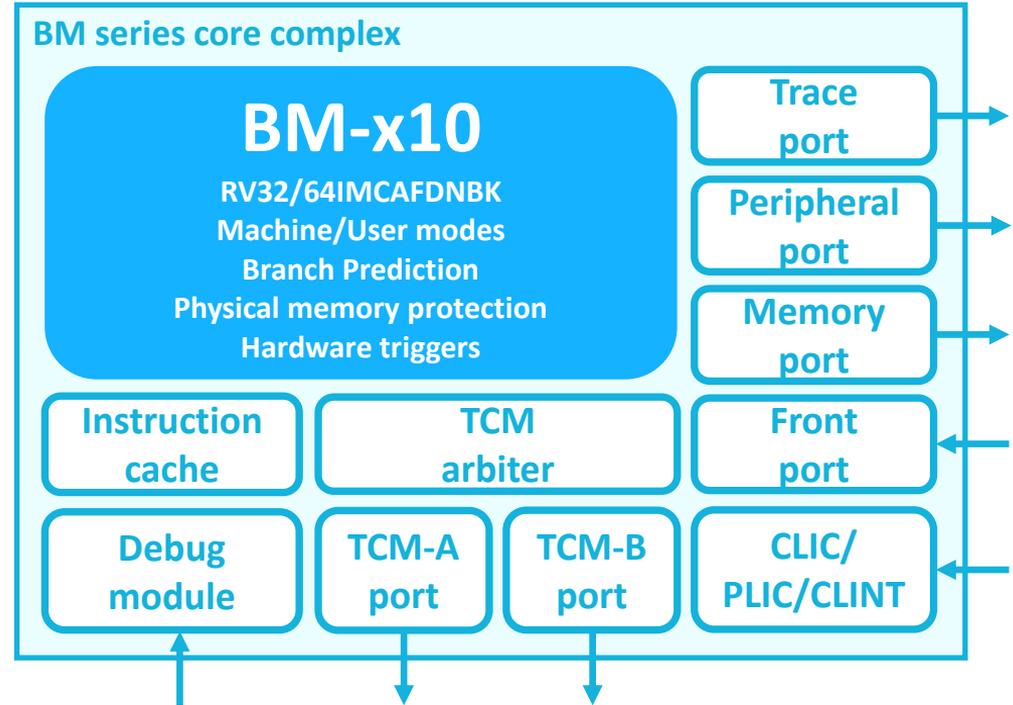
Dual issue

Out-of-order 3

BM-310/BM-610



- RV32/64IMCAFDNBK
- 2-4 stage configurable pipeline, single-issue
- Configurable ports (AXI4, AHB-lite)
- Instruction cache
- TCMs
- Branch prediction (static/dynamic)
- Configurable interrupt controllers
- Debug module
- **Nexus Trace IAR (NEW!)**
- **B, K extensions (NEW!)**



BM-310

Benchmark (GCC 10.1)	Score/MHz
Dhrystone (ground rule)	1.83
Coremark	3.91
Embench-IoT	1.21*

BM-610

Benchmark (GCC 10.1)	Score/MHz
Dhrystone (ground rule)	1.91
Coremark	4.00
Embench-IoT	1.38*

450-700MHz @ 28nm, worst case **

* Performance relative to ARM Cortex-M4 vs RV*IMCB

**Highly depend on process and memory compiler

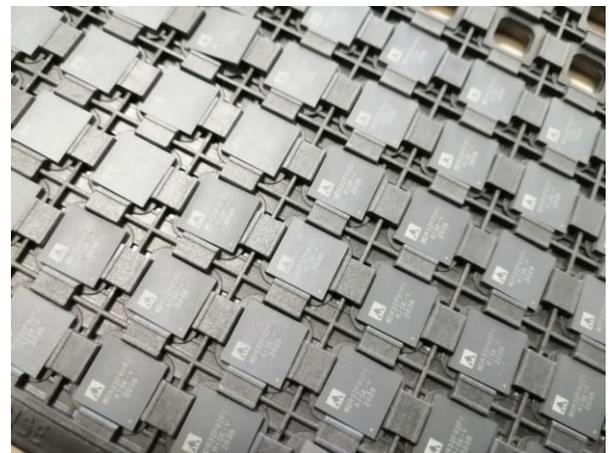
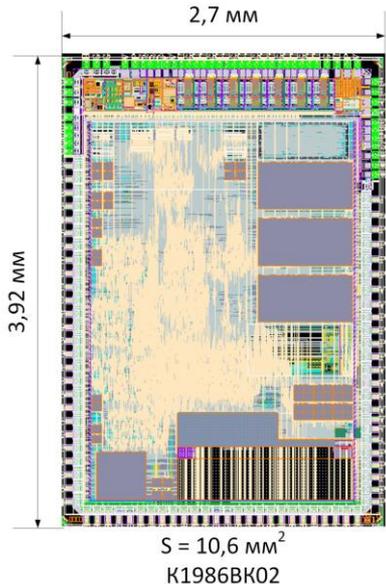
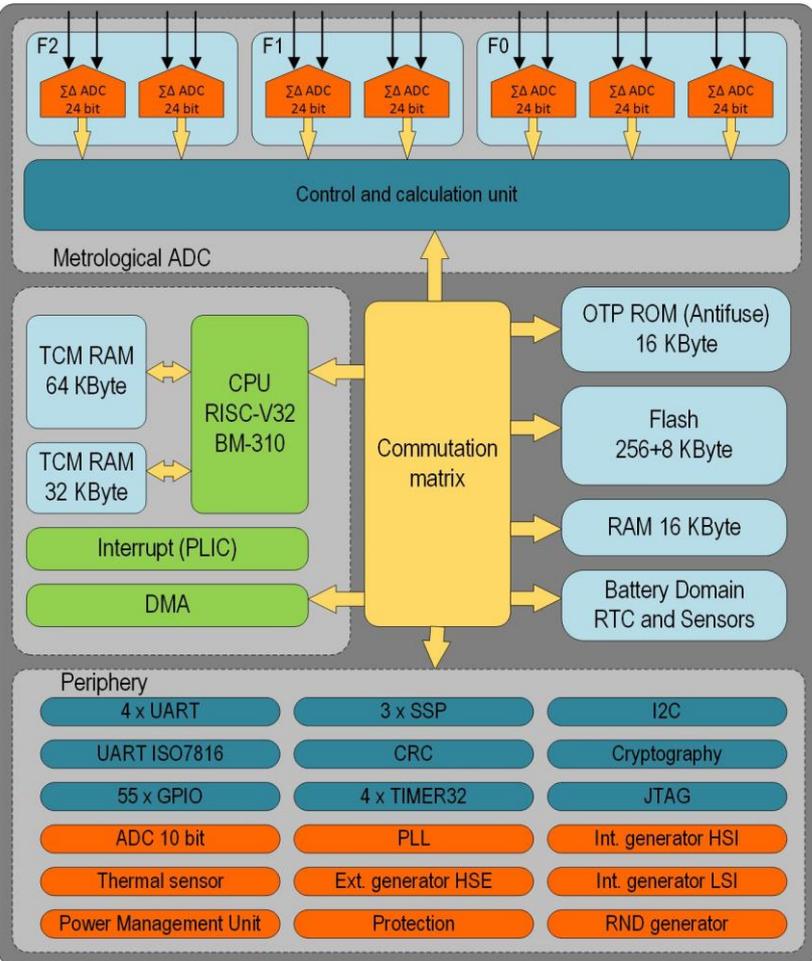
Example customer case: Smart Metering MCU



Milandr

BM-310

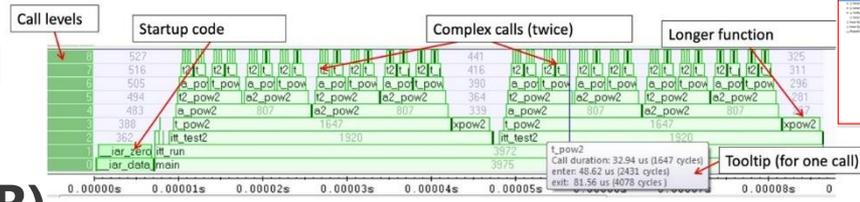
- TSMC 90nm LP
- Better than Cortex-M4 performance at lower power
- Shipping mass production



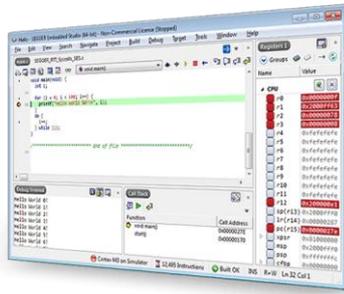
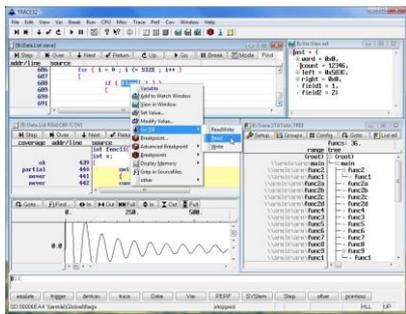
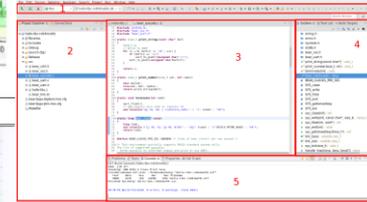
Development tools



- Third-party ecosystem of development tools
- Interoperability due to Debug spec
- HW triggers for eFlash and ROM breakpoints
- **Nexus trace available (IAR)**



Eclipse IDE



Digilent
JTAG-HS3



IAR
SYSTEMS



LAUTERBACH
DEVELOPMENT TOOLS



SEGGER

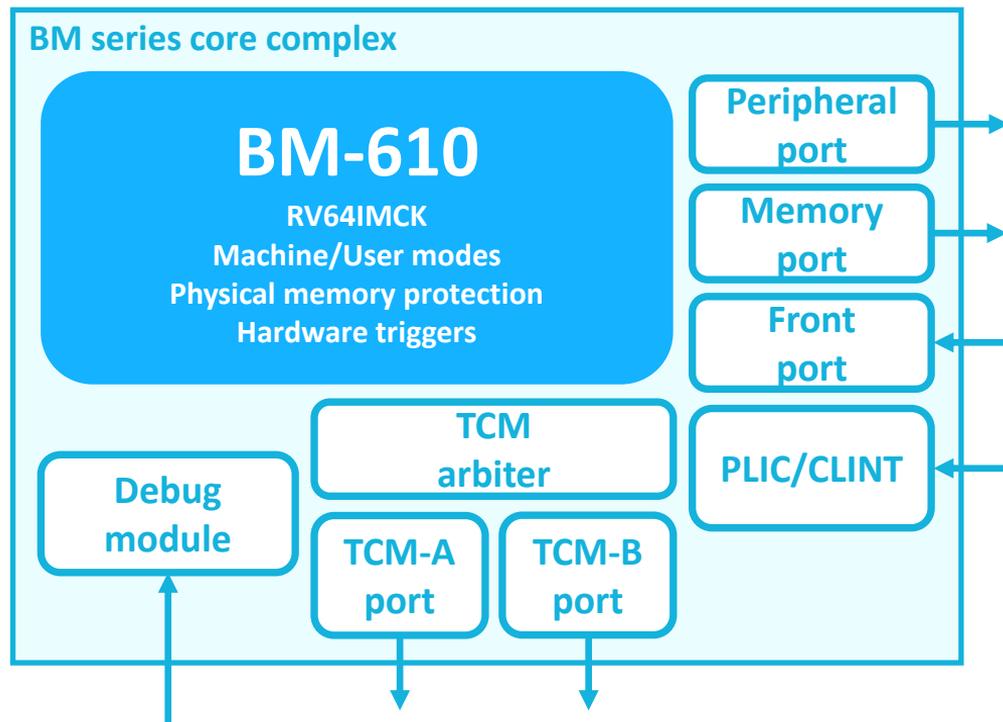


Housekeeper and security boot processor



- BM-610
 - RV64IMCK
 - 2-4 stage configurable pipeline, single-issue

Crypto Algorithm	Mbit/s/MHz
AES128	1.2
AES192	1.04
AES256	0.9
SHA2-224	0.19
SHA2-256	0.19
SHA2-384	0.33
SHA2-512	0.33



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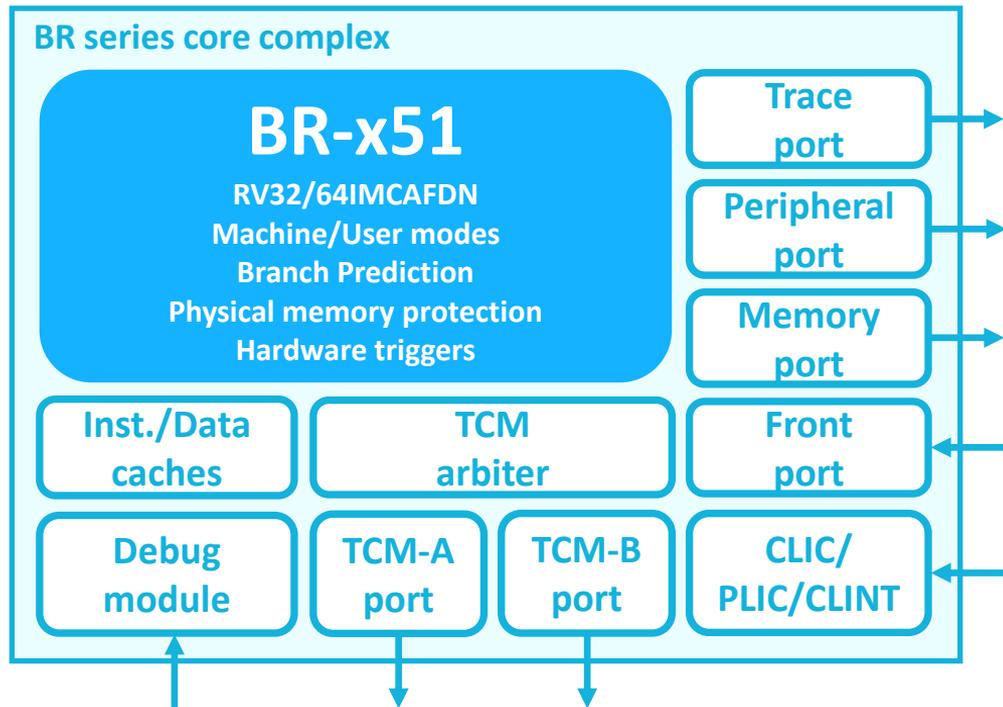
BR-351/BR-651

High-performance embedded cores



- RV32/64IMCAFDN
- Dual instruction issue
- 9-stage pipeline
- 1.2GHz @ 28nm worst case

Benchmark	Score/MHz
BR-351 Dhrystone (ground rule)	2.3
BR-651 Dhrystone (ground rule)	2.5
Coremark	5.0



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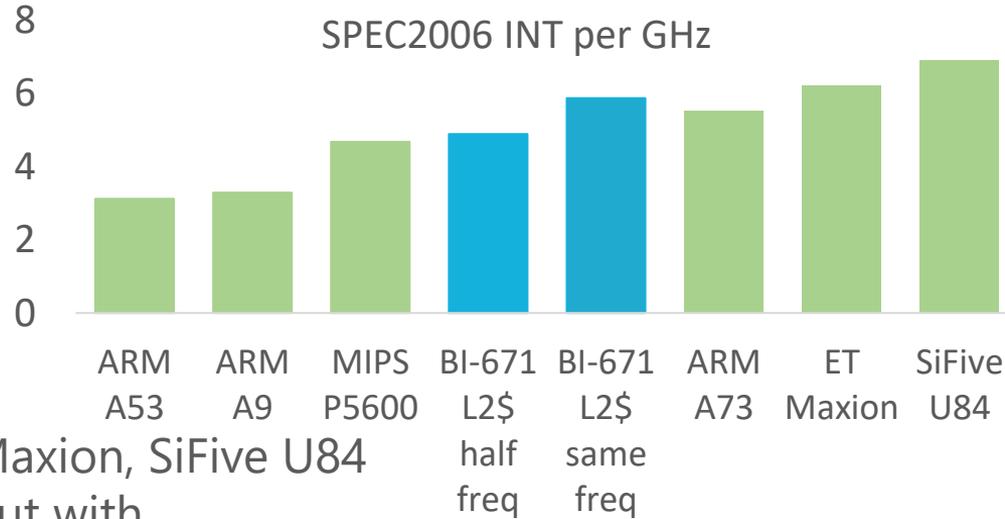
Dual issue

BI-671

RV64IMCAFDBK

Out-of-order ¹¹

BI-671 performance



- 75-80% of ET Maxion, SiFive U84 performance, but with implementing lesser power and smaller area 2-way superscalar comparing to 4-way
- 1.5-1.8x better performance than ARM A53
- On the same performance level with MIPS P5600

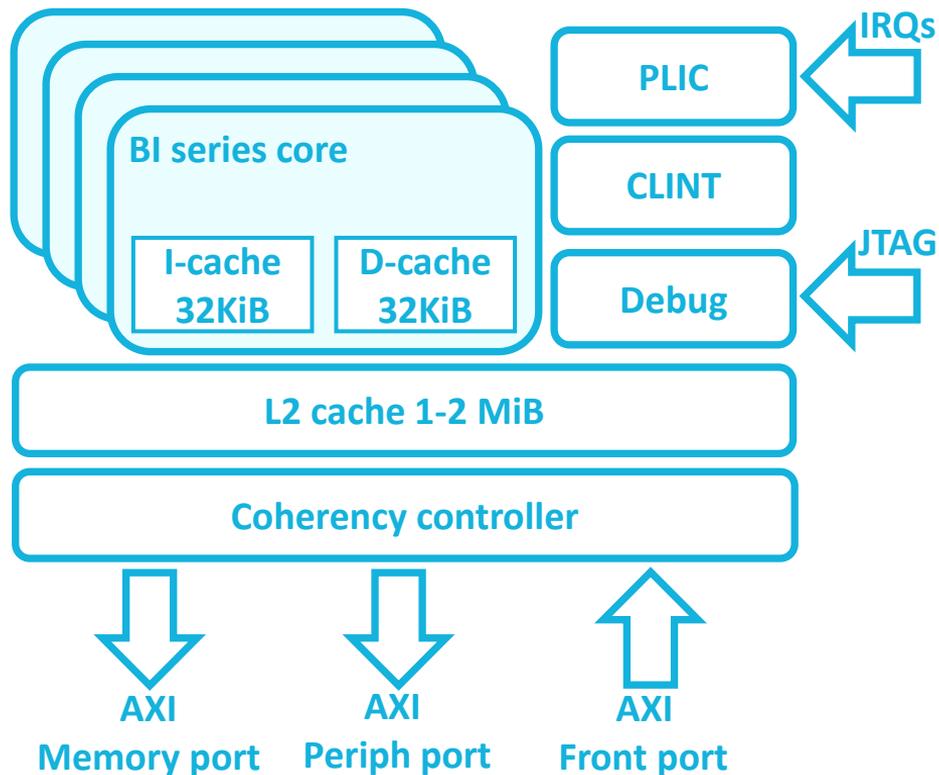
B, K extensions (NEW!)

Benchmark	Score/MHz
Dhrystone	3.87
Coremark	5.66

BI series core complex

Linux capable application cores

- Multi-core fully coherent configuration
- Machine/User/Supervisor modes
- 32 KiB 8-way I/D caches
- L2 cache 1-2 MiB
- Debug module
- Platform Level Interrupt Controller
- Physical memory protection
- Coherency controller for maintaining coherency with peripherals and accelerators



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www.cloudbear.ru