CHIPS Alliance: The Open Source Hardware Roadmap

Michael Gielda, Chair of Outreach, CHIPS Alliance
VP Business Development, Antmicro

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AGENDA

Who are we?

Today’s compute & design challenges

CHIPS Alliance projects

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What is CHIPS Alliance?

- Organization which develops and hosts:
  - Open source hardware code (IP cores) -> think open source CPUs, I/O, interconnects, ML
  - Open source ASIC & FPGA development tools -> design, verification, simulation, workflows
- A barrier-free environment for collaboration:
  - Standards organization framework for collaboration and development
  - Under governance of Linux Foundation
  - Legal framework – Apache v2 license / OWFa
- Shared resources ($, code, practices, infrastructure and time) which lower the cost of hardware development

CHIPS Alliance members – companies

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CHIPS Alliance members – universities, labs and projects

UC San Diego

Yale University

HOCHSCHULE FÜR ANGEWANDTE WISSENSCHAFTEN MÜNCHEN

UNIVERSIDAD NEBRIJA

RIOS

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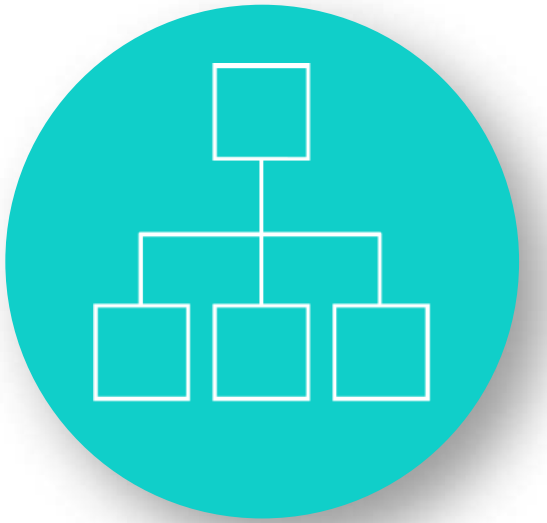
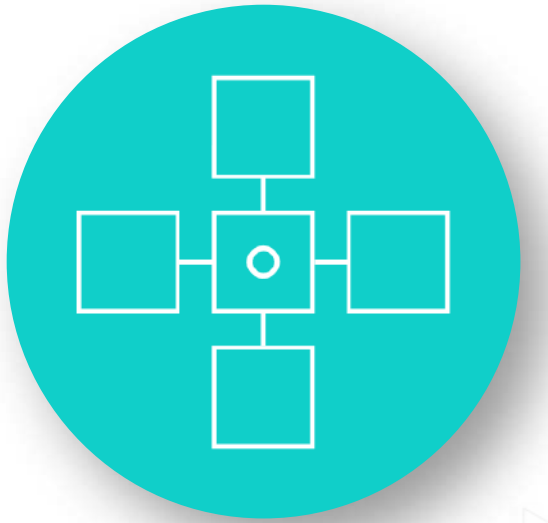
Compute and Design Challenges

Costs of hardware increasing significantly



Innovation often stalled in corporate structures



Need more purpose-built architectures

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CHIPS Alliance Aims to Deliver

- Lower development costs
  - Leverage common IP – CPU cores, Neural network accelerators, Uncore components (PCIe, DDR…), Interconnects
  - Collaboratively develop open source hardware design & development tools and infrastructure – enables new level of innovation where design engineers can modify design tools
- Open Source Collaboration in hardware
  - Allows breakthrough innovation drawing upon broad expertise and diverse experience
  - Enables purpose built solutions – think specific accelerators for new AI workloads - while keeping alignment / compatibility
- Blue hat business model development and promotion of open source policies

CHIPS Alliance Projects

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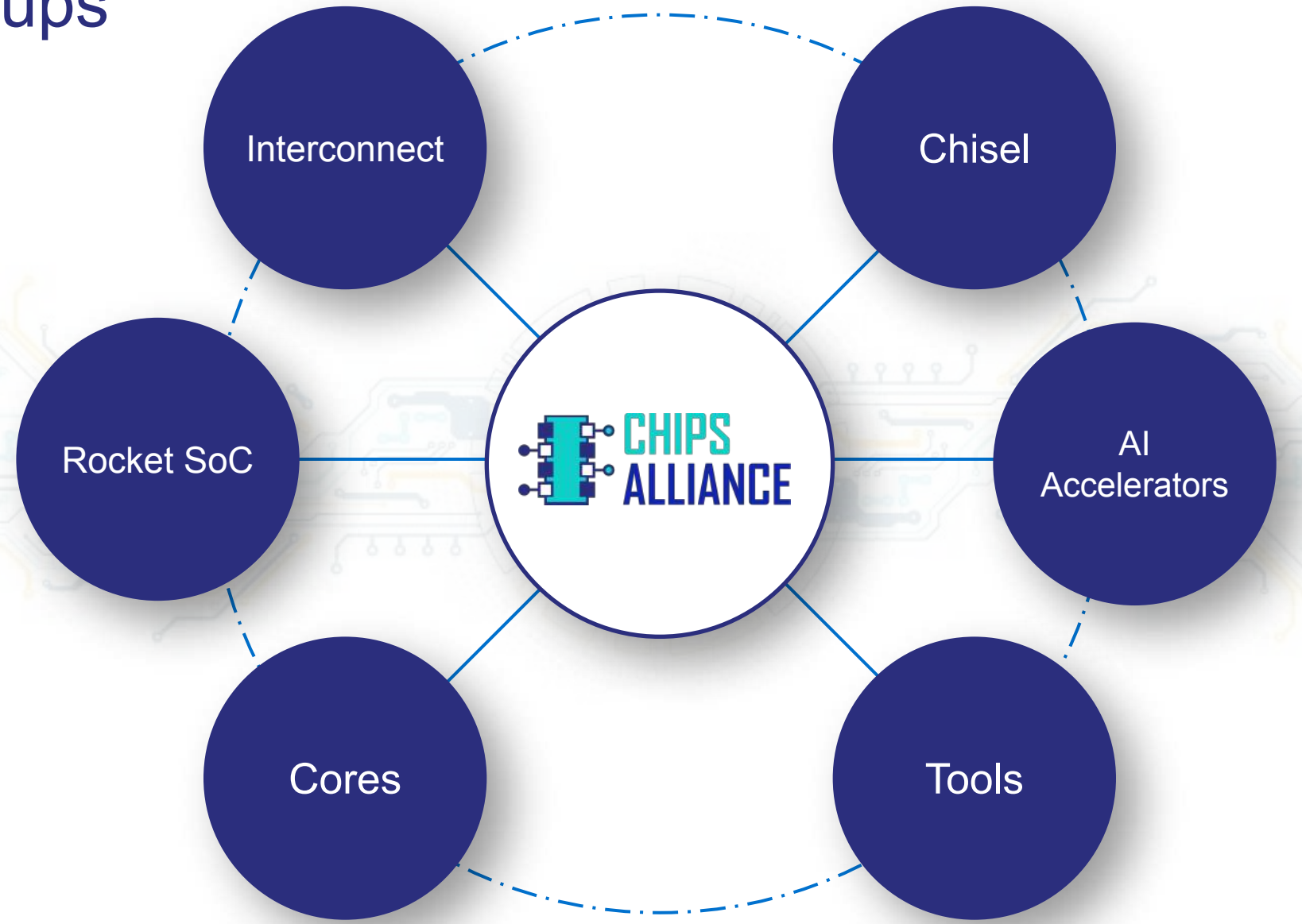
Workgroups


Interconnect
Chisel
Rocket SoC
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AI Accelerators
Cores
Tools

Milestone Achievements in 2020

- Started major project on SystemVerilog in Verilator and other FOSS tools
  - open source synthesis of SystemVerilog cores
  - fully open source SV linting and formatting flow in CI, testing suite and parsers
- Key new major projects that joined in 2020:
  - Chisel
  - OpenROAD
- Released AIB 2.0 chiplets specification
- Delivered new generation of SweRV RISC-V embedded cores (EH2 and EL2):
  - First open-sourced dual threaded high performance core targeting embedded/realtime
- Successful demonstration of OmniXtend memory centric compute system

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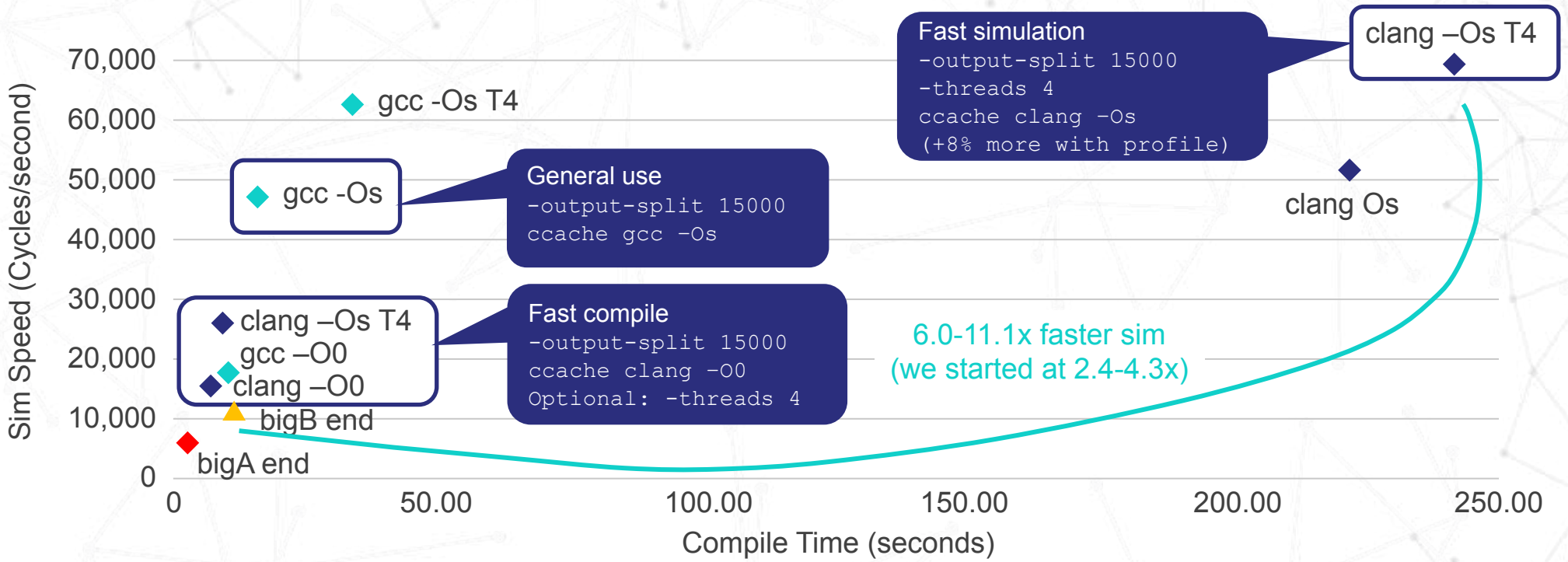
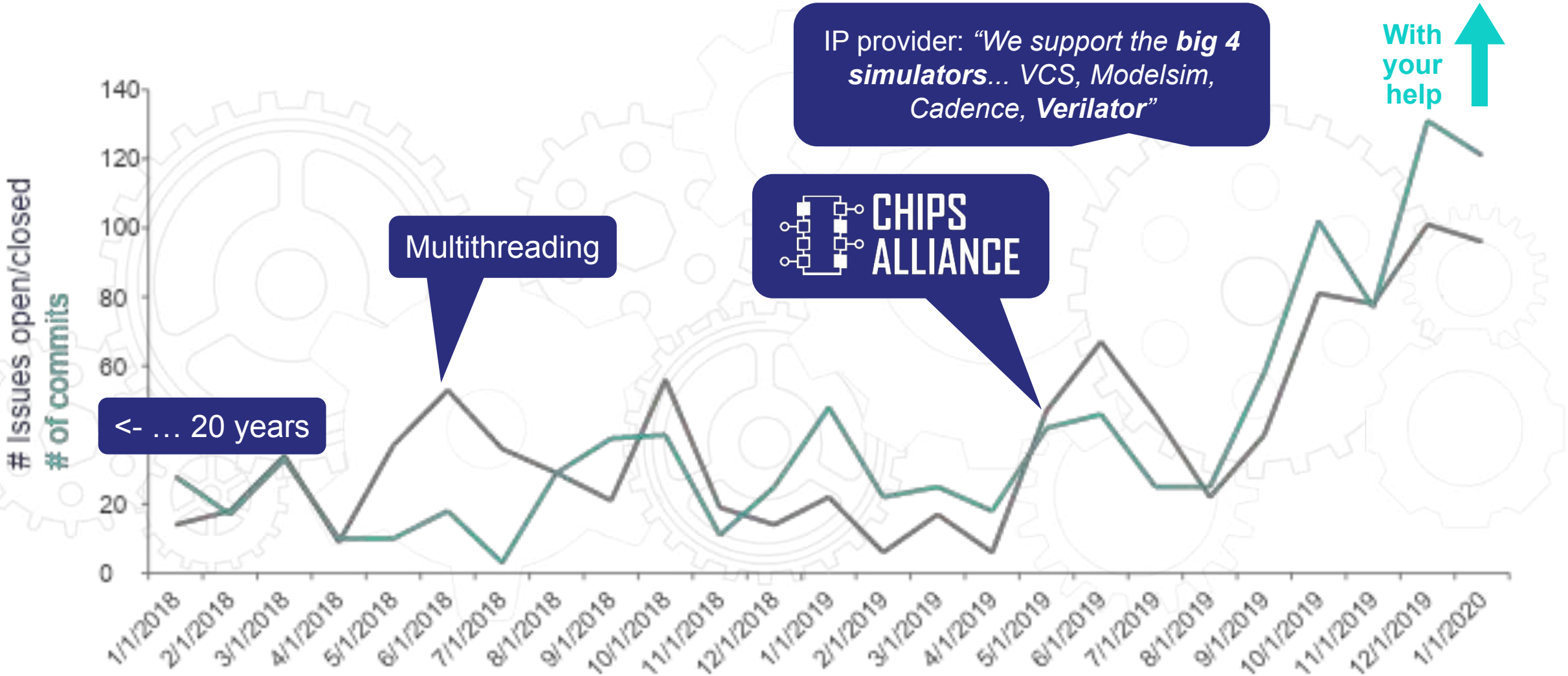
Why is Verilator RTL Simulator Interesting?



- It outperforms big three simulator by factor of up to 11x
- It can be easily customized for unique team needs:
  - Fast compile, faster execution than big three OR slower compile, incredibly faster execution
- High simulation speed implies running firmware or software on top of the simulator

Accelerated Development



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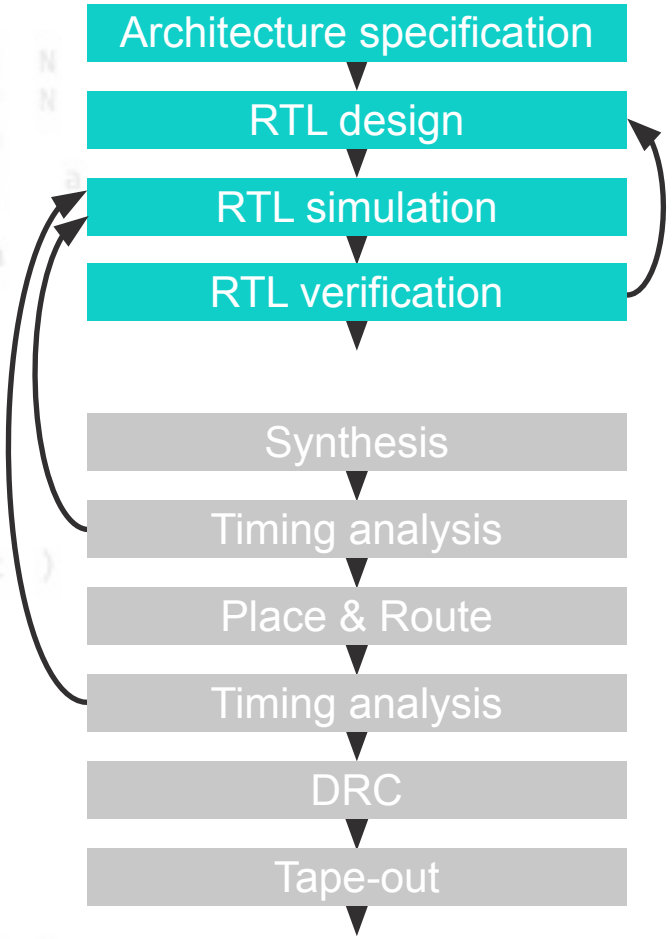
Open Source EDA Tools: Long Term (7 Year) Vision



- RTL simulator
- Design verification
- Synthesis:
  - Synthesizing design using device models that came from the foundry
- Timing analysis:
  - Checking if timing at target frequency is closed after synthesis and after place and route
- Place and route:
  - How do you customize for your own applications, when tools are close-sourced?
  - Most active area where significant disruption is occurring
  - Using machine learning models to guide place and route, instead of traditional algorithm driven – enables more power efficient and faster designs than expected

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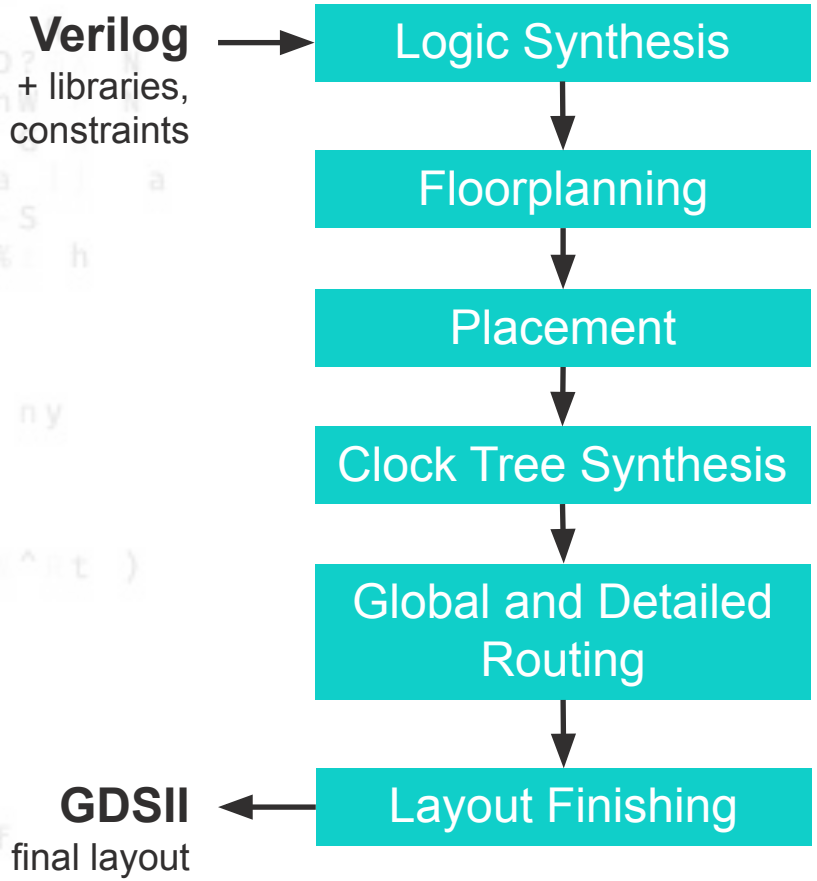
OpenROAD: No Humans, 24 hours + Open Source



IDEA will create a no-human-in-the-loop hardware compiler for translating source code to layouts of System-On-Chips, System-In-Packages, and Printed Circuit Boards in less than 24 hours

A. Olofsson, DARPA, ISPD-2018 keynote

- Digital tool flows for chip, package and board
- All tools open-source
- Flow is fully automated
- Seed an ecosystem through CHIPS Alliance
- Bring EDA research closer to industry and designers:
  - Enable critical algorithm innovation by providing functional framework

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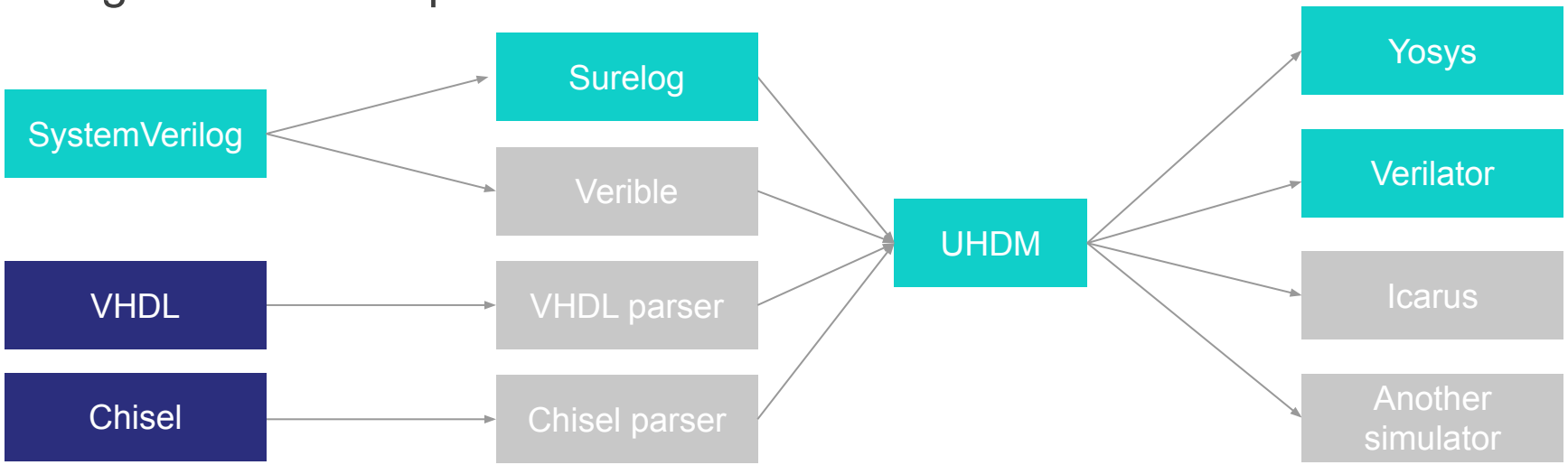
SystemVerilog in open source tooling

- Collaboration between Google, Western Digital, Antmicro
- Verible - SystemVerilog linter/formatter
- Surelog - SystemVerilog parser, front-end to UHDM
- Universal Hardware Data Model (UHDM)
  - An intermediate representation of a SystemVerilog design
  - Library for connecting front- and back-end of various tools
- CHIPS Alliance expanding UHDM support to Verilator and Yosys
- Work on expanding Verilator for open source verification



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SystemVerilog Test Suite

- Test suite for SystemVerilog (including some UVM) support in open source tools
- Aims to pinpoint all the supported and missing SystemVerilog features in various tools.
- Generates report from last passing master build at https://symbiflow.github.io/sv-tests/
- Introduces three types of tests:
  - Testing individual features as per the SystemVerilog standard
  - Existing third party test suites
  - Selected open source IP cores, such as SweRV, Ibex and others

		icarus	moore
Ariane RISC-V core	ariane	0/1	0/1
Tests imported from Basejump STL	basejump	75/320	88/320
BlackParrot RISC-V core	black-parrot	0/6	0/6
Lowrisc chip with Ibex core	earlgrey	0/1	0/1
FX68K m68k core	fx68k	0/1	0/1
Tests imported from hdlConvertor	hdlconv	55/306	54/306
Ibex RISC-V core	ibex	0/1	0/1
Tests imported from ivtest	ivtest	1579/1631	405/1631
RSD RISC-V core	rsd	0/1	0/1
Various sanity checks	sanity	1/1	1/1
SCR1 RISC-V core	scr1	0/1	0/1
SweRV RISC-V core	swerv	0/1	0/1
Taiga RISC-V core	taiga	0/1	0/1
Tests imported from utd-SystemVerilog	utd-sv	121/295	15/295
Tests imported from UVM	uvm	3/152	3/152

Open source synthesis of ibex core

- Verible and Surelog support for ibex, RISC-V 32 bit core written in SystemVerilog
- used in OpenTitan - first open source root of trust chip
- lowRISC, Google, Western Digital collaboration
- enabling useful CI workflows and practices, being adopted by other organizations

Advanced Interface Bus (AIB) PHY: Standard Chiplet Interface

AIB: Scalable chiplet (die-to-die) physical interface

- Optimized for low power, high bandwidth, and ease of porting to new and mature silicon technologies
- Build protocols like AXI on top of AIB

Open CHIPS Alliance AIB Specification

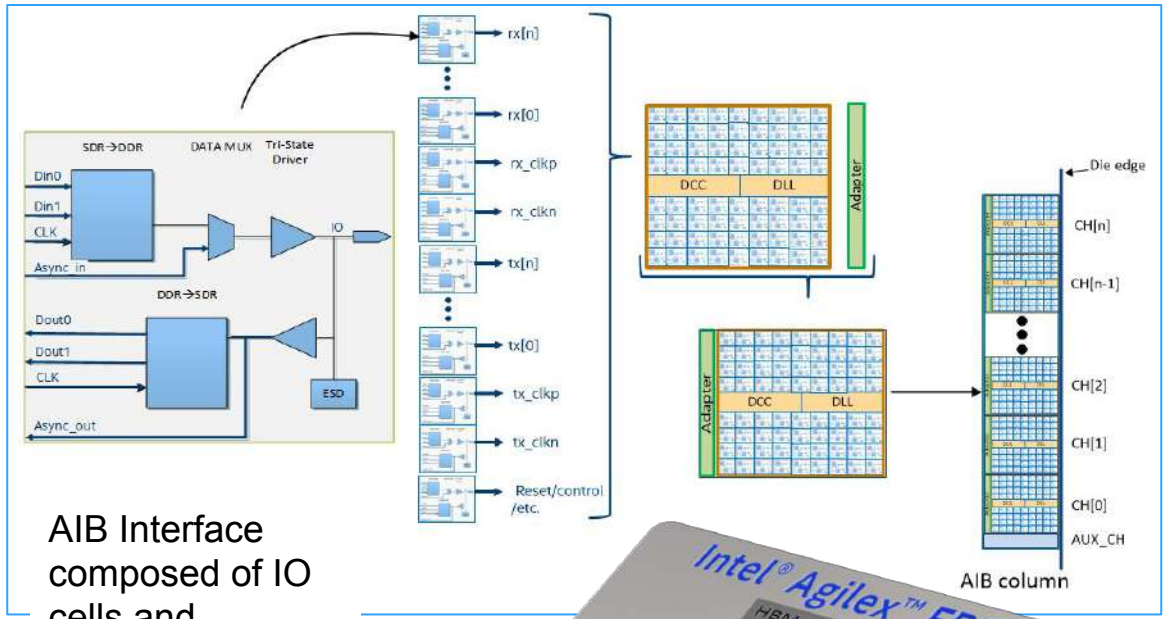
- Electrical specs, bump array mechanicals, data/ clock/ control signal definitions, reset sequence, JTAG reqts

Open source hardware intended to reduce the cost of implementing a high performance die-to-die interface

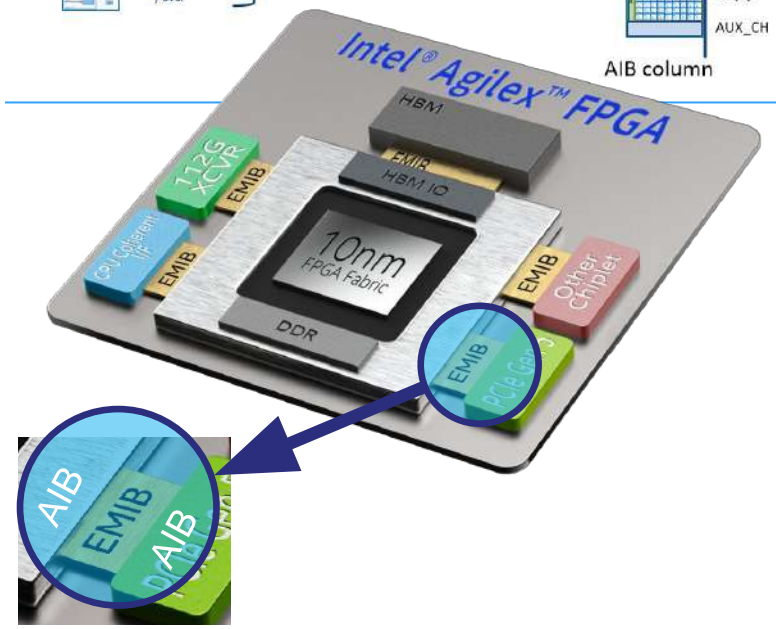
- RTL, cell models, testbenches

Delivered AIB 2.0

- Double I/O density
- Double data rate
- Lower I/O voltage for 0.5pJ energy/bit

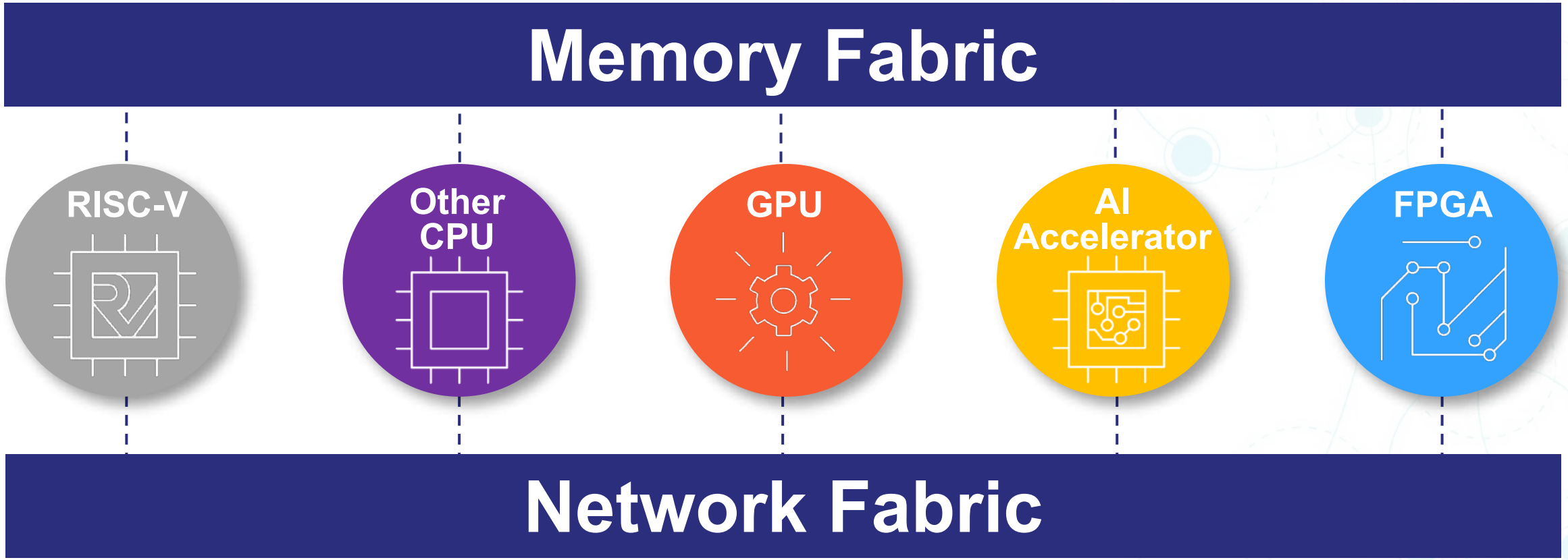


AIB Interface composed of IO cells and channels



AIB PHY intended for advanced packaging technologies such as silicon bridges, interposers and fan-out

Cache Coherent Memory Fabric – OmniXtend



Memory is the center of the architecture

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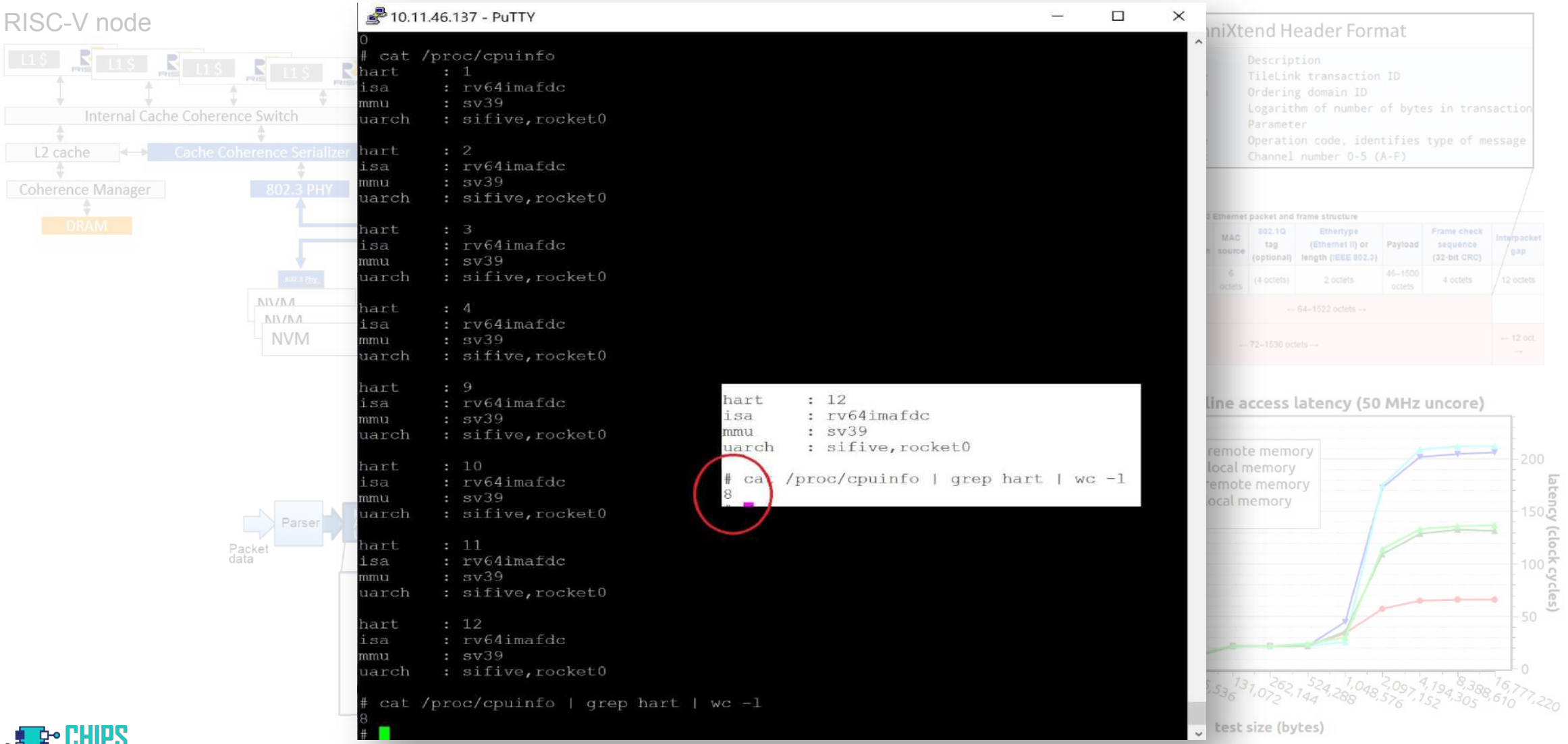
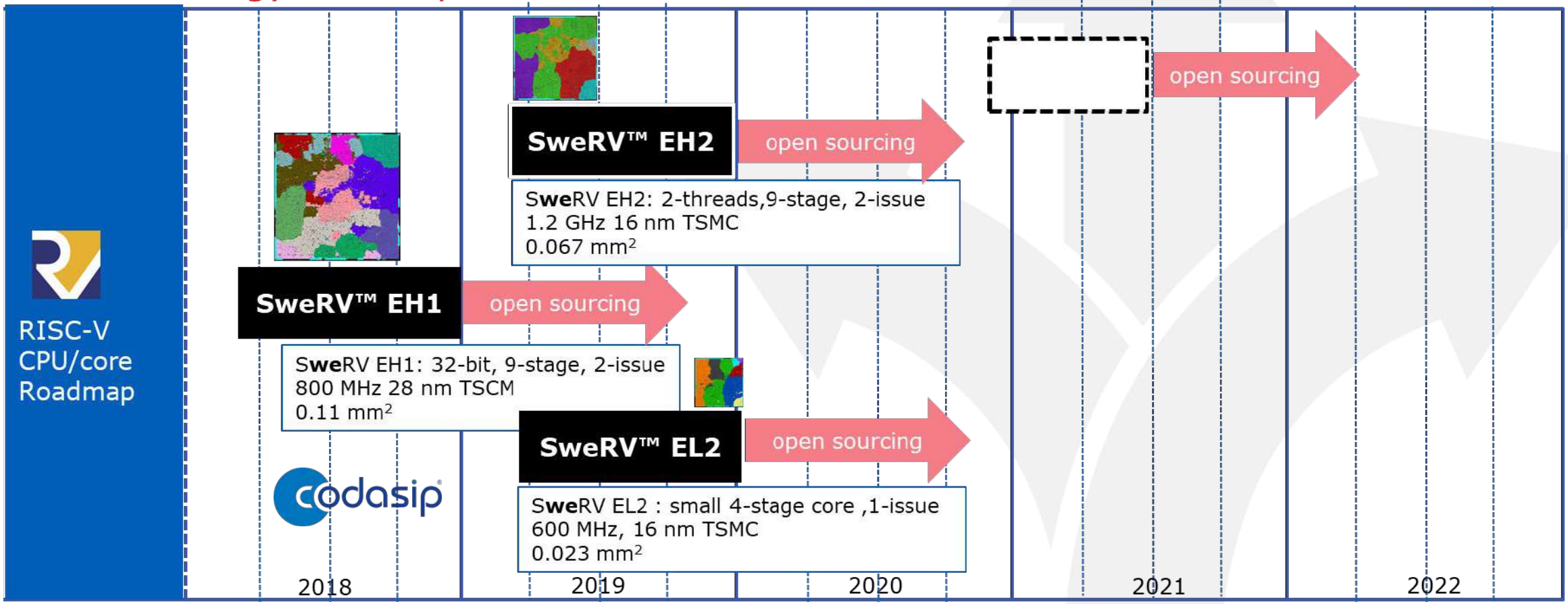
OmniXtend Architecture Overview



SweRV™ Core Roadmap

CPU technology roadmap



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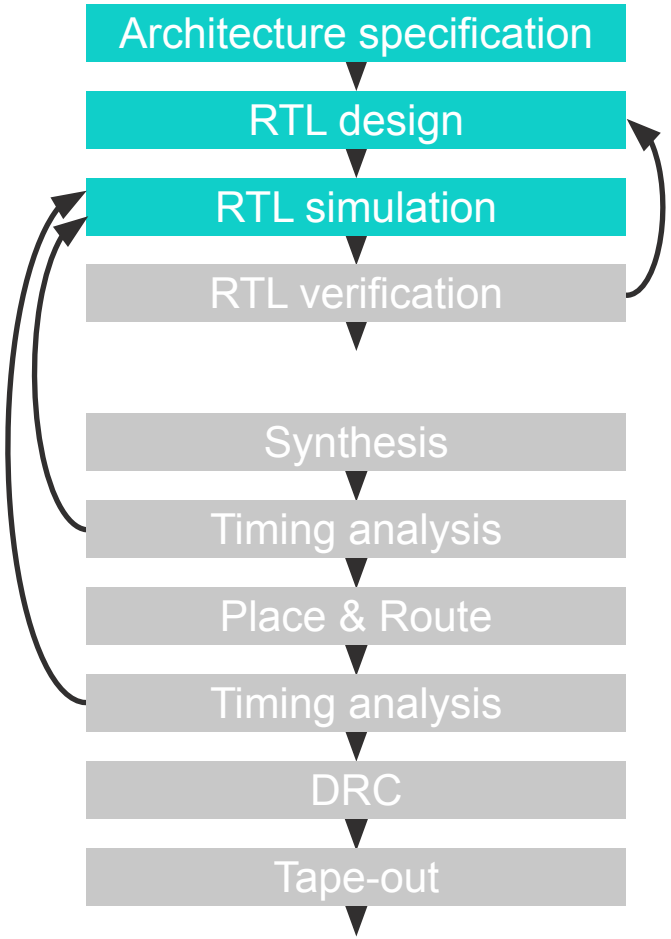
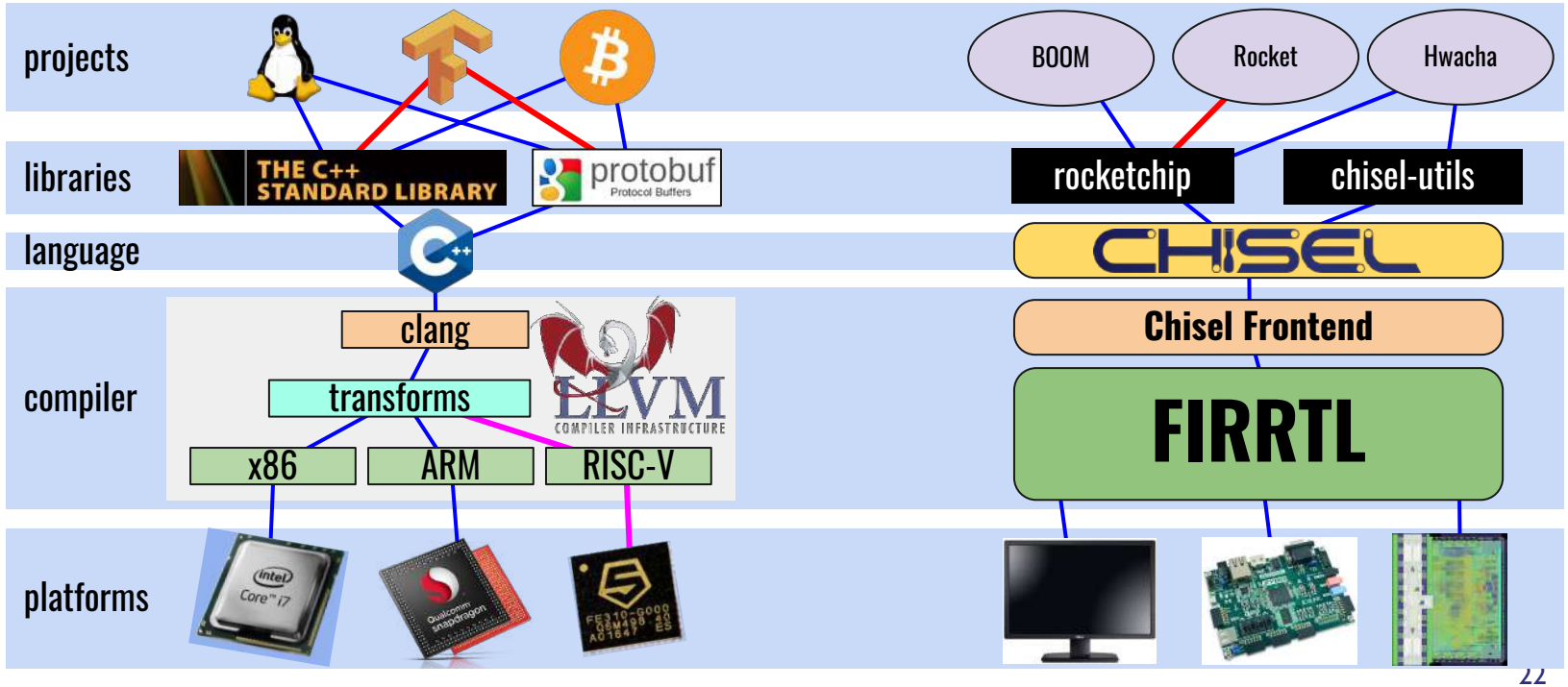
Open source EDA tools: Chisel + Chisel tools ecosystem



- RTL design automation:
  - The goal of Chisel is to AVOID RTL design, as much as we avoid assembler when programming computers
  - Programming is done in Scala programming language, and compiled into Verilog (RTL)
- Fully integrated into CHIPS Alliance, biggest success story



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Join the Alliance!

- Share resources to lower the cost of hardware development: digital and analog IP
- Collaborate in developing of open source design tools software, share good practices
- Receive high quality, open source CPU/SoC designs and complex IP blocks
- Grow your business in this forward thinking organization

Join us!

https://chipsalliance.org/join/

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