What Age Are We In

Agile Hardware Development
Accelerate chip development and commercial adoption

Agile

Improved Security
Prevent side channel attack for example

Security

AWARDS & RECOGNITION
John Hennessy and David Patterson Receive 2017 ACM A.M. Turing Award

DSA

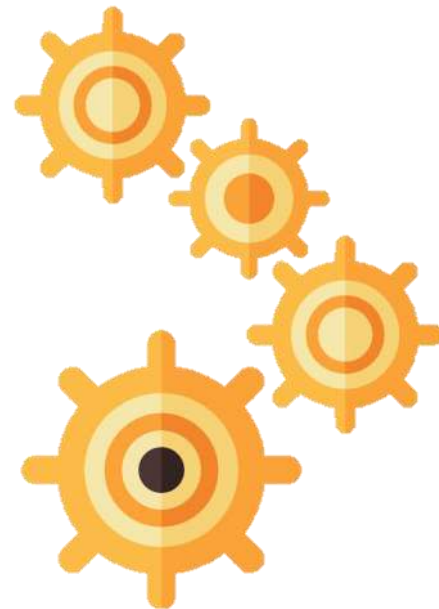**Domain-Specific Architectures**
Tailored to a specific problem domain and offer significant performance/efficiency gains

Open ISA

Open ISA
Industry-standard open ISA

A New Golden Age for Computer Architecture

OPEN ISA RISC-V

- Open ISA inspired by the success of open source software - Linux for processors

- Greater competition drive quicker innovation

- Incredible ecosystem support

Semi IPs · Foundry Services · ML/AI · Research · Design Services · Commercial · Academia · Cloud · Open Source · Dev. Tools · Software · Chip Vendors

Active Roles in RISC-V International

Frankwell Lin, CEO
RISC-V
Board Member

Dr. Charlie Su, CTO
Vice Chair, Technical
Steering Committee

Florian Wohlrab
RISC-V
Ambassador

ANDES
TECHNOLOGY

Who We Are

CPU

Pure-play CPU
IP Company

RISC-V Founding
Premier Member

Taiwan Stock
Exchange Listed

Major Open-Source
Contributor/Maintainer

Running Task Groups

Quick Facts

15
years old
company

200+
Licensees
Worldwide

80%
R&D
employees

5B+
accumulated Andes-
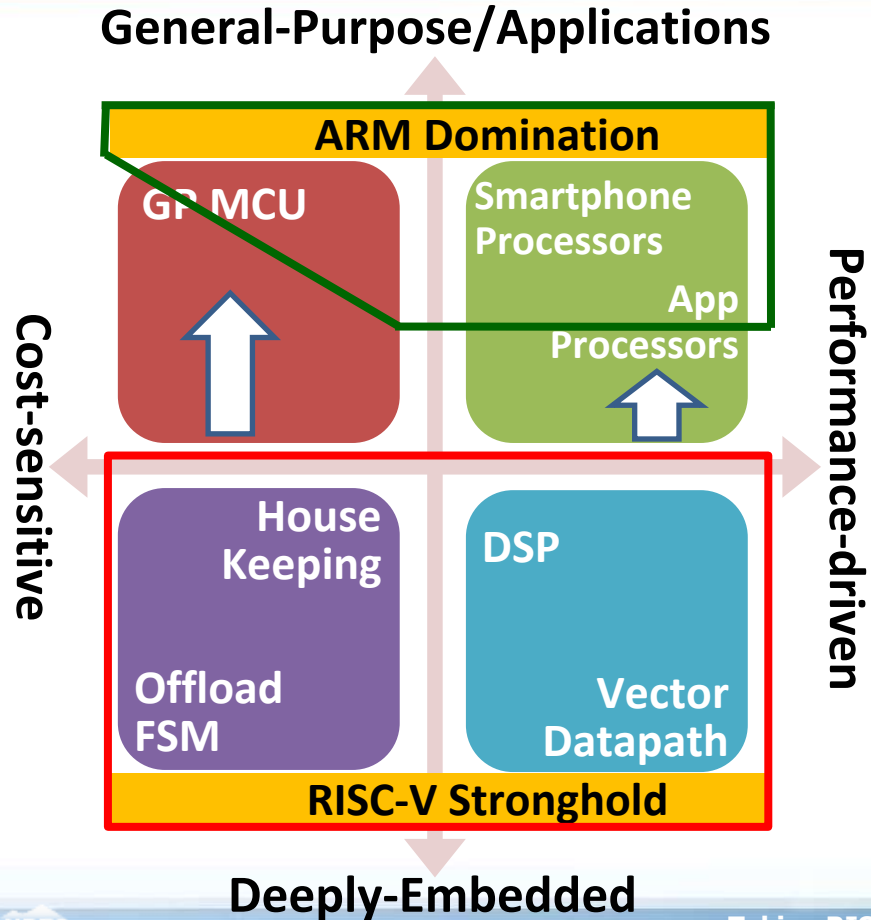embedded SoC shipped

17K+
AndeSight IDE
installation

Netherlands

France

USA

Beijing

Korea

Israel

Shanghai

Japan

Shenzhen

Taiwan HQ

RISC-V

Market adoption and usage examples

RISC-V Momentum Changing Processor Landscape

General-Purpose/Applications

ARM Domination

GP MCU

Smartphone Processors

App Processors

Cost-sensitive — **Performance-driven**

House Keeping

DSP

Offload FSM

Vector Datapath

RISC-V Stronghold

Deeply-Embedded

- RISC-V business quickly started in:
  - Cost affordable
  - Replacement of FSM and house keeping
- RISC-V is catching up MCU but not phone and tablet yet
- Andes focuses on real-time & performance
  - Bringing accelerators closer to CPUs
  - AI/AR/VR/CV/etc. in-between layer work-load
  - Efficiently move data

Andes RISC-V on Audio product

- D25F on LE Audio(BLE 5.2) for True Wireless Earbuds and Hearing Aids

  - Customer Tape out already!

  This product will be the one of the first SoCs supporting both of LE audio and Classic Audio
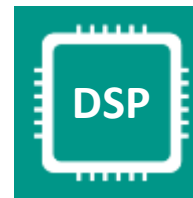
Bluetooth Baseband and Audio Subsystem	Application CPU	DSP/AI Accelerator

LC3 codec - high quality, low power LE Audio/BLE 5.2 – Multi-Stream, Broadcast Audio

Power Efficient – Excellent PPA
Mature Ecosystem – Support various RTOSs
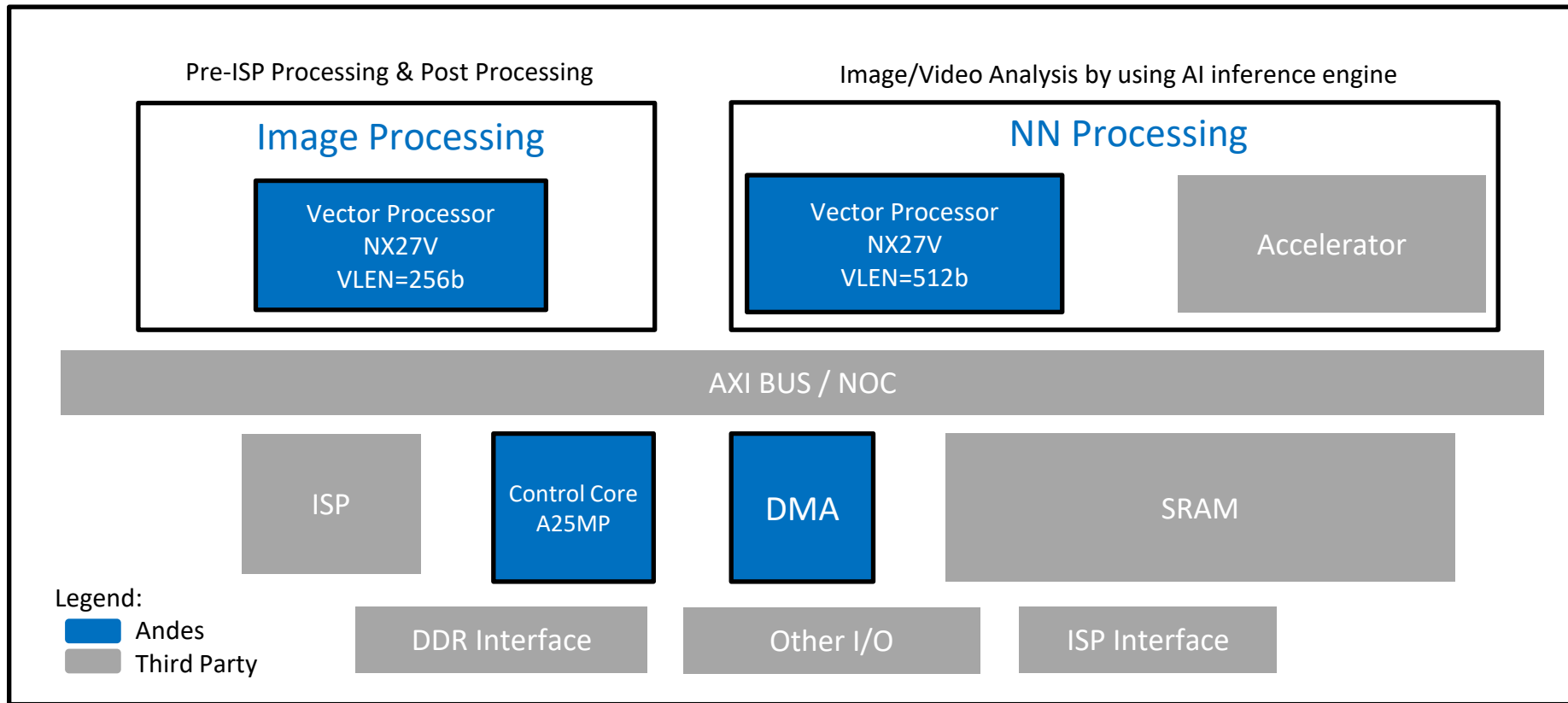**RISC-V DSP Extension** – outstanding performance DSP library

DSP Algorithm for Noise and Echo Cancelation
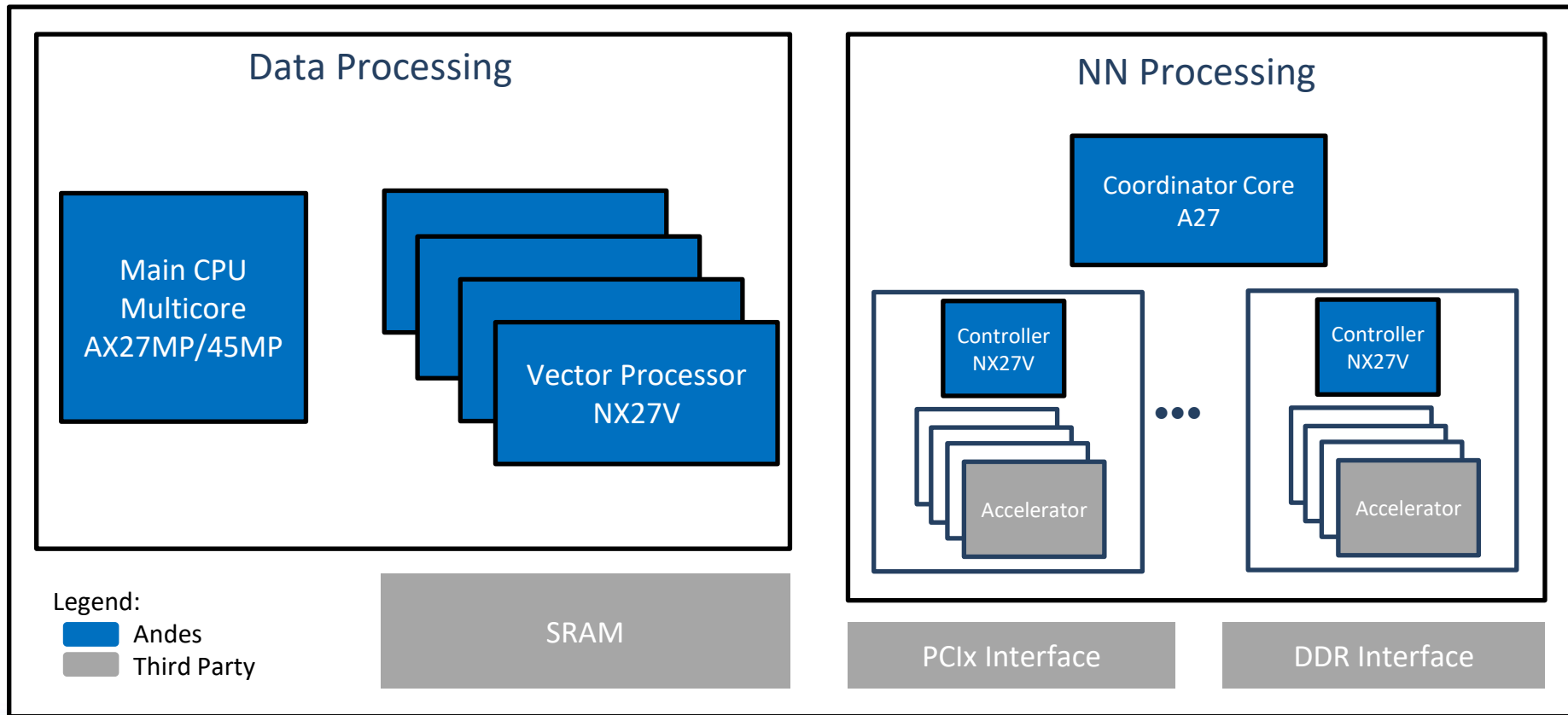Machine Learning for Key Word Spotting

Example of Edge Computing – Vision Processing

Pre-ISP Processing & Post Processing

Image/Video Analysis by using AI inference engine

Image Processing

Vector Processor
NX27V
VLEN=256b

NN Processing

Vector Processor
NX27V
VLEN=512b

Accelerator

AXI BUS / NOC

ISP

Control Core
A25MP

DMA

SRAM

Legend:
Andes
Third Party

DDR Interface

Other I/O

ISP Interface

Example of Cloud Computing - Datacenter

RISC-V

Added Value and contributed extensions
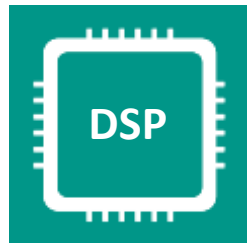
❖ Andes extensions to RISC-V

- Baseline ISA extension to speed up memory access and branches
- CoDense to reduce code size (12% better measured by GCC)
- PowerBrake to save power by stalling pipeline
- StackSafe HW stack protection
- vPLIC vectored dispatch and preemption(reduce 57% of latency)

❖ Powerful features to differentiate your products
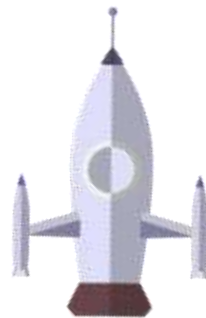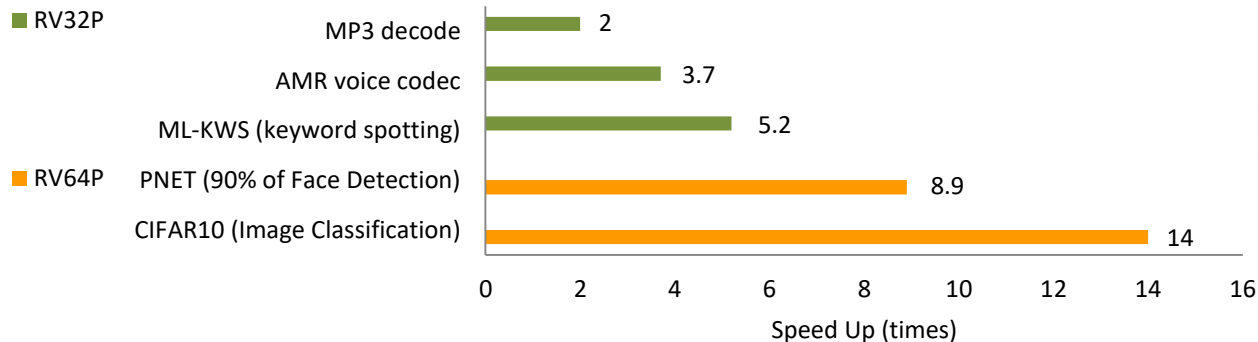❖ Create competitive edge for your systems

RISC-V DSP Extension (Packed SIMD/DSP)

- Andes contributed market-proven DSP(SIMD) as P-Extension
- Designed to accelerate slow video, audio/voice and low data rate DSP workloads

Real world speedup using P-Extension

	Speed Up (times)
RV32P MP3 decode	2
AMR voice codec	3.7
ML-KWS (keyword spotting)	5.2
RV64P PNET (90% of Face Detection)	8.9
CIFAR10 (Image Classification)	14

❖ Increase power efficiency to your DSP applications

Andes Custom Extension – EDA Tool

- ACE unlocks RISC-V's Potential of RISC-V DSA
  - Define ACE instructions to handle time critical codes
  - Another approach to co-processor or accelerators

- All-in-one **COPILOT** development environment
  - EDA Automation tool and ease of use
  - Extensions are easy to re-use, can be used as a library

AndesCore™ RISC-V Families
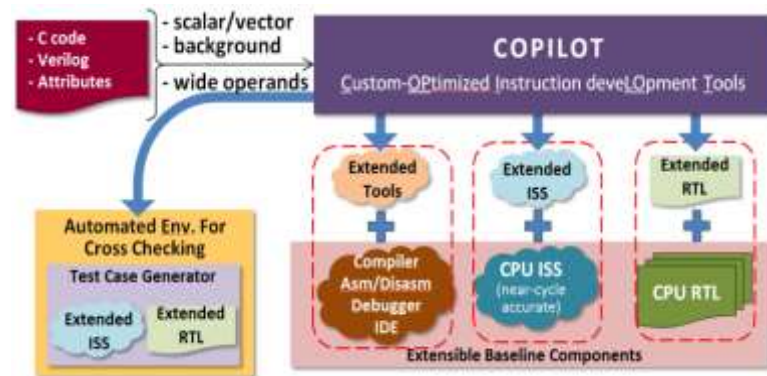
Fast and Compact /Slim and Efficient	DSP Extension	Linux with FPU/DSP	Cache-Coherent Multicores	
N(X)45 V5, Dual Issue, Superscalar, FPU, PMP	**D(X)45** N(X)45, FPU, DSP	**A(X)45** D45, **MMU**	**A(X)45MP** L2$, L1/IO coherence	**8-stage 1.2GHz***
NX27V 5-stage CPU 128/256/512b data width VPU		**A(X)27** **MemBoost**, MMU, DSP	**A(X)27MP** **MemBoost** ,L2$, L1/IO coherence	**5-stage 1.1GHz***
N(X□)25F V5/32&64b, FPU, PMP	**D25F** N25F, **DSP**	**A(X)25** N(X)25F, **MMU**, DSP	**A(X)25MP** L2$, L1/IO coherence	
N22 V5[e], 32/16 GPR				**2-stage 700MHz***

In Production
In Development

Features/Performance

□: X represents 64-bit CPU core
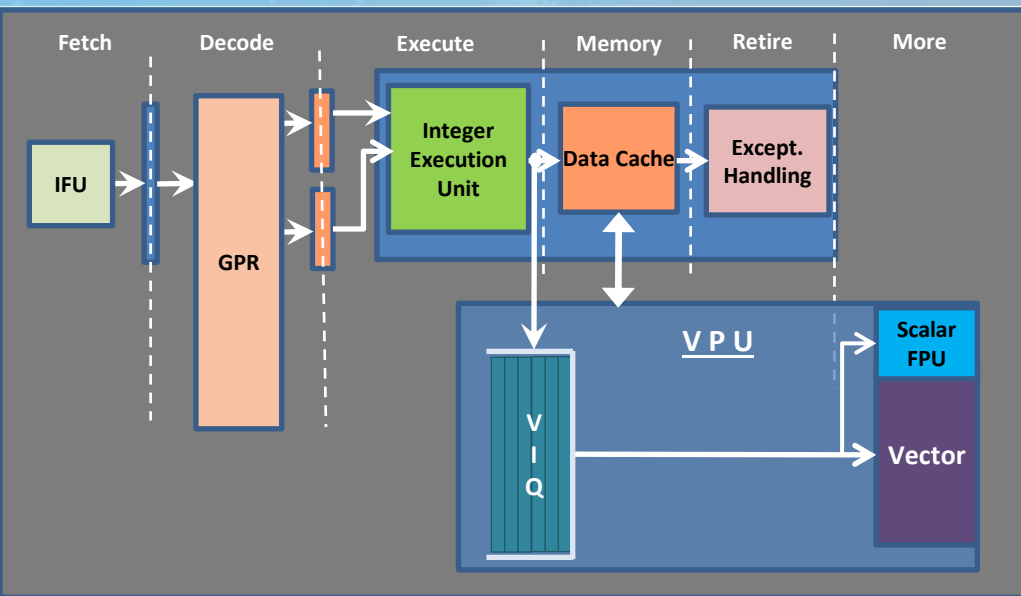*: TSMC 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

V-Series

Cray style, scalable vector processor

First RISC-V Vector Engine Shipped in Industry!

RVV v0.8 support*

AI optimized with BFloat16 & INT4

1GHz, $0.3mm^2$ in TSMC 7nm FF+

Configurable & scalable

- Vector length 128-bits to 512-bits
- Licensee configurable ALUs

Low power, simple to use

- Multi-level clock-gating
- In-order, 1R/W SRAM, cell based

> 50 VPU in < 10W Open Compute card

Core Overview

Some details

### From 2-stage over 5-stage to 8-stage

AndesCore™ 25 Series

- ❖ **32-bit and 64-bit cores**
- ❖ **AndeStar V5 architecture**:
  - RV-IMAC + Andes V5 Extensions
  - Optional: F/D and S-mode/MMU
- ❖ **5-stage pipeline, single-issue**
- ❖ **Configurable multiplier**
- ❖ **Optional branch prediction**
- ❖ **I/D caches and Local Memory**
  - Optional parity or ECC protection
  - Hit-under-miss caches
  - HW unaligned load/store accesses
- ❖ **Bus interface**
  - A master port (AHB, AXI, AXIx2)
  - An optional slave port (AHB)
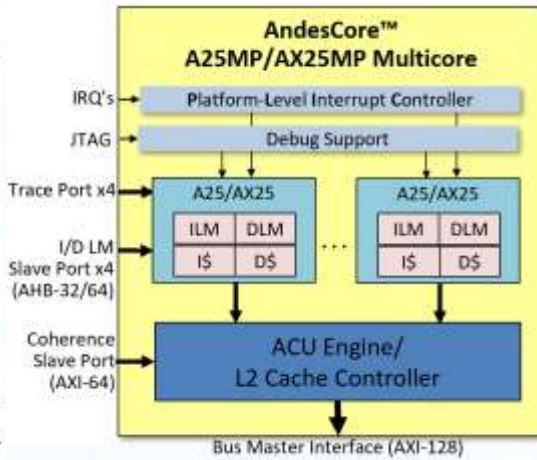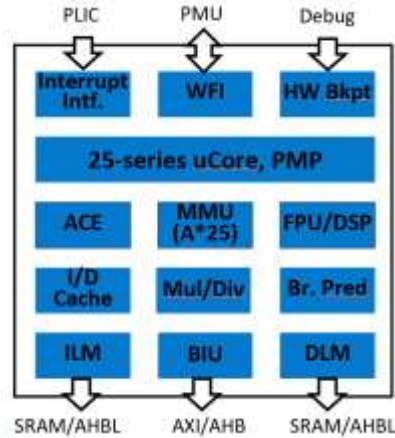
1~4 A25/AX25 CPUs:
- RV-IMACFD ISA + V5 extensions
- P-extension draft
- Supporting SMP Linux

Bus Interfaces
- LM slave port
- Coherence slave port
- AXI bus master interface
  - N:1 synchronous clock ratio

PLIC for interrupt handling

Debug/trace support

Andes Coherence Unit
- MESI cache coherence protocol
- Duplicate L1 dcache tags
- IO coherence for cacheless masters

L2 Controller
- Size: 128KB to 2MB
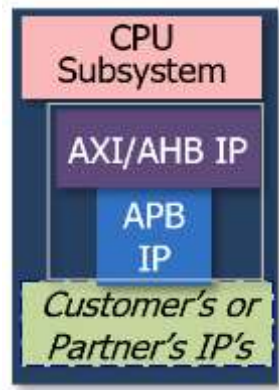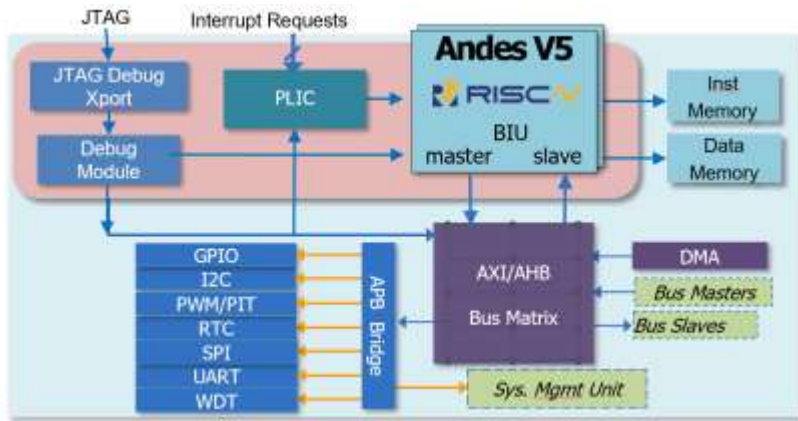
AndesCore™ 45 Series

- **8-stage in-order dual-issue**
- **AndeStar™ V5 ISA:**
  - RV*GCN (S/D FPU)
  - RV*P-ext (DSP/SIMD)
  - MMU: for Linux Applications
  - ALL have Andes extensions
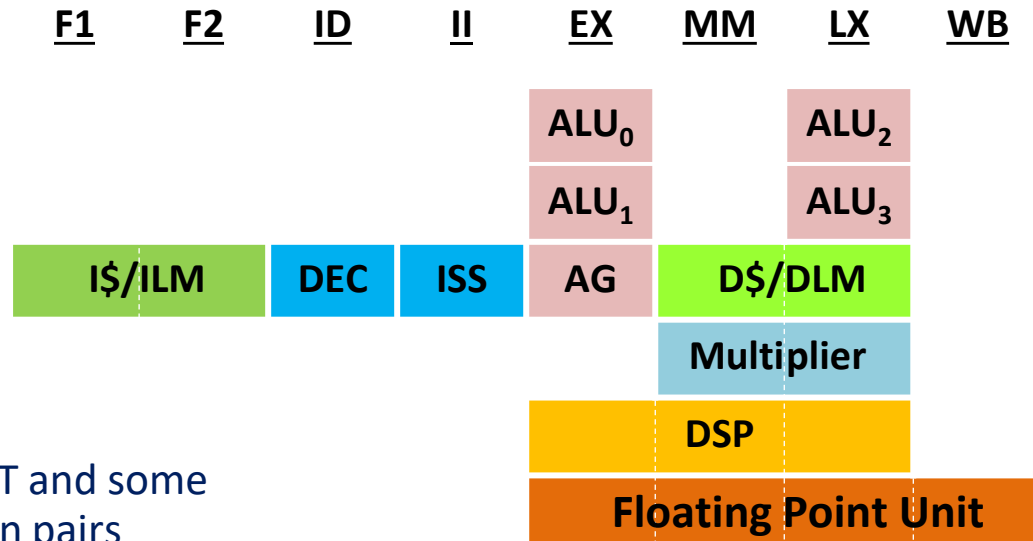- **Dual-issue most instruction pairs**
  - Except for 2 MUL/FPU/DSP/LD_ST and some special dependent ALU instruction pairs
  - Late ALUs enable 0-cycle load-use penalty
- **MemBoost** for memory subsystem
- **Low power dynamic branch prediction**
- **Unaligned data accesses**
- **Fast or small multiplier**

F1	**F2**	**ID**	**II**	**EX**	**MM**	**LX**	**WB**
				ALU_0		ALU_2	
				ALU_1		ALU_3	
I\$/ILM		DEC	ISS	AG	D\$/DLM		
					Multiplier		
				DSP			
				Floating Point Unit			

(\$/LM: 2nd cycle for alignment)

45-Series Pipeline

Time-to-Market

Get the whole set, IDE, Debug Probes, BSP's and Core IP

Complete Development Environment

- **AndeSight™ Feature-Rich IDE**

  Free Evaluation on SID and ICE target

- **AndeSoft™ Software Stack**

  Bare metal demo projects

  FreeRTOS ver10

  Linux

- **AndeShape™ Development Boards**

  Full-Featured ADP-XC7K

  Corvette-F1 Amazon FreeRTOS-qualified
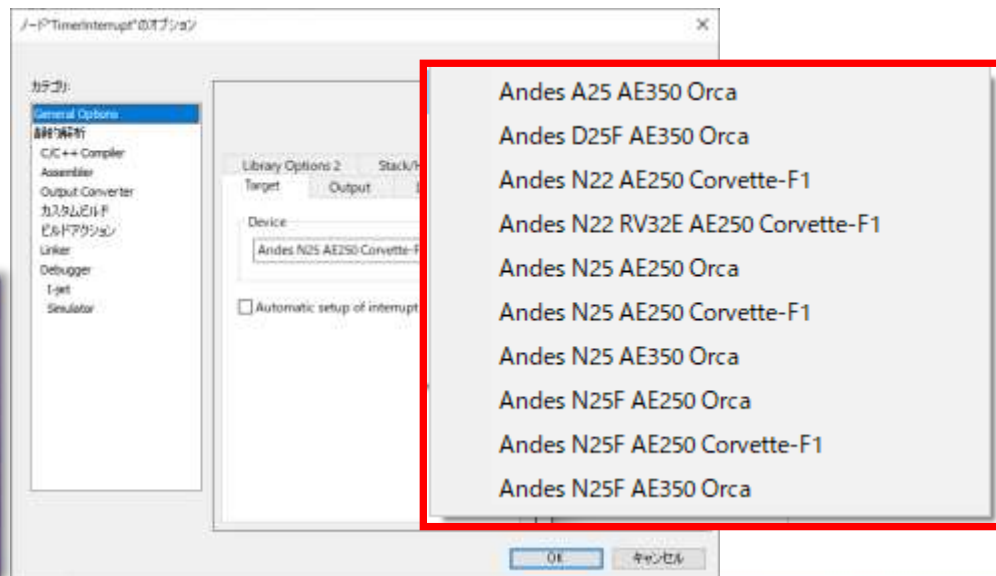

- **Debugging Hardware**

  AICE-MINI+, AICE-MICRO
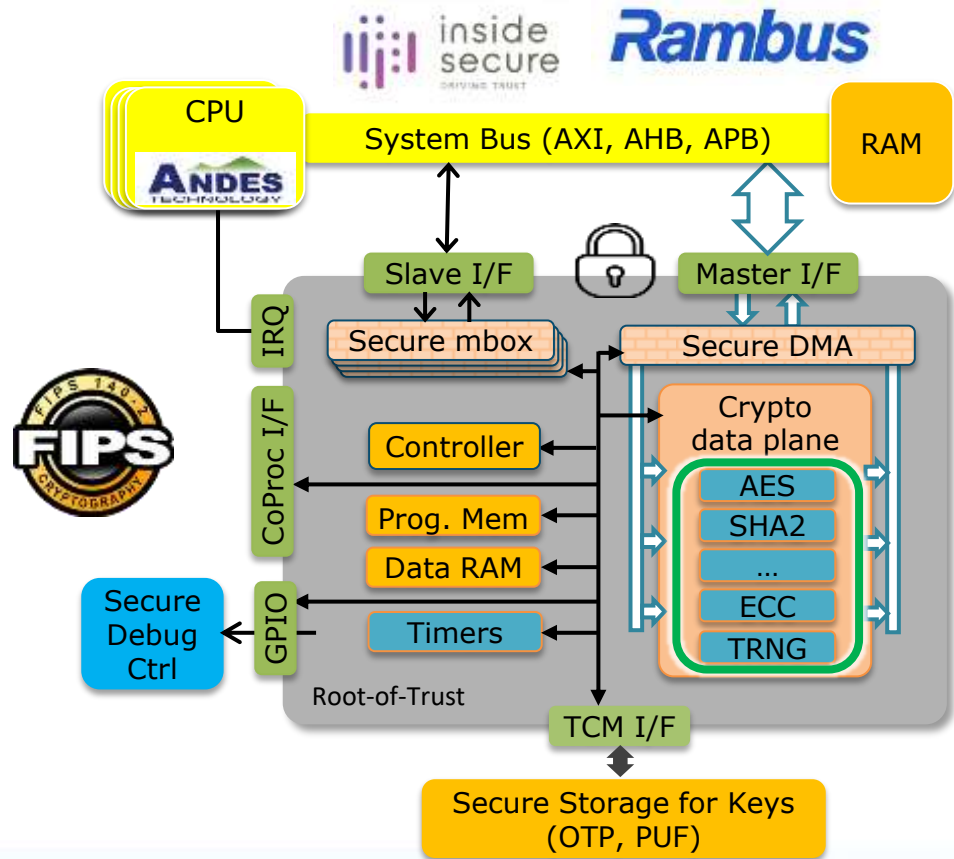
AndesCore™ Ecosystem - Tools

► IAR Embedded Workbench®

- Support RISC-V
- Support P-Extension (DSP/Packed-SIMD)
- excellent optimization technology
- static code analysis
- Extensive Debugging
  via I-jet probe

IDE	Debugger	Toolchain
Embedded Workbench	I-Jet ICE	Compiler
	C-SPY tool	C-STAT
		Functional Safety

Andes A25 AE350 Orca
Andes D25F AE350 Orca
Andes N22 AE250 Corvette-F1
Andes N22 RV32E AE250 Corvette-F1
Andes N25 AE250 Orca
Andes N25 AE250 Corvette-F1
Andes N25 AE350 Orca
Andes N25F AE250 Orca
Andes N25F AE250 Corvette-F1
Andes N25F AE350 Orca

Root-of-Trust Solution

Root-of-Trust

- **FIPS-140-2 Level 2 certified**
- **Secure Boot**
- **Side Channel Protection**
- **Anti-Tampering**
- **HW Protection for Keys**
- **TLS Device Authentication**
- **Secure DMA**
- **Secure Debug**

Summary

- RISC-V has built a strong ecosystem contributing technologies and innovations

- RISC-V keeps evolving through the collaborative community

- Andes is the only ONE provides P & V & custom extension framework to accelerate AI

- Commercialization, customization and user experience will be the three keys to succeed

JOIN RISC-V !
WORK WITH ANDES !