AI : RISC-V Linuxを使用したエッジ
→ サーバーへスケーリングするロードマップ

RISC-V Day Tokyo 2020

Florian Wohlrab

RISC-V Ambassador &

EMEA日本地域営業代表, アンデステクノロジ（台湾）06.Nov 2020

What Age Are We In

Agile Hardware Development
Accelerate chip development and commercial adoption

Agile

Improved Security
Prevent side channel attack for example

Security

John Hennessy and David Patterson Receive 2017 ACM A.M. Turing Award

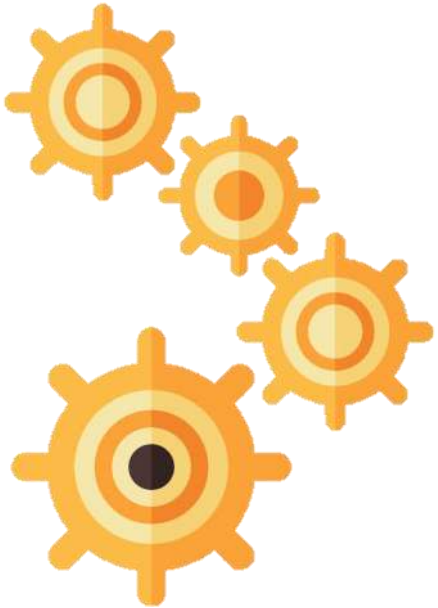
DSA

Domain-Specific Architectures
Tailored to a specific problem domain and offer significant performance/efficiency gains

Open ISA

Open ISA
Industry-standard open ISA

A New Golden Age for Computer Architecture



Source: https://www.acm.org/hennessy-patterson-turing-lecture

OPEN ISA RISC-V

- Open ISA inspired by the success of open source software - Linux for processors
- Greater competition drive quicker innovation
- Incredible ecosystem support

Active Roles in RISC-V International

Frankwell Lin, CEO
RISC-V
Board Member

Dr. Charlie Su, CTO
Vice Chair, Technical
Steering Committee

Florian Wohlrab
RISC-V
Ambassador

Who is Andes

Who We Are

Pure-play CPU IP Company

RISC-V Founding Premier Member

Taiwan Stock Exchange Listed TPE: 6533

Major Open-Source Contributor/Maintainer

Running Task Groups

Quick Facts

15 years old company

200+ Licensees Worldwide

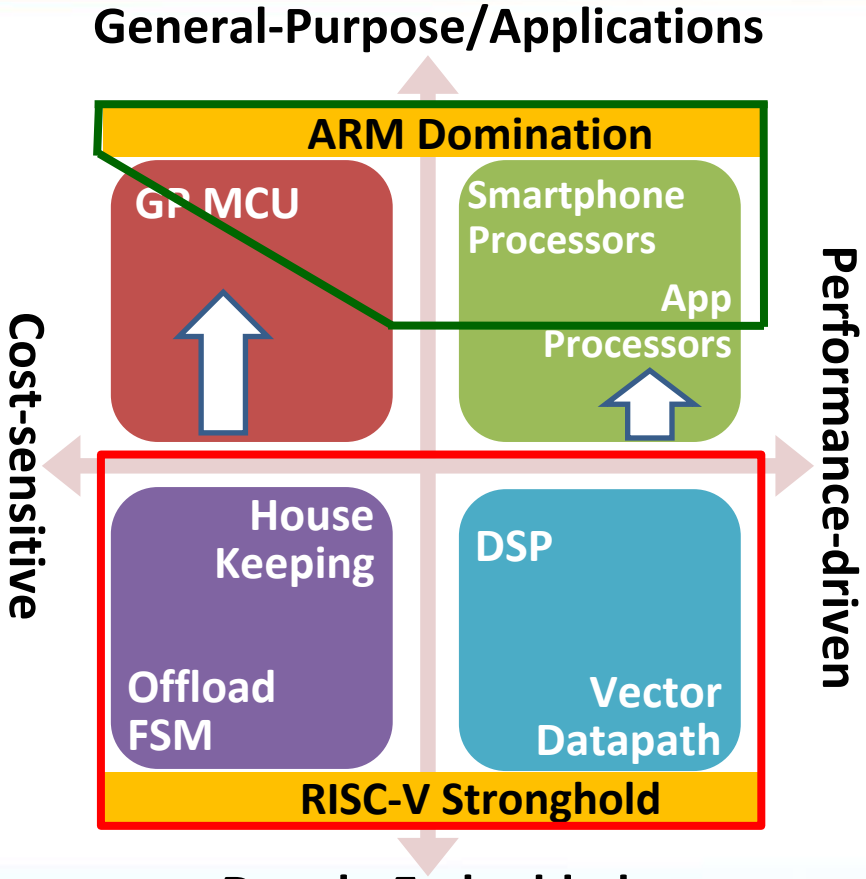
80% R&D employees

5B+ accumulated Andes-embedded SoC shipped

17K+ AndeSight IDE installation

RISC-V
Market adoption and usage examples

RISC-V Adoption: Applications TODAY



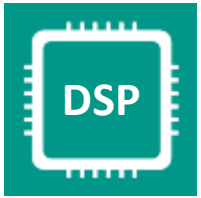
- Edge to Cloud
  - MCU
  - AIoT
  - Blockchain
  - Wireless (BT/WiFi)
  - 5G (macro/small Cells)
  - Datacenter AI Accellerators
  - ADAS
  - Storage
  - Touch
- Typical usage: 1 to 1000~ Cores
- Technology: 40nm to 7nm
- Driver: AI / ML

Andes RISC-V on Audio product

- D25F on LE Audio(BLE 5.2) for True Wireless Earbuds and Hearing Aids
  - Customer Tape out already!

  This product will be the one of the first SoCs supporting both of LE audio and Classic Audio

Bluetooth Baseband and Audio Subsystem	Application CPU	DSP/AI Accelerator
LC3 codec - high quality, low power LE Audio/BLE 5.2 – Multi-Stream, Broadcast Audio	**Power Efficient** – Excellent PPA **Mature Ecosystem** – Support various RTOSs **RISC-V DSP Extension** – outstanding performance DSP library	DSP Algorithm for Noise and Echo Cancelation Machine Learning for Key Word Spotting



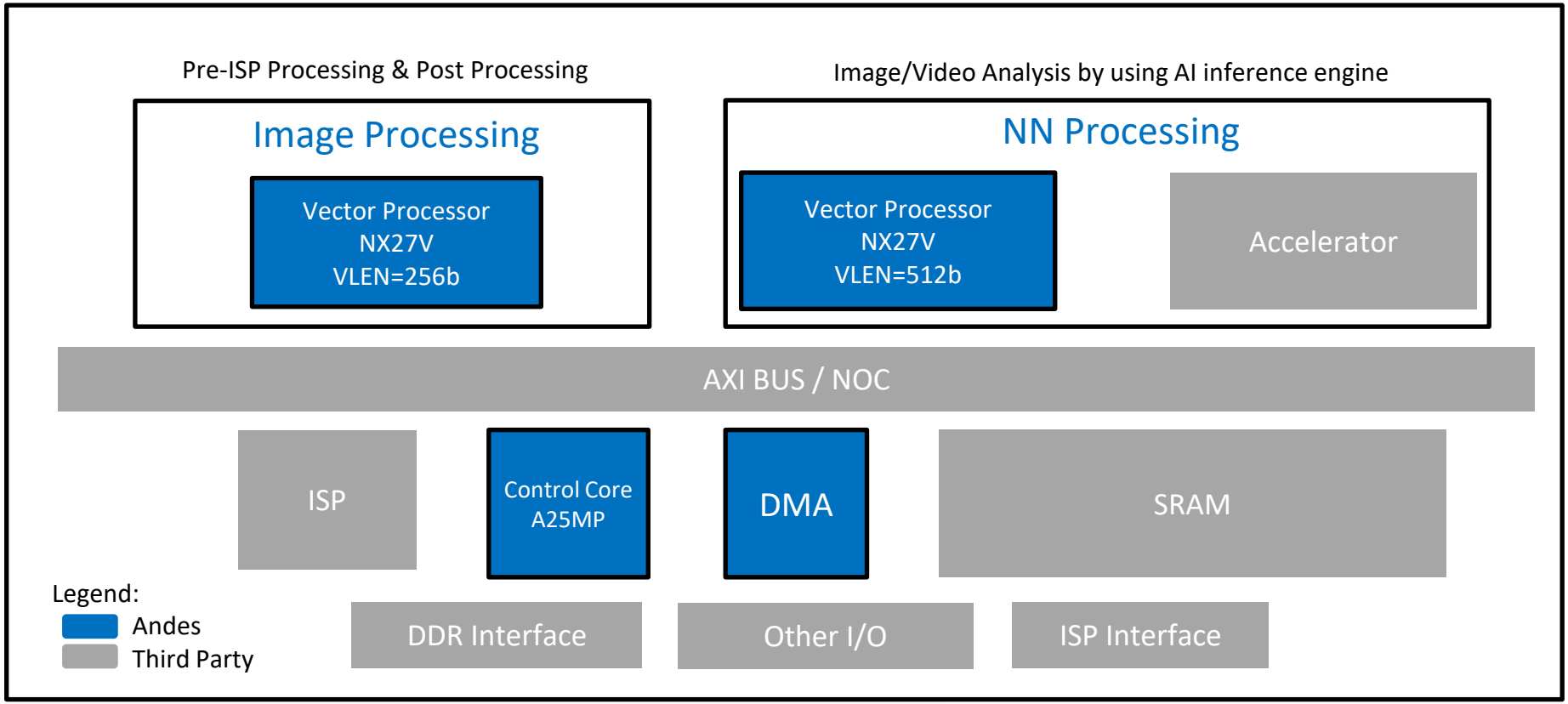
RISC-V Deployment – Renesas ASSP

RENESAS
BIG IDEAS FOR EVERY SPACE

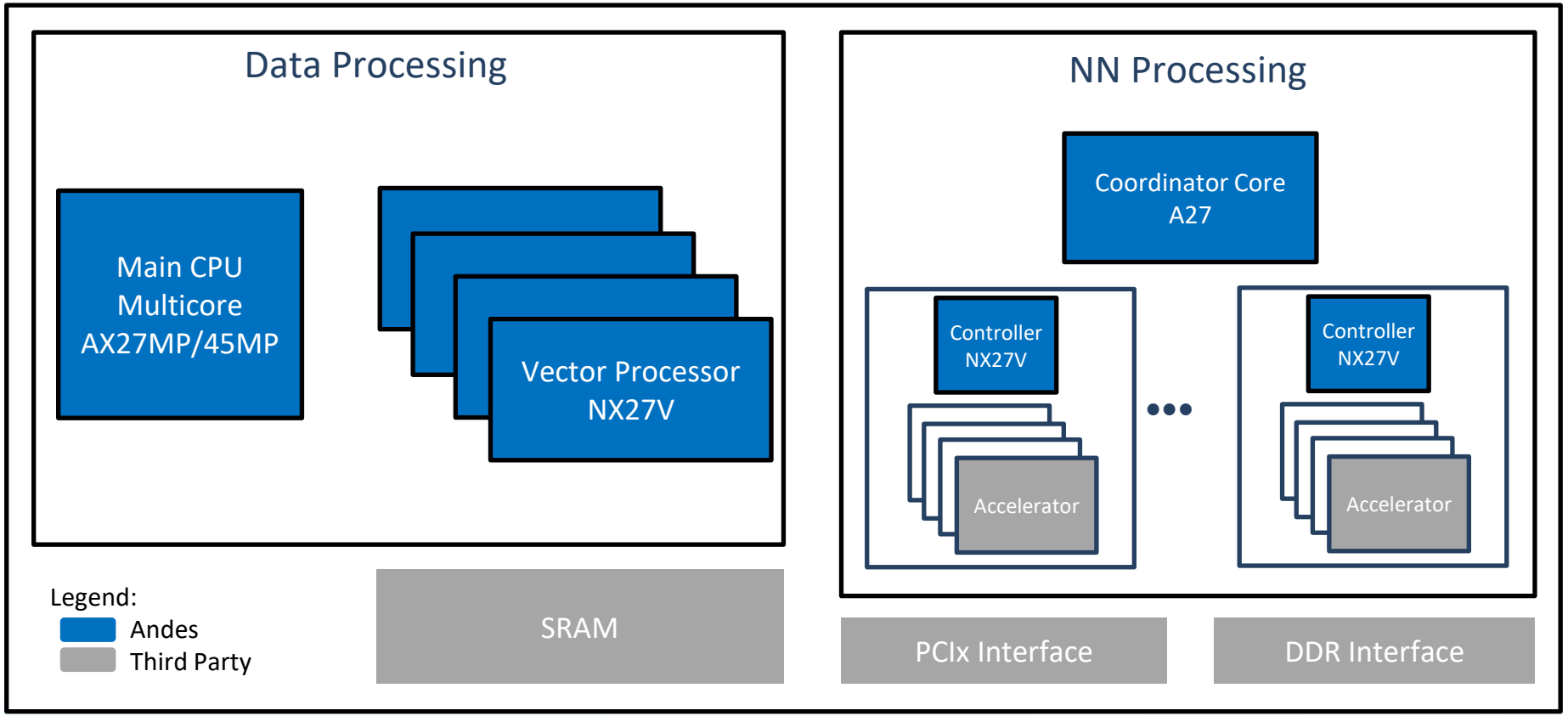
- ルネサス初のRISC-V搭載ASSPの開発に向けて、アンデス社のRISC-V 32ビットCPUコアを採用
- 2020年10月01日
  - ルネサス エレクトロニクス株式会社（CEO: 柴田　英利、以下ルネサス）は、このたびRISC-Vベースの組み込みCPUコアおよび関連するSoC（System on Chip）開発環境のトップサプライヤである**Andes Technology**（以下、アンデス社）との技術IP提携を発表します。ルネサスは、新たなASSP（Application Specific Standard Product）に、AndesCore™ IP 32ビットRISC-V CPUコアを組み込むことを決定し、2021年の下半期にサンプル提供を開始する予定です。

- **https://www.renesas.com/jp/ja/about/press-center/news/2020/news20201001.html**

Example of Edge Computing – Vision Processing



Example of Cloud Computing - Datacenter



RISC-V
Added Value and contributed extensions

Andes Added Value in RISC-V

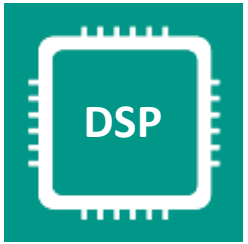
Andes extensions to RISC-V

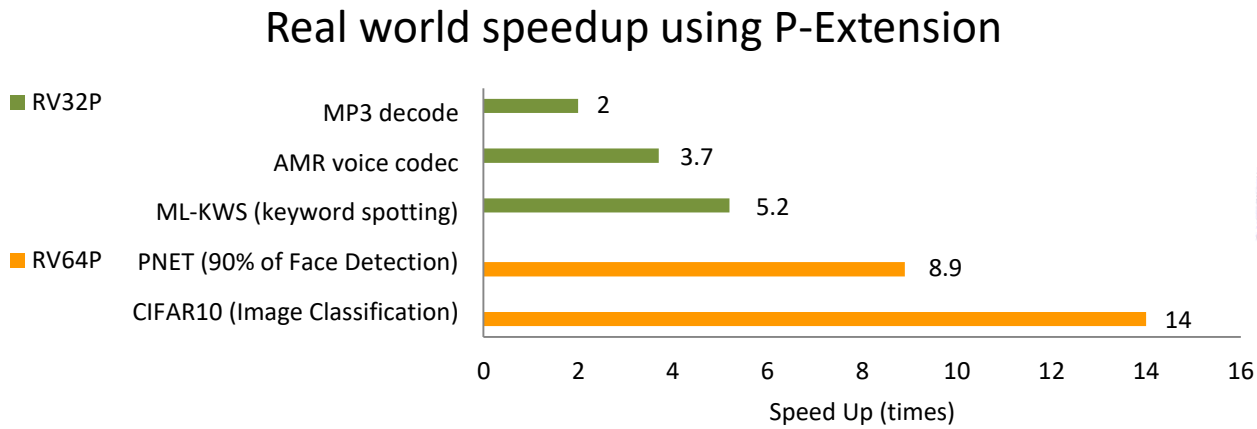
- Baseline ISA extension to speed up memory access and branches
- CoDense to reduce code size (12% better measured by GCC)
- PowerBrake to save power by stalling pipeline
- StackSafe HW stack protection
- vPLIC vectored dispatch and preemption(reduce 57% of latency)

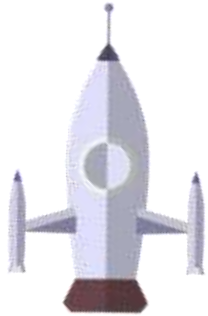
- Powerful features to differentiate your products
- Create competitive edge for your systems

RISC-V DSP Extension (Packed SIMD/DSP)

- Andes contributed market-proven DSP(SIMD) as P-Extension
- Designed to accelerate slow video, audio/voice and low data rate DSP workloads





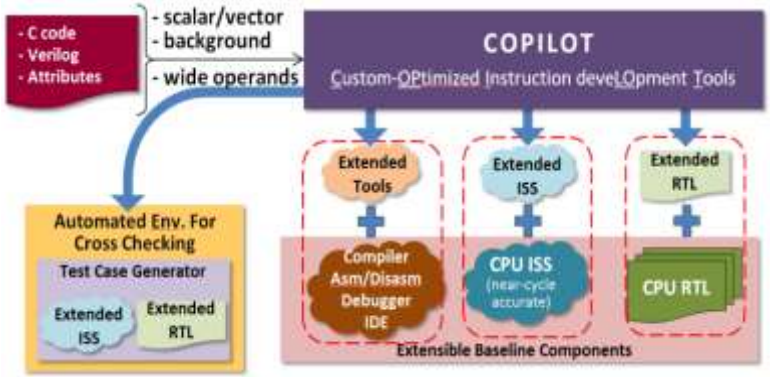


❖ Increase power efficiency to your DSP applications

Andes Custom Extension – EDA Tool

- ACE unlocks RISC-V's Potential of RISC-V DSA
  - Define ACE instructions to handle time critical codes
  - Another approach to co-processor or accelerators

- All-in-one **COPILOT** development environment
  - EDA Automation tool and ease of use
  - Extensions are easy to re-use, can be used as a library



AndesCore™ RISC-V Families

Fast and Compact /Slim and Efficient	DSP Extension	Linux with FPU/DSP	Cache-Coherent Multicores
N(X)45 V5, Dual Issue, Superscalar, FPU, PMP	**D(X)45** N(X)45, FPU, DSP	**A(X)45** D45, **MMU**	**A(X)45MP** L2$, L1/IO coherence
NX27V 5-stage CPU 128/256/512b data width VPU		**A(X)27** **MemBoost**, **MMU**, DSP	**A(X)27MP** **MemBoost** ,L2$, L1/IO coherence
N(X□)25F V5/32&64b, FPU, PMP	**D25F** N25F, **DSP**	**A(X)25** N(X)25F, **MMU**, DSP	**A(X)25MP** L2$, L1/IO coherence
N22 V5[e], 32/16 GPR			

In Production
In Development

Features/Performance

8-stage 1.2GHz*

5-stage 1.1GHz*

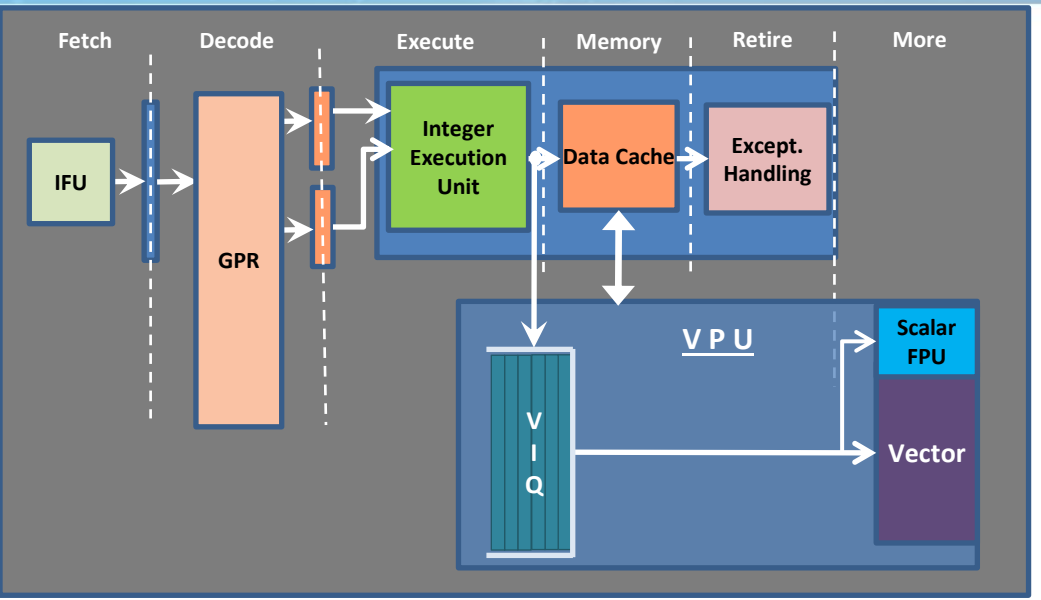
2-stage 700MHz*

□: X represents 64-bit CPU core
*: TSMC 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

V-Series

Cray style, scalable vector processor

First RISC-V Vector Engine Shipped in Industry!



RVV v0.8 support*

AI optimized with BFloat16 & INT4

1GHz, 0.3mm^2 in TSMC 7nm FF+

Configurable & scalable

- Vector length 128-bits to 512-bits
- Licensee configurable ALUs

Low power, simple to use

- Multi-level clock-gating
- In-order, 1R/W SRAM, cell based

> 50 VPU in < 10W Open Compute card

Linley MicroProcessor Report (MPR)
Email me for free copy: florian@andestech.com

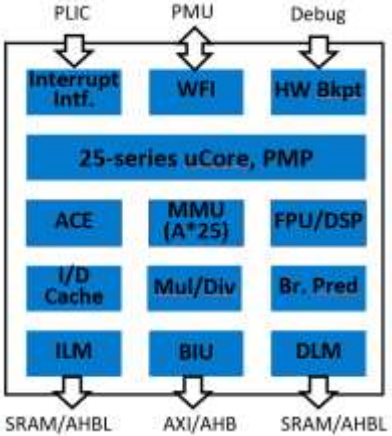
Core Overview

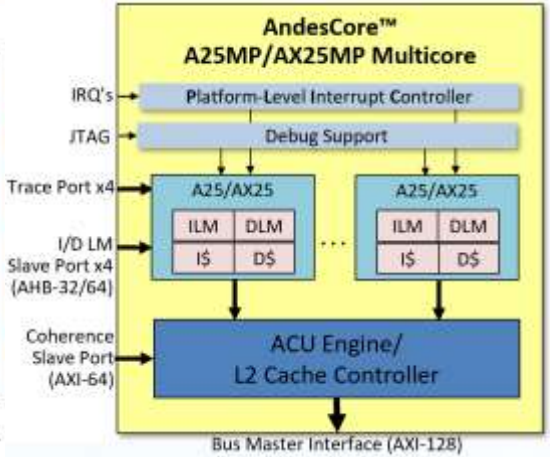
Some details

From 2-stage over 5-stage to 8-stage

AndesCore™ 25 Series

- **32-bit and 64-bit cores**
- **AndeStar V5 architecture**:
  - RV-IMAC + Andes V5 Extensions
  - Optional: F/D and S-mode/MMU
- **5-stage pipeline, single-issue**
- **Configurable multiplier**
- **Optional branch prediction**
- **I/D caches and Local Memory**
  - Optional parity or ECC protection
  - Hit-under-miss caches
  - HW unaligned load/store accesses
- **Bus interface**
  - A master port (AHB, AXI, AXIx2)
  - An optional slave port (AHB)





1~4 A25/AX25 CPUs:
- RV-IMACFD ISA + V5 extensions
- P-extension draft
- Supporting SMP Linux

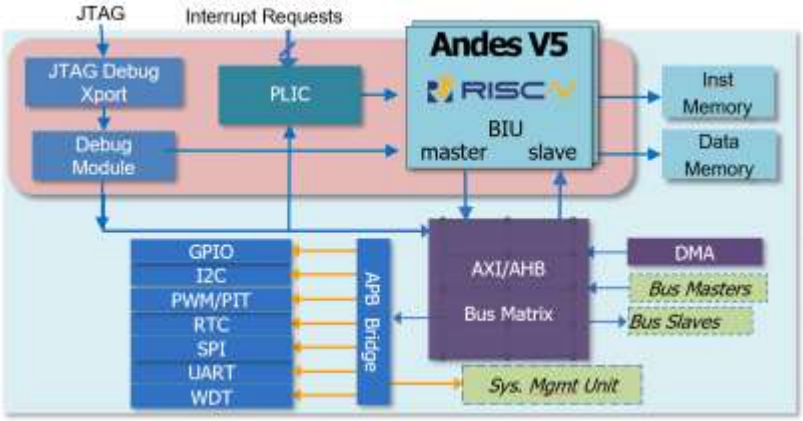
Bus Interfaces
- LM slave port
- Coherence slave port
- AXI bus master interface
  - N:1 synchronous clock ratio

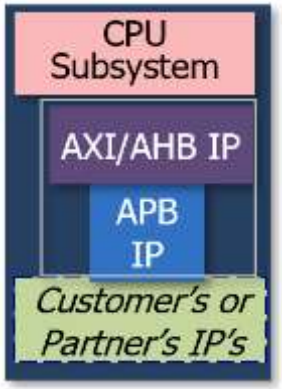
PLIC for interrupt handling

Debug/trace support

Andes Coherence Unit
- MESI cache coherence protocol
- Duplicate L1 dcache tags
- IO coherence for cacheless masters

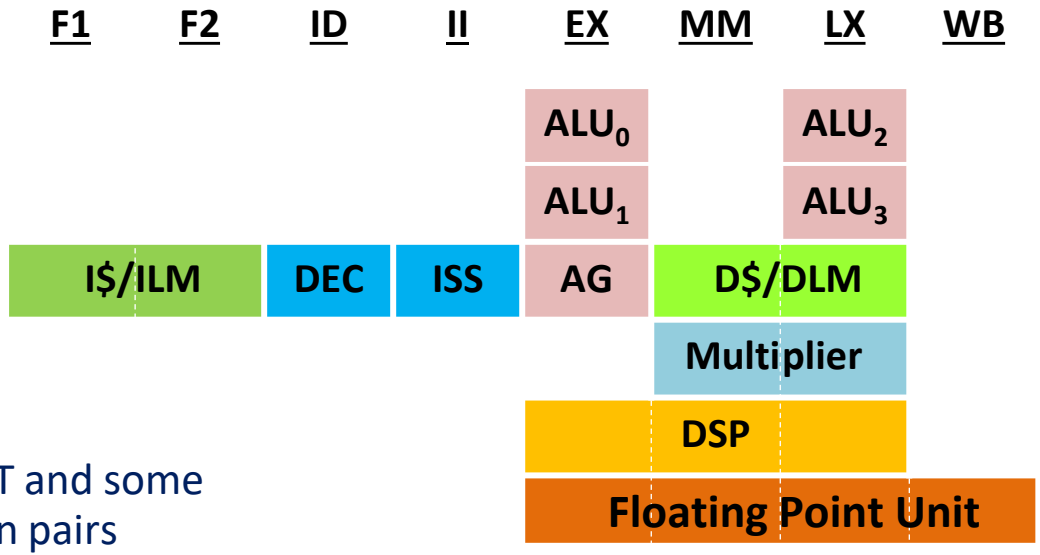
L2 Controller
- Size: 128KB to 2MB





AndesCore™ 45 Series

- **8-stage in-order dual-issue**
- **AndeStar™ V5 ISA:**
  - RV*GCN (S/D FPU)
  - RV*P-ext (DSP/SIMD)
  - MMU: for Linux Applications
  - ALL have Andes extensions
- **Dual-issue most instruction pairs**
  - Except for 2 MUL/FPU/DSP/LD_ST and some special dependent ALU instruction pairs
  - Late ALUs enable 0-cycle load-use penalty
- **MemBoost** for memory subsystem
- **Low power dynamic branch prediction**
- **Unaligned data accesses**
- **Fast or small multiplier**



($/LM: 2nd cycle for alignment)

45-Series Pipeline

Time-to-Market

Get the whole set, IDE, Debug Probes, BSP's and Core IP

Complete Development Environment

- **AndeSight™ Feature-Rich IDE**
  Free Evaluation on SID and ICE target

- **AndeShape™ Development Boards**
  Full-Featured ADP-XC7K
  Corvette-F1 Amazon FreeRTOS-qualified

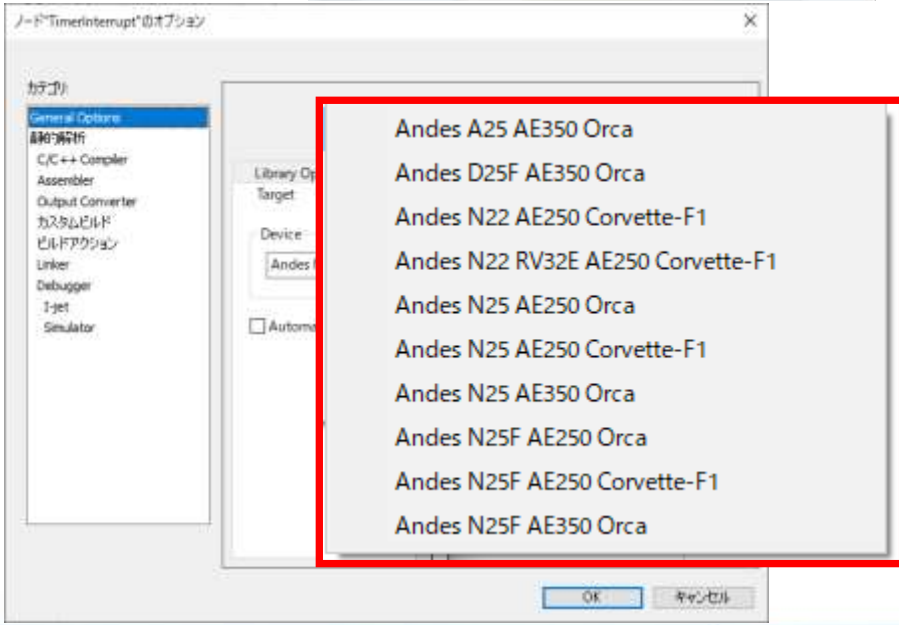
aws qualified device Amazon FreeRTOS

- **AndeSoft™ Software Stack**
  Bare metal demo projects
  FreeRTOS ver10
  Linux

- **Debugging Hardware**
  AICE-MINI+, AICE-MICRO

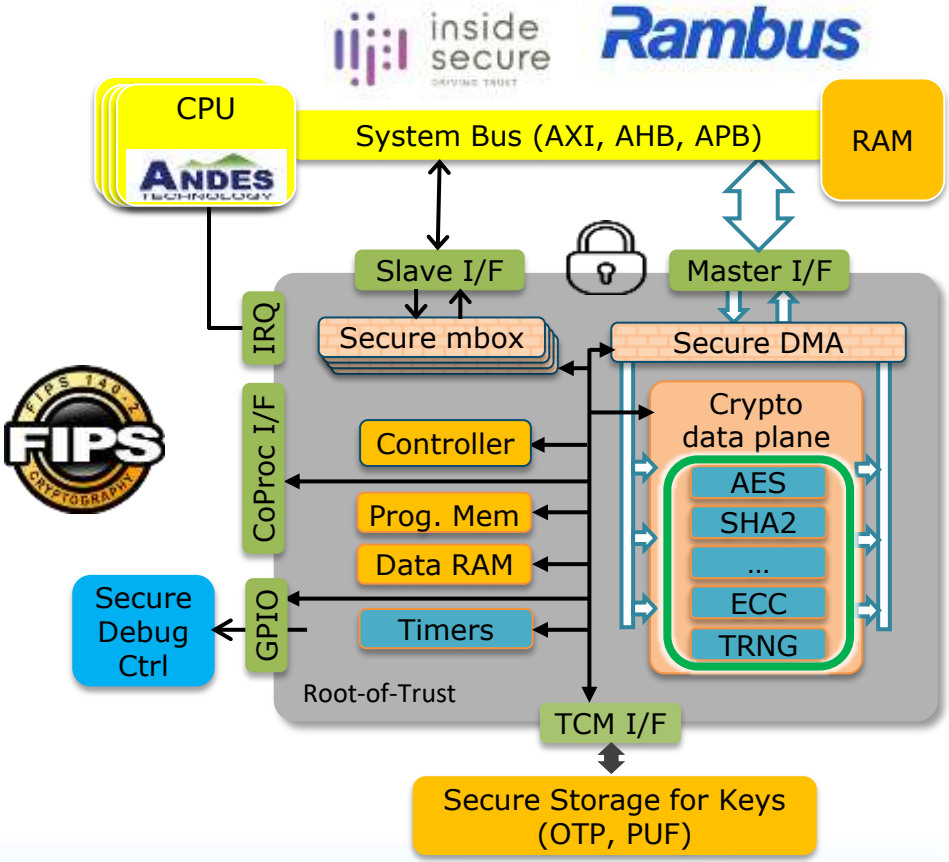
AndesCore™ Ecosystem - Tools

- IAR Embedded Workbench®
  - Support RISC-V
  - Support P-Extension (DSP/Packed-SIMD)
  - excellent optimization technology
  - static code analysis
  - Extensive Debugging
    via I-jet probe



IDE	Debugger	Toolchain
Embedded Workbench	I-Jet ICE	Compiler
	C-SPY tool	C-STAT
		Functional Safety

Root-of-Trust Solution



Root-of-Trust
FIPS-140-2 Level 2 certified
Secure Boot
Side Channel Protection
Anti-Tampering
HW Protection for Keys
TLS Device Authentication
Secure DMA
Secure Debug

Summary

- RISC-V has built a strong ecosystem contributing technologies and innovations
- RISC-V keeps evolving through the collaborative community
- Andes is the only ONE provides P & V & custom extension framework to accelerate AI
- Commercialization, customization and user experience will be the three keys to succeed

JOIN RISC-V !
WORK WITH ANDES !

Florian Wohlrab

RISC-V Day Tokyo 2020

www.andestech.com

ありがとうございました

THANK YOU

ANDES TECHNOLOGY

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RISC-V®