Ventana Founding Team Overview

Balaji Baktha
Founder and CEO

Greg Favor
Co-founder and Chief Architect

**Pioneer in Data Center semiconductors:
30+ years experience**

- World's first 64-bit ARM with Veloce (Acquired by AppliedMicro)
- Led Marvell BU delivering Data Center class Networking, Communications, Compute, Storage and Wireless infrastructure products
- World's first iSCSI with Platys, (Acquired by PMC-Sierra (Adaptec))

**One of the world's leading CPU architects:
35+ years experience**

- Architected K6 processor at startup NexGen, acquired by AMD
- Chief Architect at Siara Systems, acquired by RedBack
- Architected first successful 64-bit ARM CPU

Founded in 2019 by industry veterans with a proven track record of delivering Data Center class processors

arm   Qualcomm   Apple   SAMSUNG   intel.   AMD   digital   NVIDIA.   IBM   AMPERE   Transmeta CORPORATION   Sun microsystems

Ventana: Leadership in Action

1. Performance Leadership

2. Contribution to the RISC-V International Community

Member of Board of Directors	Balaji Baktha
Vice-Chair of Technical Steering Committee	Greg Favor
Chair of Privileged Architecture Standing Committee	Greg Favor
Chair of Platforms Horizontal Sub-Committee	Kumar Sankaran
Chair of CacheOps Task Group	David Kruckemyer
Chair of Marketing Events Committee	Omar Hassen
Vice-Chair of Debug Task Group	Paul Donahue
Co-author of Advanced Interrupt Architecture	Greg Favor
Chair of Hypervisor SIG	Anup Patel
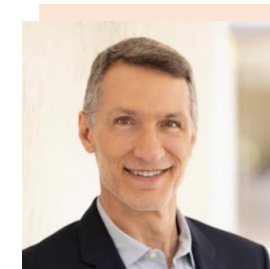
Greg Favor

'21 RVI BoD Technical Leadership Award
'20 RVI BoD Technical Contributor Award

Anup Patel

'22 RVI BoD Technical Leadership Award

3. Driving the RISC-V Software Ecosystem...

Founding Member of RISE to Ensure RISC-V Software Readiness

RISE
RISC-V Software Ecosystem

Mission

- Accelerate the development of open source software for RISC-V

- Raise the quality of RISC-V Platform software implementations

- Push the RISC-V Software ecosystem forward and align partners' efforts

- Ensure RISC-V is a tier 1 platform for all tools and libraries

- Accelerate RISC-V adoption for Client and above segments

VENTANA   Google   intel   SAMSUNG

MEDIATEK   NVIDIA   Qualcomm   Red Hat

Ventana: The Leading RISC-V & Chiplet Company

THECHANNELCO.
CRN®
CELEBRATING 40 YEARS

Jan '23:
Ventana placed among AMD, Nvidia, Intel, Qualcomm, and Arm as a Top 10 Semis To Watch for 2nd year in row

10 Hot Semiconductor Companies To Watch In 2023

BY DYLAN MARTIN ▶

JANUARY 28, 2023, 10:00 AM EST

CRN breaks down 10 semiconductor companies that are driving the market with new innovations — or are on the verge of doing so — while navigating the tough economic environment.

- Most Recognized High Performance RISC-V Leader

- One of the Best CPU Teams in the world

- World-Class RISC-V CPU Product and Roadmap

- Pioneered Chiplet based Productization and Business Model

- Strong Customer Traction in Data Center, Automotive and Mobile Client Markets

- Led the way in Defining and Creating a Robust Server Class Platform and Software Ecosystem, driving Mobile Ecosystem

- Co-founded RISE with Andes, Google, Imagination, Intel, Mediatek, nVidia, Qualcomm, Red Hat, Rivos, Samsung, SiFive, and T-head

- One of the most influential companies at RISC-V International at the Board of Directors, Technical and Marketing Committees

GSA Where Leaders Meet

Invited Speaker on How RISC-V & Chiplets

DATA CENTER WORLD
INNOVATION challenge
WINNER

Most Influential Founding Team

SmartNICs SUMMIT

Invited Speaker on RISC-V in Data Center

The Six Five SUMMIT

2x Presenter at Thought Leadership Conference

Ventana: High-Performance RISC-V Leadership

- Highest Socket Performance

- Highest Single Thread Performance; significantly better than closest RISC-V competitor

- Easily portable across process nodes

Highest Performance RISC-V Competitive with x86 and Arm

Complete Platform Solution

- Founding member of RISE

- Complete reference design ready today

- Complete open-source software stack optimized for Veyron V1

Pioneered Chiplets for Rapid Productization

Custom Domain Specific Acceleration

- Drastic reduction in Dev Time and Cost:
  IP model: ~3 years & $100M+
  Chiplet: ~1 year & $25M

- UCIe based D2D interconnect

- Core (5/3nm) and Uncore (12/16nm) chiplets implemented in optimal process nodes to maximize yield and cost
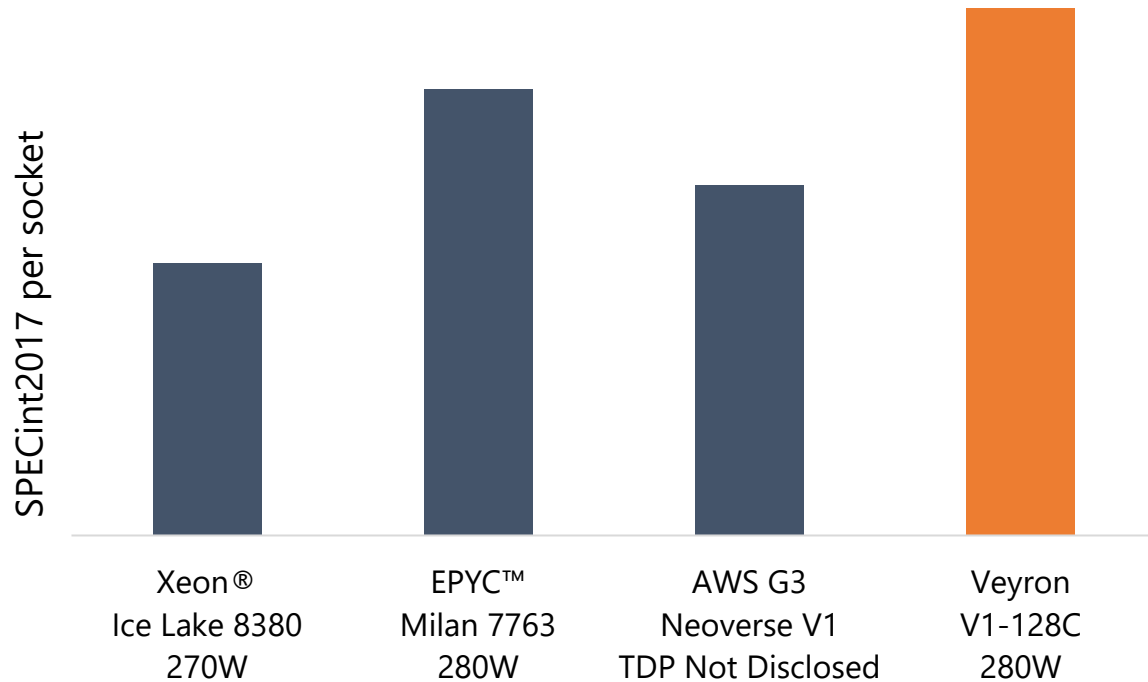
- Customer innovation through extensible architecture

- Multi-chiplet Heterogenous Architecture

# Veyron V1: World's First Data Center Class RISC-V Processor

Highest Performance RISC-V CPU

3.6GHz in 5nm process technology

Bar chart — Y axis: SPECint2017 per socket

Category	
Xeon® Ice Lake 8380 270W	
EPYC™ Milan 7763 280W	
AWS G3 Neoverse V1 TDP Not Disclosed	
Veyron V1-128C 280W	

ASSP Based on High Performance Chiplet Architecture

Significant reduction in development Time and Cost compared to prevailing monolithic SoC model

Launched December 2022 | 2nd Generation Underway | 2+ Year Lead vs Followers
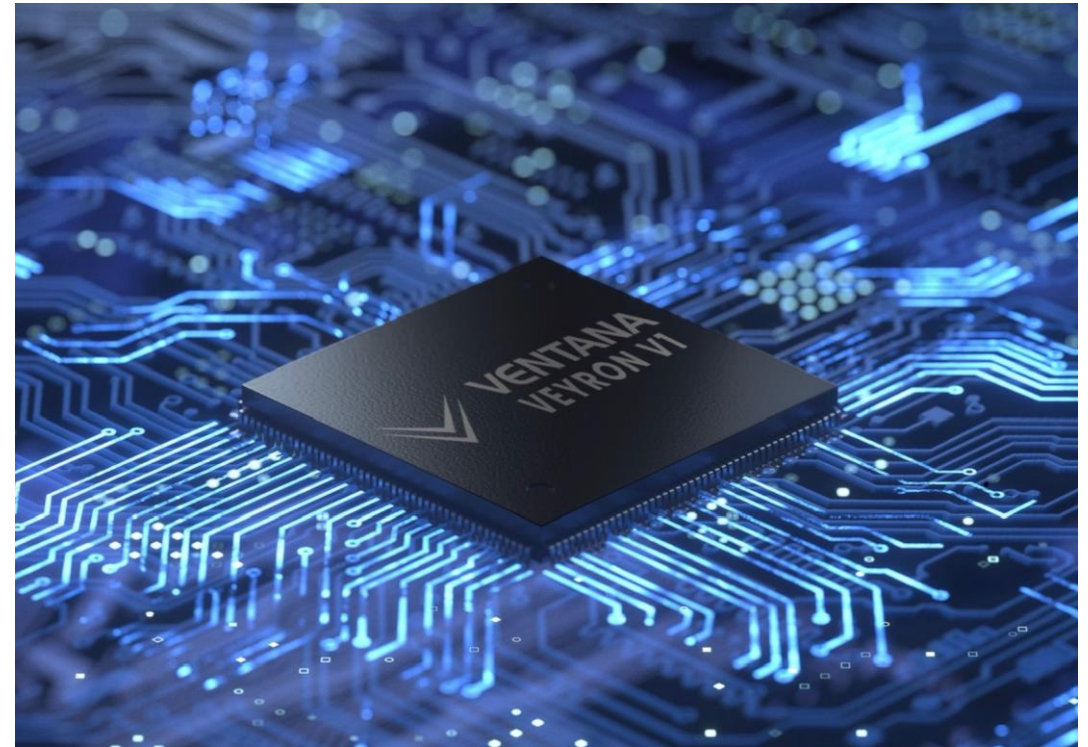
The Semiconductor Innovator's Dilemma

- Semiconductors are the foundation of the modern economy
- Unrelenting massive semiconductor consolidation since 2008
- Led to monopoly in each of the semi markets
- Average lifecycle of products is extended from 18 months to 3 years due to the lack competition
- No room for innovation and differentiation
  - OEMs are forced to use silicon from limited sources
- OEMs cannot build their own SoCs
  - Very high development cost: $100-200M per project
  - Incumbent ISAs don't allow them to innovate
- How do you break the cycle?

Dilemma to Opportunity!
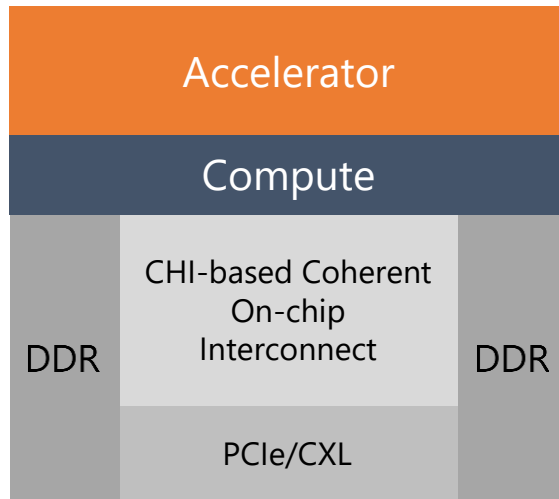
Monolithic SoC

- **TTM: 3+ years**
- **Development cost: $100M+**
- Leading edge process node
- Fixed performance
- Large die/high unit cost
- Risk of incorrect definition by time it comes to market
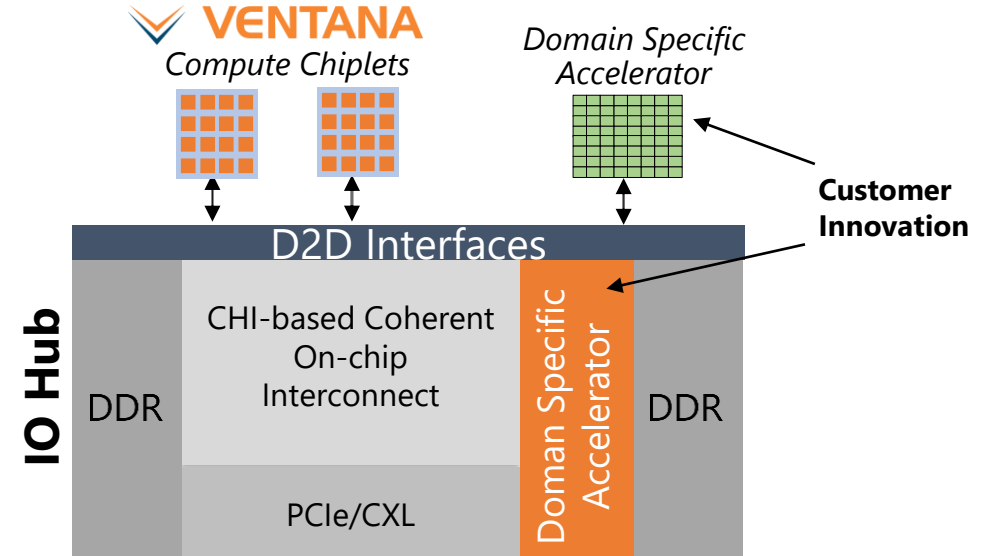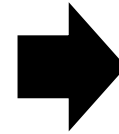
Chiplet-based SoC

- **TTM: ~1 year**
- **Development cost: < $25M**
- Each chiplet in optimal process node
- Scalable Compute, Accelerator and I/O performance
- Cost optimized solution
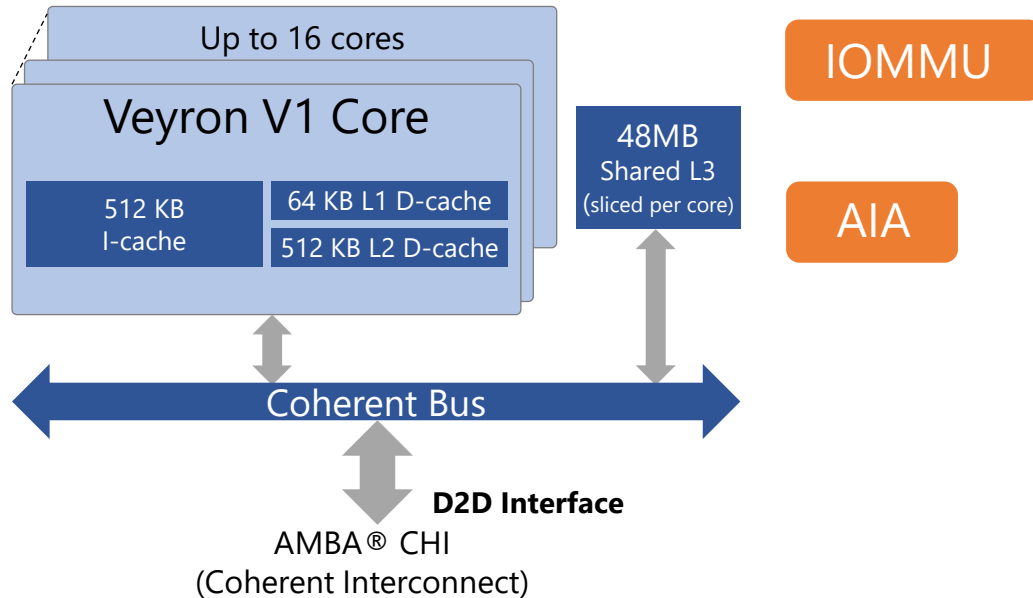- Chiplets introduce the concept of late binding and scalability

The Ventana Solution

Resurgence of Semiconductor Innovation: RISC-V + Chiplets

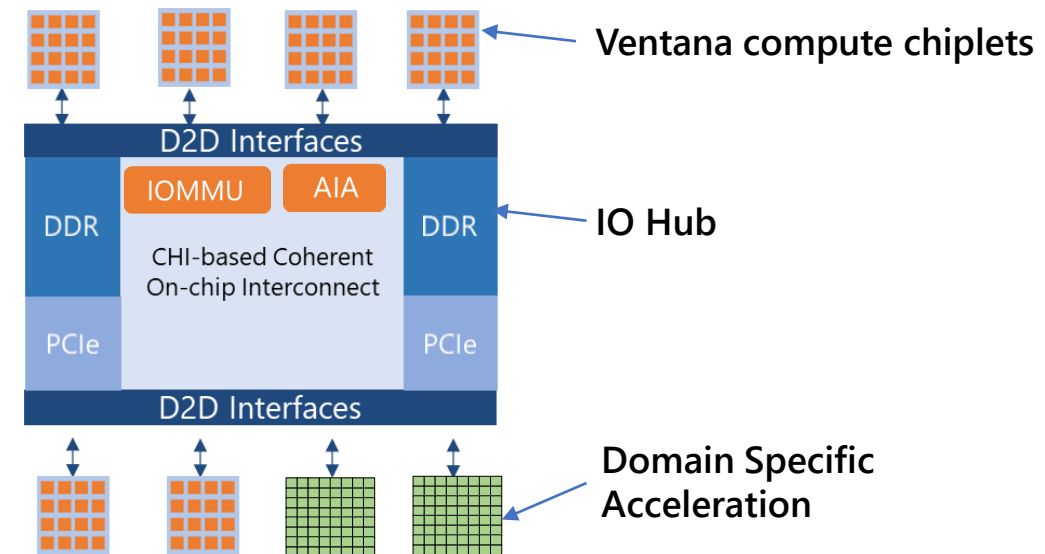**Automotive** **Data Center** **Generative AI at the Edge** **Client**

- Zonal architectures are a compelling opportunity to innovate and differentiate with Veyron Chiplets and Cores in ADAS, Infotainment (IVI), and Telemetry
    - Automotive-class RAS, Functional Safety and Security
    - Rapidly developing Software ecosystem and toolchain
    - UCIe for Automotive
- Sovereign Data Centers with Security & User Privacy
- Explosive use cases of Generative AI at the Edge

Ventana Veyron: Server Class RISC-V IP + Chiplets
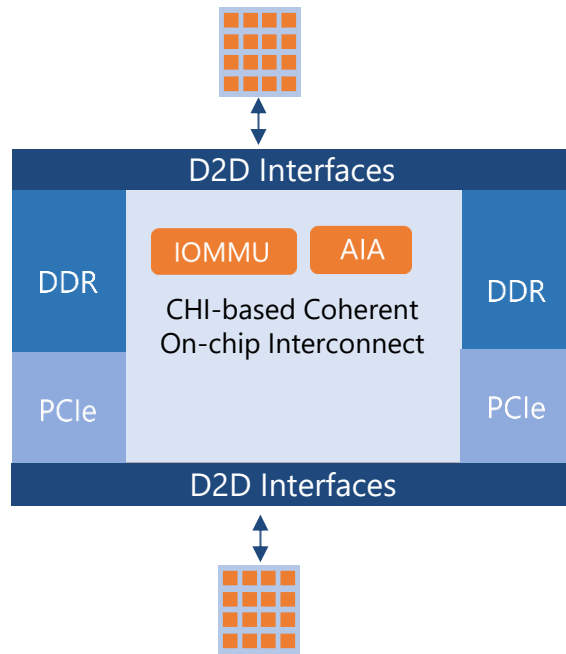
Veyron High Performance RISC-V CPU IP

Up to 16 cores

Veyron V1 Core

| 512 KB I-cache | 64 KB L1 D-cache |
| | 512 KB L2 D-cache |

48MB Shared L3 (sliced per core)

IOMMU

AIA

Coherent Bus

D2D Interface
AMBA® CHI
(Coherent Interconnect)

Veyron Chiplet Solutions

D2D Interfaces

DDR

IOMMU   AIA

CHI-based Coherent On-chip Interconnect

PCIe

DDR

PCIe

D2D Interfaces

Ventana compute chiplets

IO Hub

Domain Specific Acceleration

- Eight wide, aggressive out-of-order instruction pipeline
- High core count multi-cluster scalability (Up to 192 cores)
- Advanced side channel attack mitigations
- Comprehensive RAS features
- IOMMU & Advanced Interrupt Architecture (AIA) system IP

- Veyron compute chiplets
  - In latest process node technology
  - Scalable CPU performance/count
- IO Hub
  - Implemented in process node of choice
  - Customized for application requirements
- Custom Domain Specific Acceleration
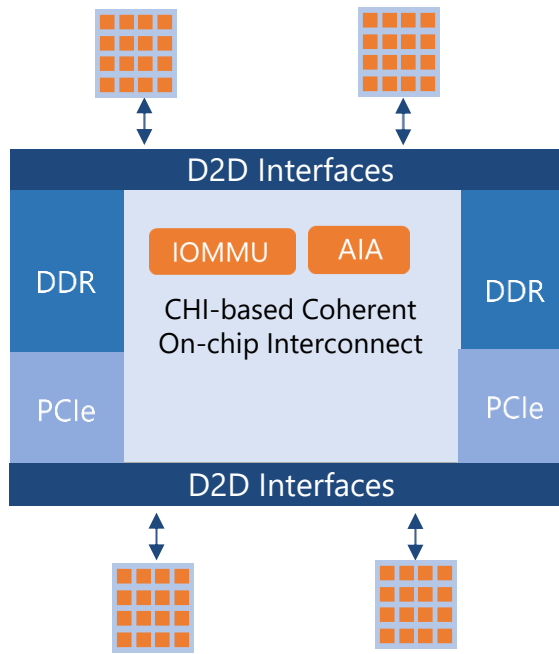 - Low-cost process node
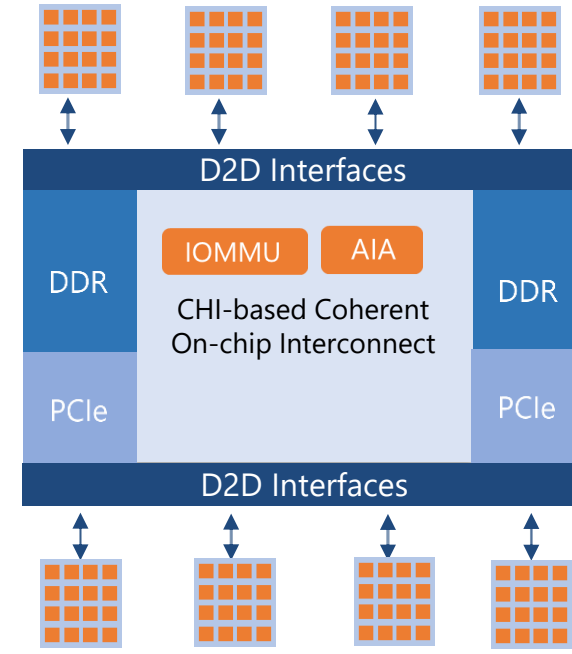
Scalable Architecture for Server-class Compute

Entry level server

D2D Interfaces

DDR	IOMMU	AIA	DDR
PCIe	CHI-based Coherent On-chip Interconnect		PCIe

D2D Interfaces

2 chiplets (32 cores)

Mid level server

D2D Interfaces

DDR	IOMMU	AIA	DDR
PCIe	CHI-based Coherent On-chip Interconnect		PCIe

D2D Interfaces

4 chiplets (64 cores)

High end server

D2D Interfaces

DDR	IOMMU	AIA	DDR
PCIe	CHI-based Coherent On-chip Interconnect		PCIe

D2D Interfaces

8-12 chiplets (128-192 cores)

Realizing Efficient Chiplet D2D PHY

Requirements

- Power efficient
- Small area overhead
- High data rates

|	PCIe Gen5	BoW-Fast
Power Efficiency pJ/bit	7	0.55
Area Density Tbps/mm2	0.1	0.69

Parallel D2D interconnects such as UCIe or BoW offer much lower power, area, and complexity overhead compared to serial/ SERDES based solutions like PCIe

D2D Refinement Required for Automotive

- Failure predictability through monitoring
- Detection & reporting of failures

Example Parallel D2D Interconnect:
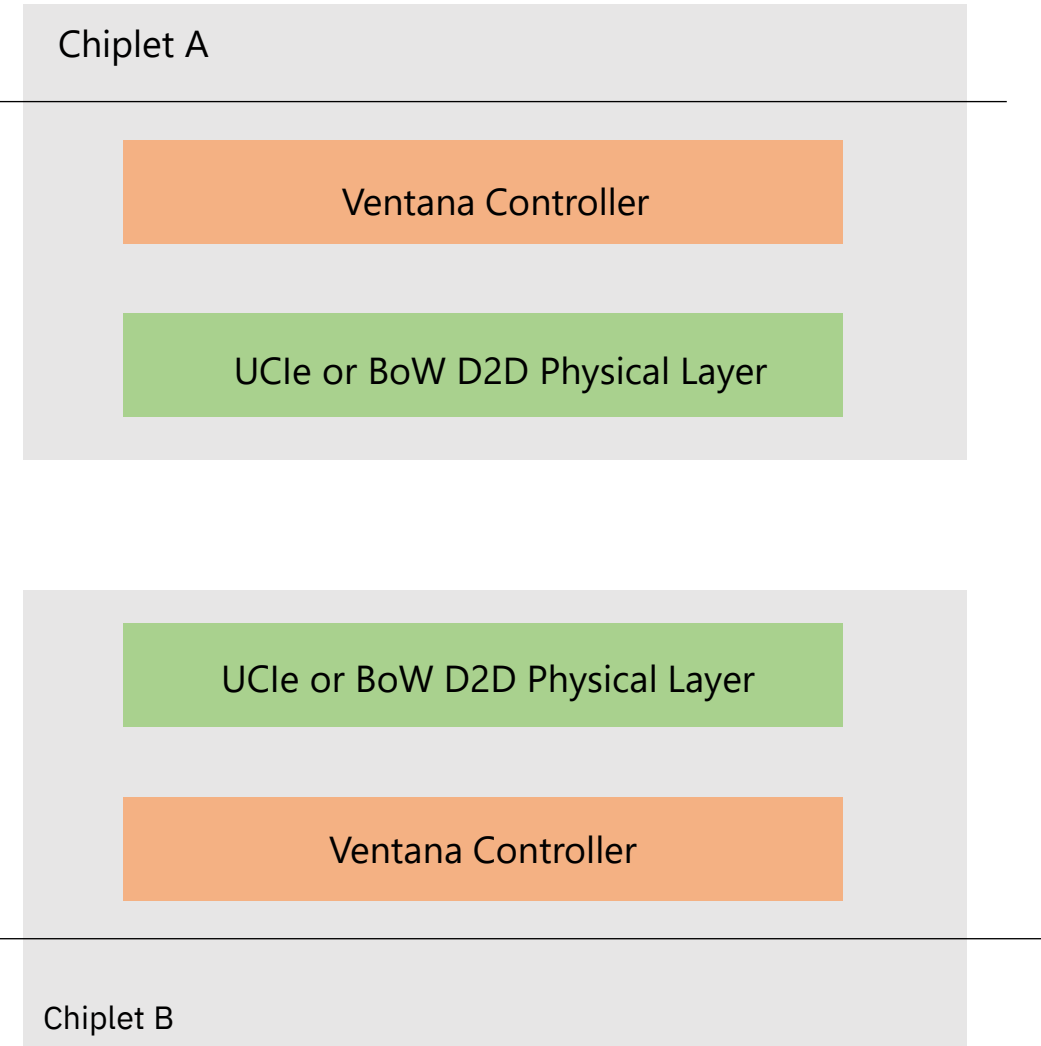BoW Minimal Bidirectional Refence Link
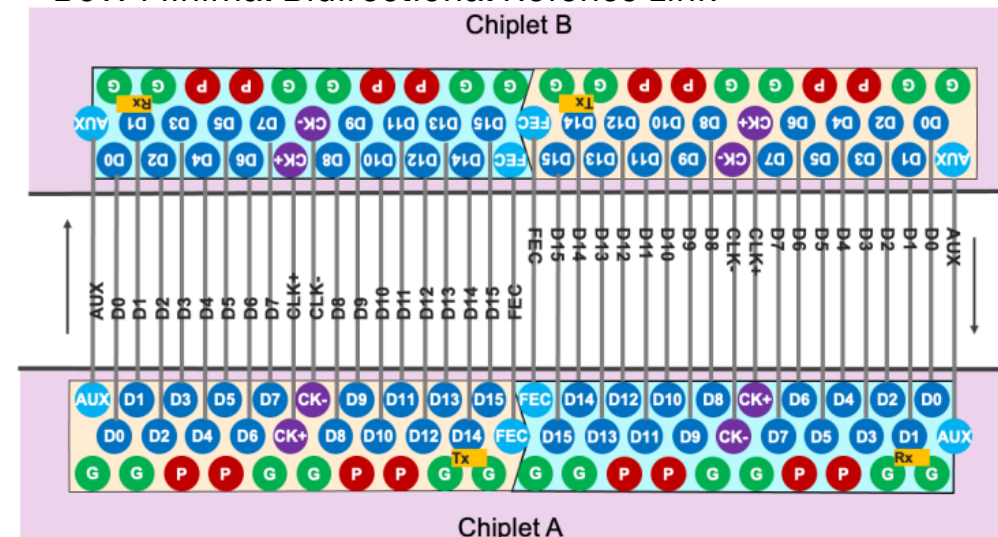
Pioneering Efficient Chiplet Interconnect Controller

Requirements

- Low D2D latency
- Predictable memory performance
- Standard SoC buses and networks must map easily to D2D transport
  - CHI, AXI, …
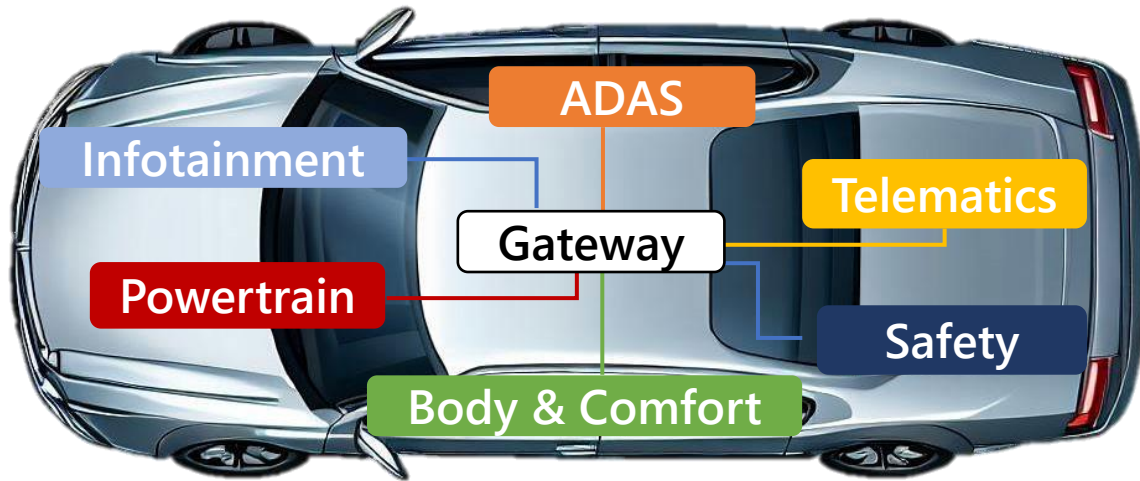- HW memory coherency for efficient support of accelerators

< 7ns latency vs 100ns+ for PCIe

**Ventana has developed a low latency controller IP which maps standard, coherent SoC buses to D2D PHY**

Chiplet A

Ventana Controller

UCIe or BoW D2D Physical Layer

UCIe or BoW D2D Physical Layer

Ventana Controller

Chiplet B

Automotive Following Server Architecture

Today: Domain Architecture

- ADAS
- Infotainment
- Telematics
- Gateway
- Powertrain
- Safety
- Body & Comfort

Future: Zonal Architecture

- Zonal Gateway
- Central Compute
- Zonal Gateway
- Zonal Gateway
- Gateway
- Telematics
- Zonal Gateway
- Zonal Gateway
- Zonal Gateway

- Dedicated, lower performance controllers
- Increasing hardware varieties
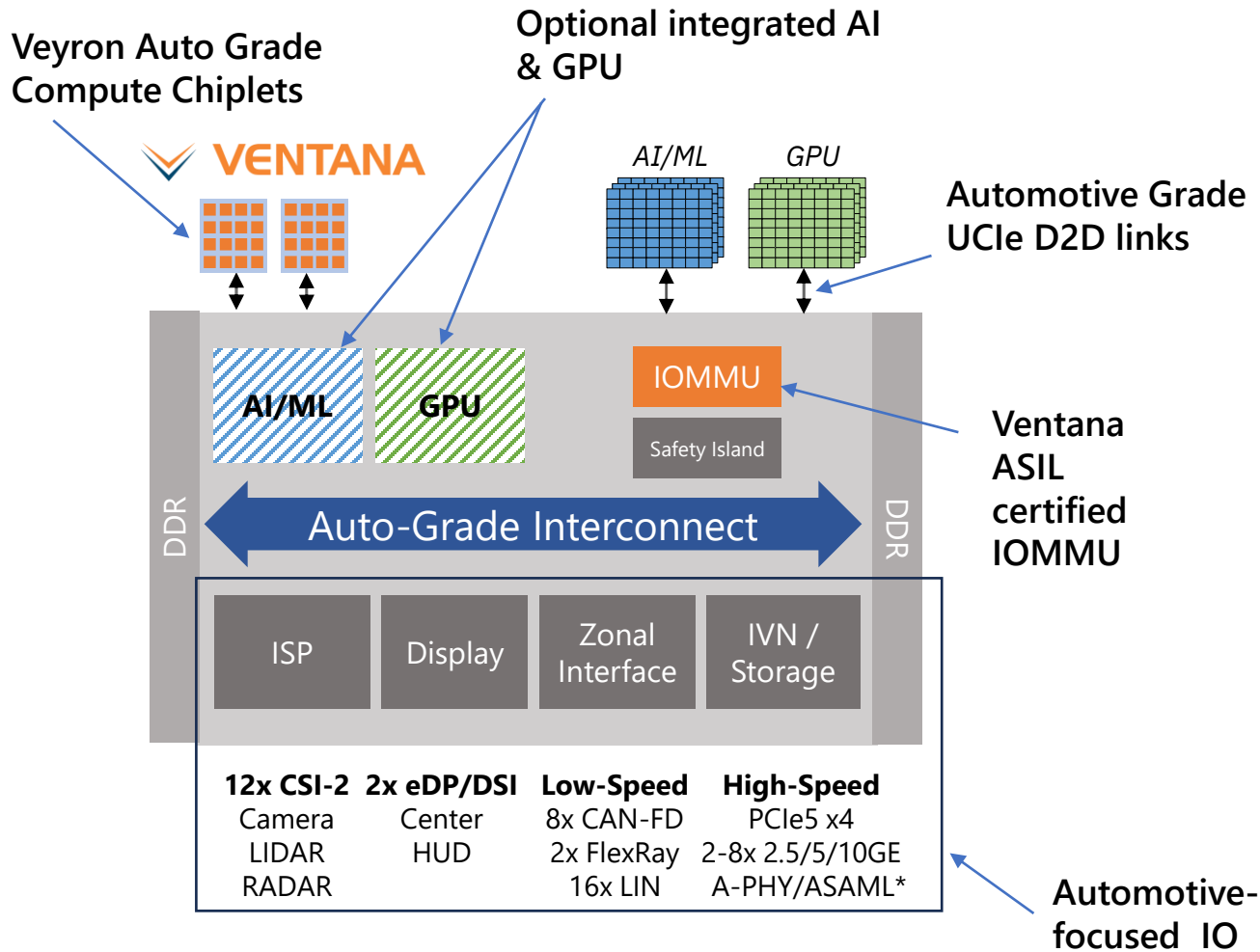- Fragment code development environments
- Not easily upgraded or scaled
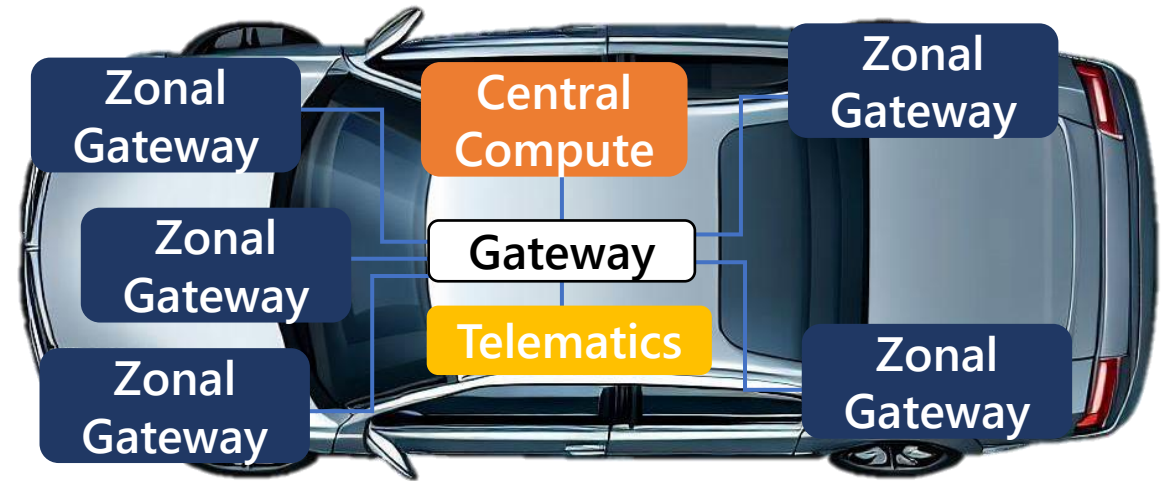
- Centralized high-performance compute
- Unified software environment
  - Automotive-class RAS, Functional Safety and Security
  - Rapidly developing Software ecosystem and toolchain
  - UCIe for Automotive
- Efficient development
- Scalable and easy to develop hardware

Same RISC-V + Chiplets concept applies

RISC-V and Chiplets Driving Innovation in Automotive

Veyron Auto Grade
Compute Chiplets

VENTANA

Optional integrated AI
& GPU

AI/ML   GPU

Automotive Grade
UCIe D2D links

AI/ML   GPU

IOMMU

Safety Island

Ventana
ASIL
certified
IOMMU

DDR   Auto-Grade Interconnect   DDR

ISP   Display   Zonal
Interface   IVN /
Storage

12x CSI-2	2x eDP/DSI	Low-Speed	High-Speed
Camera	Center	8x CAN-FD	PCIe5 x4
LIDAR	HUD	2x FlexRay	2-8x 2.5/5/10GE
RADAR		16x LIN	A-PHY/ASAML*

Automotive-
focused IO

- Automotive can benefit from same cost efficient chiplet architectures to create differentiated platforms
- Ventana ASIL certified chiplets and IP
- Partners create automotive Hub
- Accelerators can be integrated in Hub or scaled up in chiplets

Ventana Veyron Optimized Software Stack
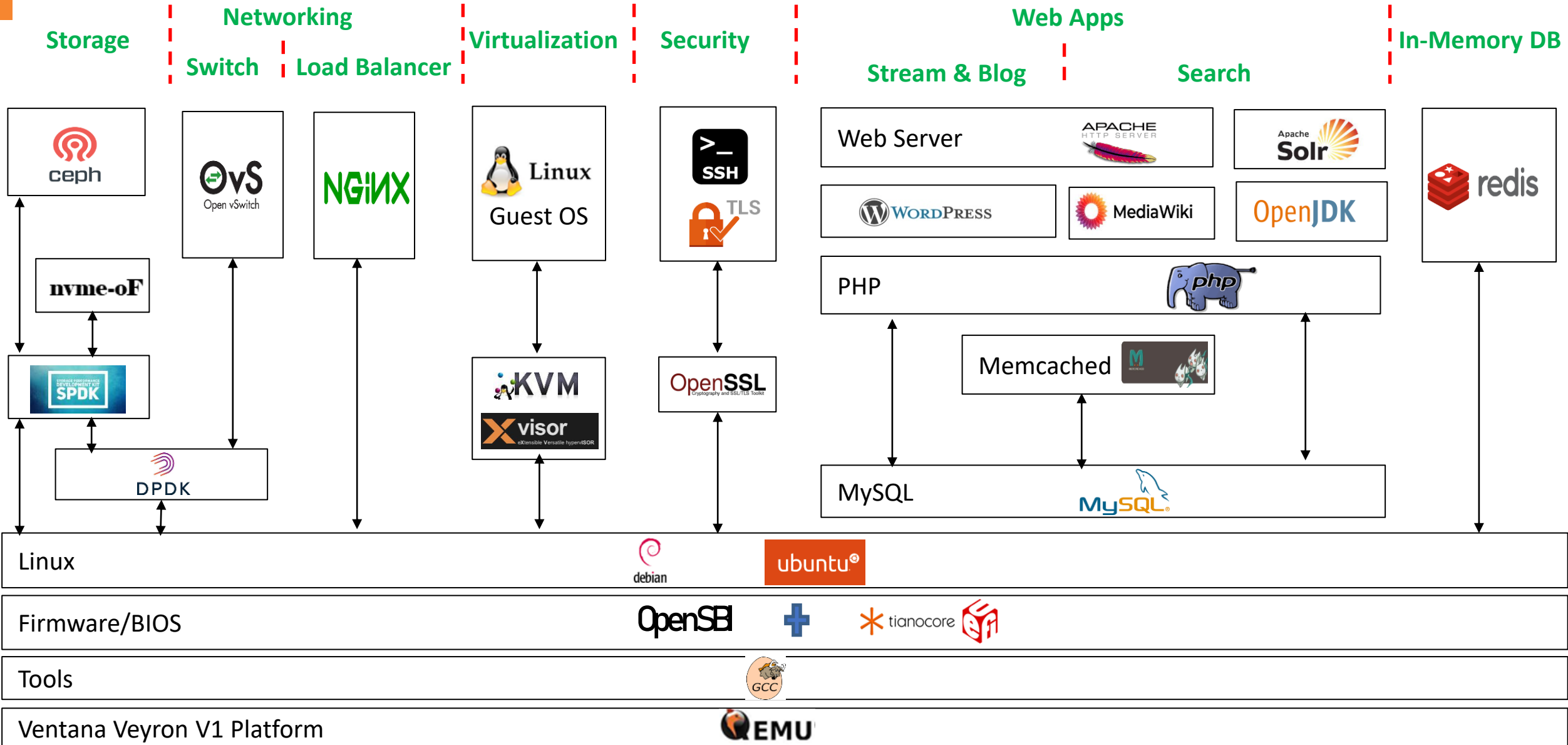
In Closing …

- High Performance Leader with Veyron V1

- Established Leadership with Veyron V1 to address all High-Performance RISC-V Target Markets

- Sustaining Leadership with upcoming next generation Veyron

- Ventana is a uniquely positioned to drive the adoption of high-performance RISC-V in Japan across automotive, data center, and other markets

VENTANA

Thank You