国立大学法人
電気通信大学

RISC-V Day Tokyo 2019

RISC-V research & education at UEC : Freedom Rocket-chip (64-bit) VexRiscv SpinalHDL (32-bit)

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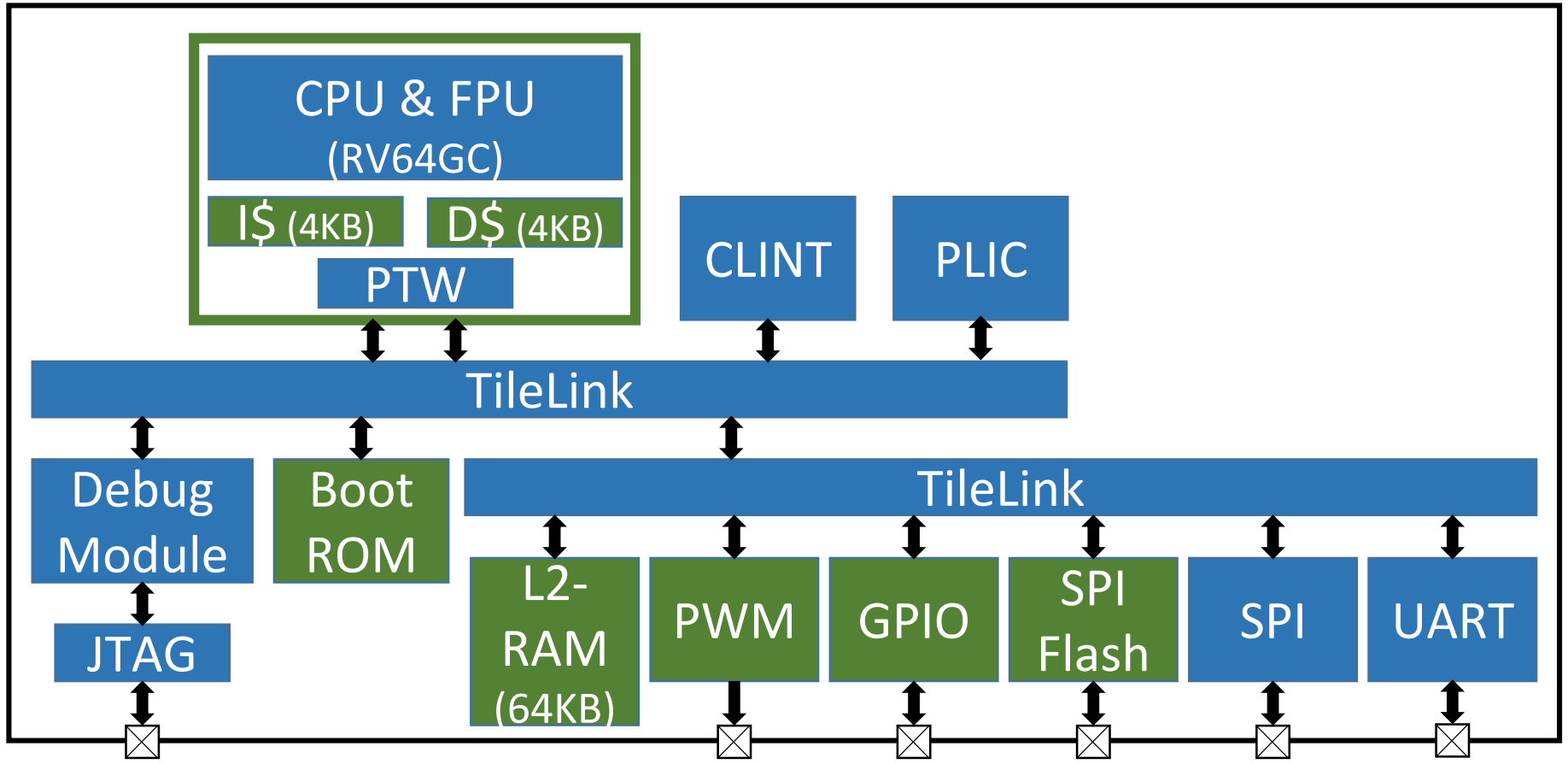
電気通信大学　範　公可

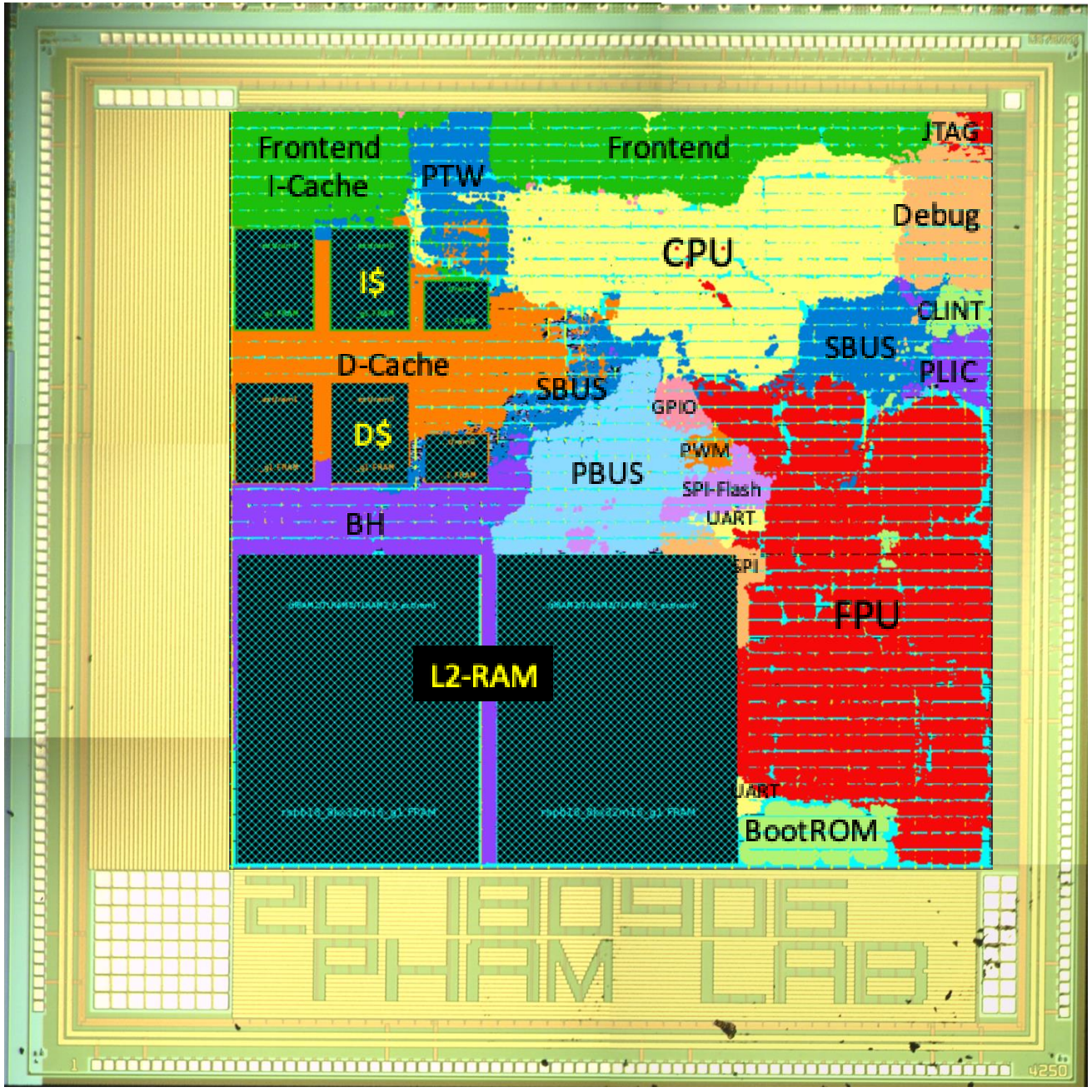
30th September 2019

Freedom Rocket-chip (64-bit)

64-bit RISC-V Chip with MMU, L1 and L2 Memories



Freedom Rocket-chip (64-bit)



Process: ROHM 0.18um

Chip Area: 5mm x 5mm

Core Area: 3.75mm x 3.75mm

SRAM:

I$ + D$: 4KiB + 4KiB

L2-RAM: 64KiB

Std. Cell: 302KG

(Utilization: 53%)

Frequency: 80MHz @typ

(not optimized)

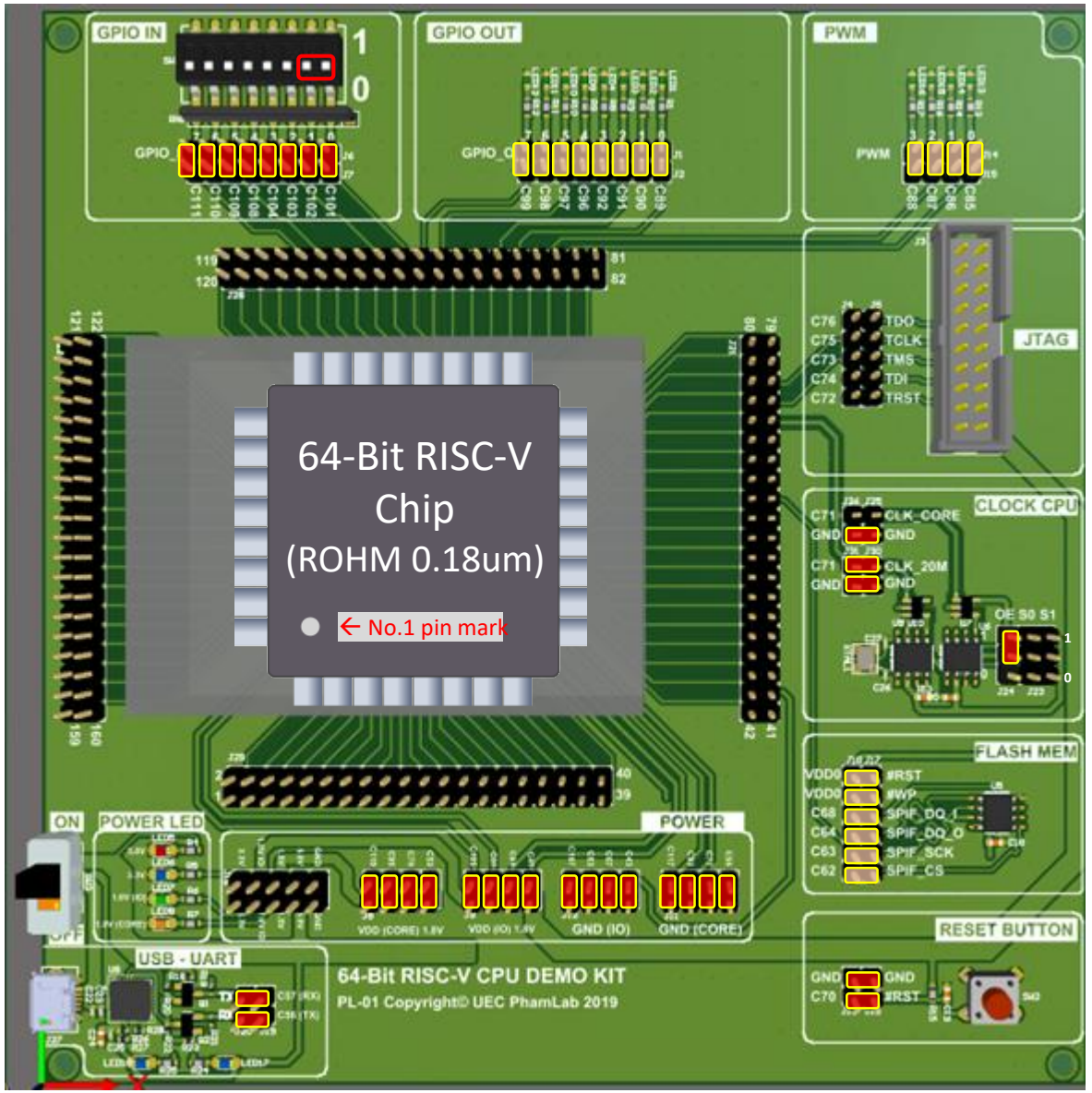
Freedom Rocket-chip (64-bit) test kit

Setup

GPIO_IN[1:0]	Boot From
00	On-Chip Boot ROM (@0x00010000)
01	Off-Chip SPI-FLASH (@0x20000000)
10	On-Chip RAM (@0x80000000)

Jumpers

- Mandatory
- Optional

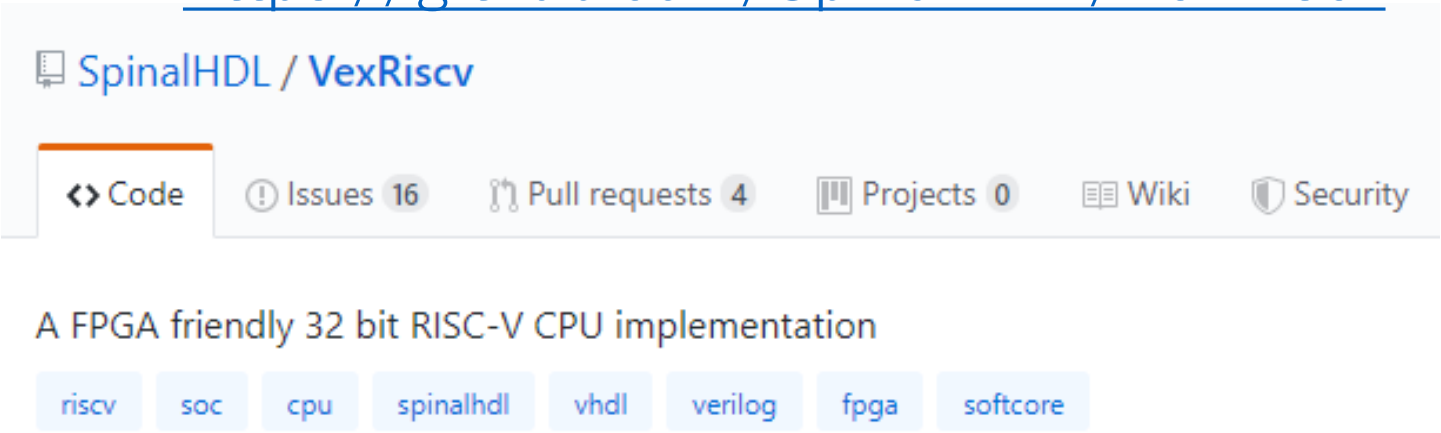


Freedom Rocket-chip (64-bit) test kit

LED demo

VexRiscv SpinalHDL (32-bit) FPGA

Follow the VexRiscv of SpinalHDL github.
Link: https://github.com/SpinalHDL/VexRiscv



Created multiple demos on various FPGAs:

- Cyclone IV: DE2-115, DE0 Nano
- Cyclone V: DE1-SoC, Arrow SoCKit
- Stratix IV: TR4, DE4

Easy to modified on the level of Scala/HDL codes & FPGA-related IPs.
Also easy to transfer the system across different FPGAs.

Small and cheap FPGAs: (suit for microcontroller development)

- DE2-115
- DE0 Nano
- DE1-SoC

Large and powerful FPGAs: (suit for Linux OS development)

- Arrow SoCKit (1GB DDR3)
- TR4 (1 DIMM-RAM socket)
- DE4 (2 DIMM-RAM sockets)

The DE4 board even has 4 serial ATA ports.

VexRiscv SpinalHDL (32-bit) FPGA

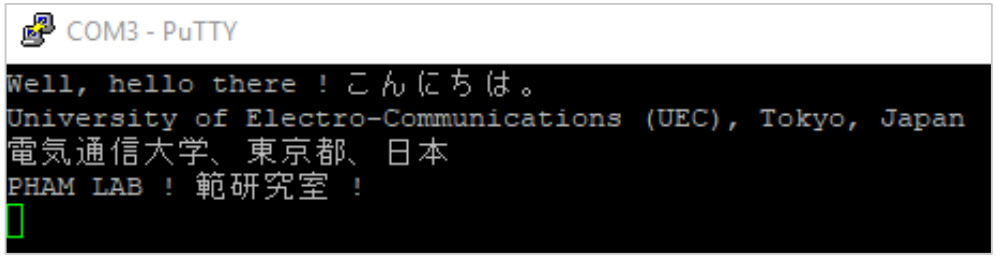
Programmed directly via GDB

GDB

```
For bug reporting instructions, please see:
<http://www.gnu.org/software/gdb/bugs/>.
Find the GDB manual and other documentation resources online at:
    <http://www.gnu.org/software/gdb/documentation/>.

For help, type "help".
Type "apropos word" to search for commands related to "word"...
Reading symbols from briey.elf...
(gdb) target remote localhost:3333
Remote debugging using localhost:3333
crtStart () at src/briey_crt.S:6
6       src/briey_crt.S: No such file or directory.
(gdb) monitor reset halt
JTAG tap: fpga_spinal.bridge tap/device found: 0x10001fff (mfg: 0x7ff (<inva
lid>), part: 0x0001, ver: 0x1)
(gdb) load
Loading section .memory, size 0x328 lma 0x40000000
Loading section .rodata, size 0x110 lma 0x40000328
Loading section .vector, size 0x13c lma 0x80000000
Start address 0x80000000, load size 1396
Transfer rate: 56 KB/sec, 465 bytes/write.
(gdb) continue
Continuing.
```

Result on UART

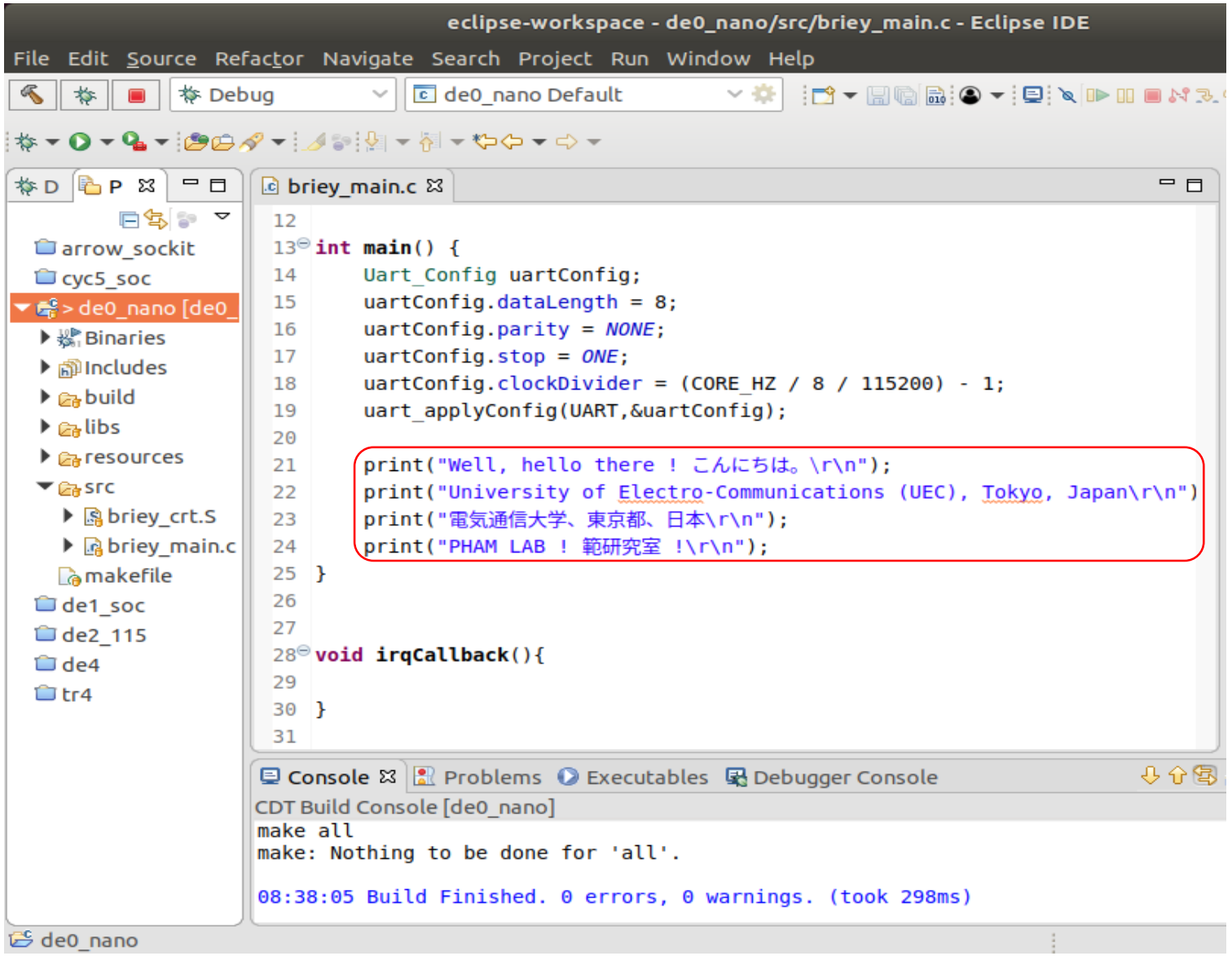


Baud-rate: 115200

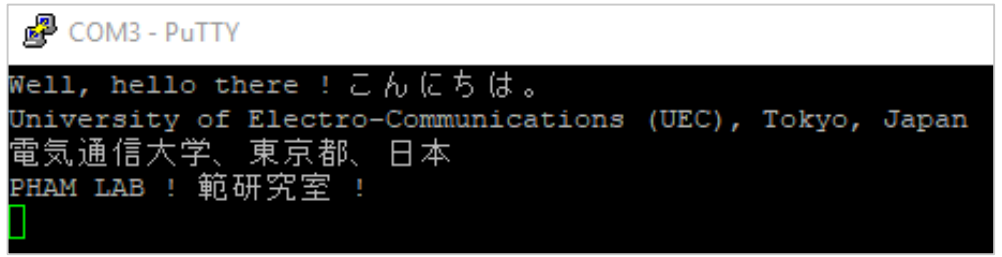
VexRiscv SpinalHDL (32-bit) FPGA

Eclipse

Debug with Eclipse tool



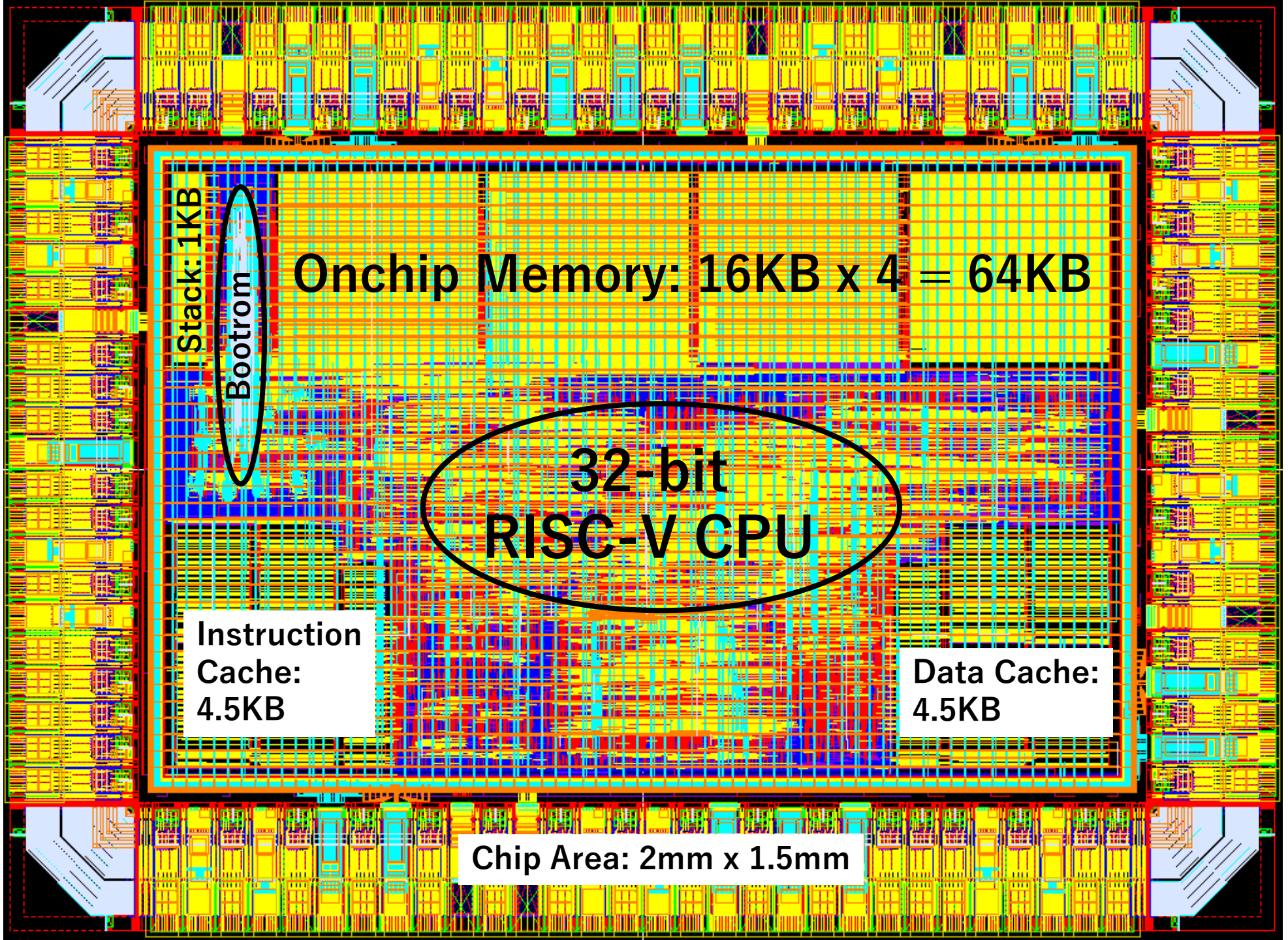
Result on UART



Baud-rate: 115200

VexRiscv SpinalHDL (32-bit) SoC on 65-nm Silicon-On-Thin-Box (SOTB)

- The chip has SRAMs inside with 64KB of on-chip memory, 4.5KB of instruction cache, 4.5KB of data cache, and 1KB for the stack. Moreover, 8KB of hard-coded boot ROM was built inside.
- The boot ROM's code will run at start to find the correct SD card partition via the SPI pins, load the corresponding program in that partition to the 64KB on-chip SRAM, and execute that program in the SRAM.
- Besides the on-chip memory, the boot ROM, and the SPI module, the chip also contains a timer module, a UART module, 32-bit GPIOs (with 16-bit input and 16-bit output), and compatible for on-chip debugging via JTAG connection.


Stack: 1KB
Bootrom
Onchip Memory: 16KB x 4 = 64KB
32-bit
RISC-V CPU
Instruction
Cache:
4.5KB
Data Cache:
4.5KB
Chip Area: 2mm x 1.5mm