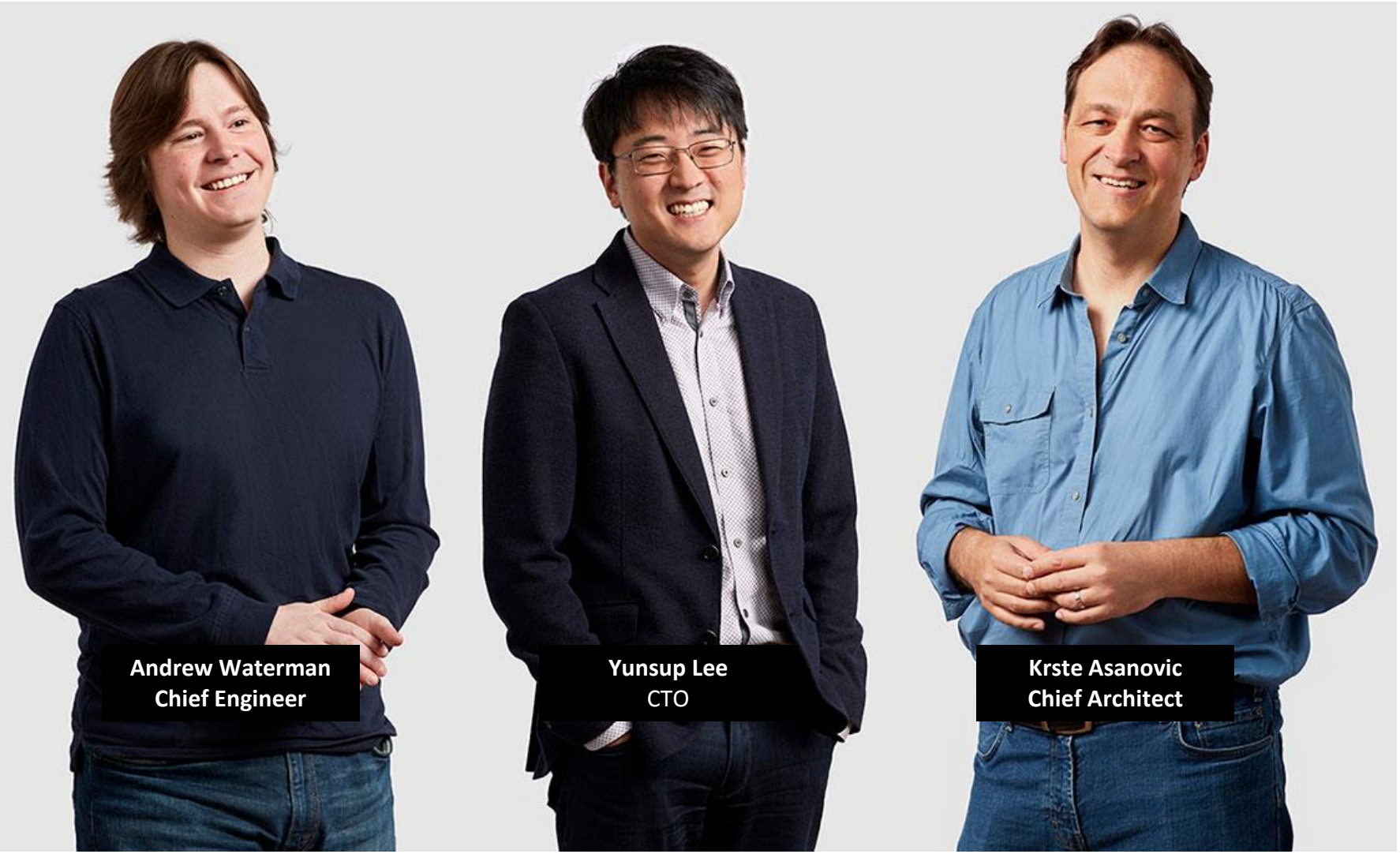
SiFive

Leading Semiconductor Design Revolution with SiFive 7-series RISC-V Core IP Enabling Embedded Intelligence

September 30, 2019



We invented RISC-V

SiFive's founders are the same UC Berkeley professor and PhDs who invented and have been leading the commercial implementation of the RISC-V Instruction Set Architecture (ISA) since 2010

GSA Global Semiconductor Alliance

"SiFive Recognized as Most Respected Private Semiconductor Company"

GSA 2018 Awards

About SiFive

SiFive

Worldwide Presence
13 Offices
350+ Employees (275+ Engineers)
300+ Tapeouts

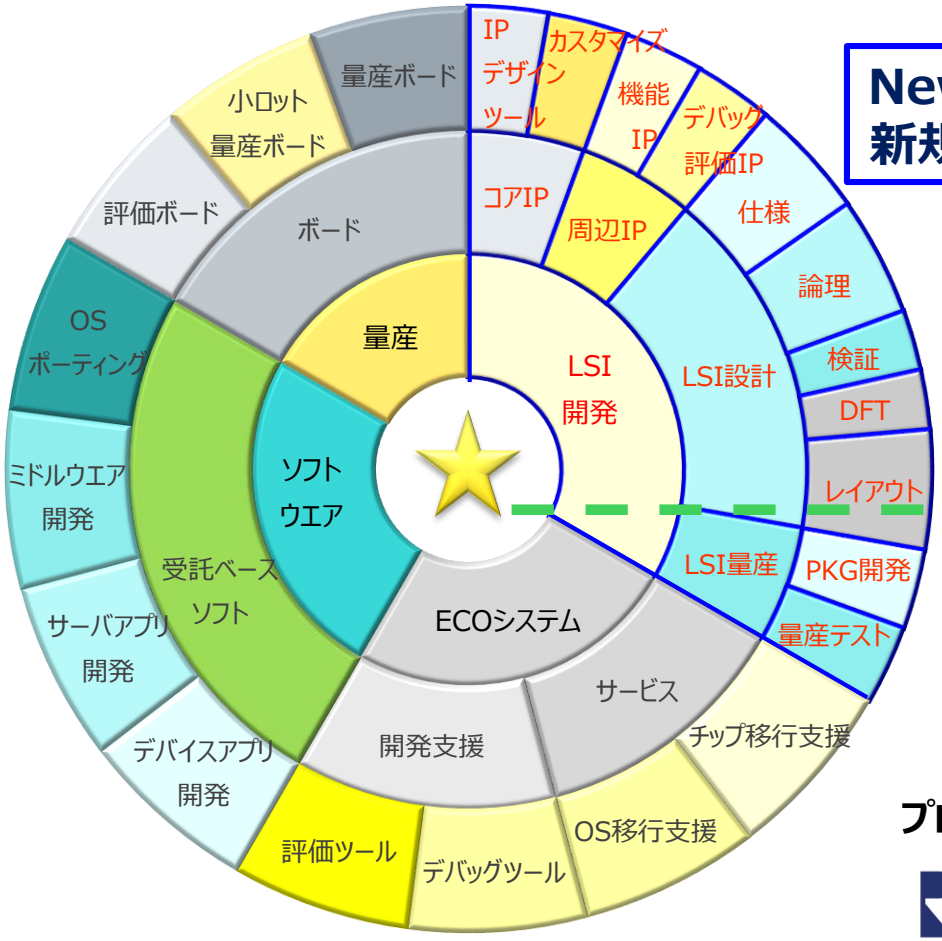
World-class expertise
- Inventors of RISC-V
- Chip Design in the Cloud
- RTL Design & Verification
- FPGA & Emulation
- Physical Design
- Wafer Fabrication
- Board Design
- Full Silicon Validation

SiFive社日本国内代理店 DTSインサイトが目指すビジネス領域

ハードウェア/ファームウェア組込などの得意領域を活かし、
お客様のあらゆるニーズにお応えする**One Stop Solution**をご提案いたします

Mainstream
既存ビジネス領域

- 組込みソフトウェア開発
- ハードウェア開発
  - （回路設計、PCB設計、機構・筐体設計から試作製造、量産）
- デバッガ(ICEなど)
- データモニターツール
- 動的テスト/解析ツール
- ソフトウェア構造分析ツール
- トレーサビリティ管理ツール



New Business
新規ビジネス領域

- **LSIデザインサービス**
  - **株式会社SSC様と協業**
- **RISC-V開発ボード環境**
- **RISC-Vデバッガ**
- **FW移行サービス**

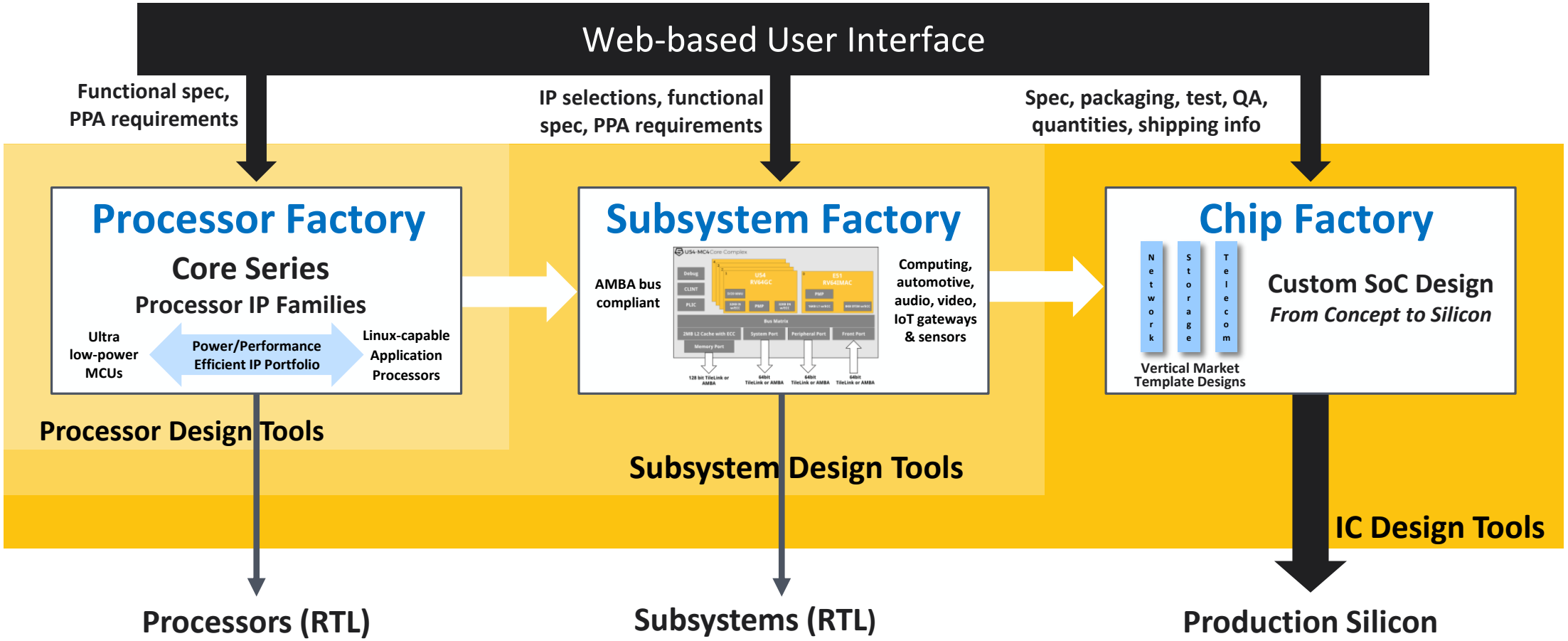
プロセッサIP（RISC-V）

RISC-V を題材にスタート

What we do

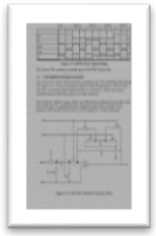
Leaders in RISC-V	Leaders in taking Semiconductors to the Cloud	Leaders in traditional ASICs (CSoC BU)
• Inventors of RISC-V • Most complete product line of CPU IP: from microcontrollers, to embedded, to high-performance multi-core processors • Very easy to customize	• Leverages software, high-level design, and automation • Dramatically reduce cost and increase innovation • Builds custom CPU IP and ASICs	• Flexible engagement model (Spec2Chip, RTL, Netlist, GDS2, Production) • Robust design methodology and extensive experience in integration of IP • Manufacturing excellence • Full responsibility of production supply chain

INNOVATION by SiFive

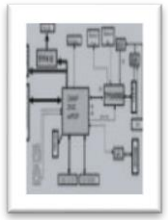


Introducing a fundamentally new approach to developing processor IP and custom SoCs (CSoCs)

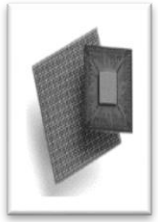
Custom SoC BU: Full Turnkey Custom SoC Solution Capability



Product Requirement & Specification



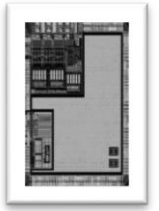
Architecture Analysis, RTL Design & Verification



IP Development, Selection & Integration

Software Design, Development & Test

FPGA & Emulation



Physical Design

Wafer Fabrication

Package & Assembly

Test & Production Engineering

Board Design

Post Silicon Validation & Software Bring-up

SiFive RISC-V Core IP Product Overview

SiFive Core IP : Efficient, High-Performance, Customizable Core IP

SiFive RISC-V Core IP

E Cores

32-bit Embedded Cores

- Edge Computing
- Artificial Intelligence
- Embedded IoT
- Wearables

S Cores

Industry leading 64-bit Embedded Cores

- Embedded Intelligence
- Storage/SSD
- AR/VR
- Machine Learning

U Cores

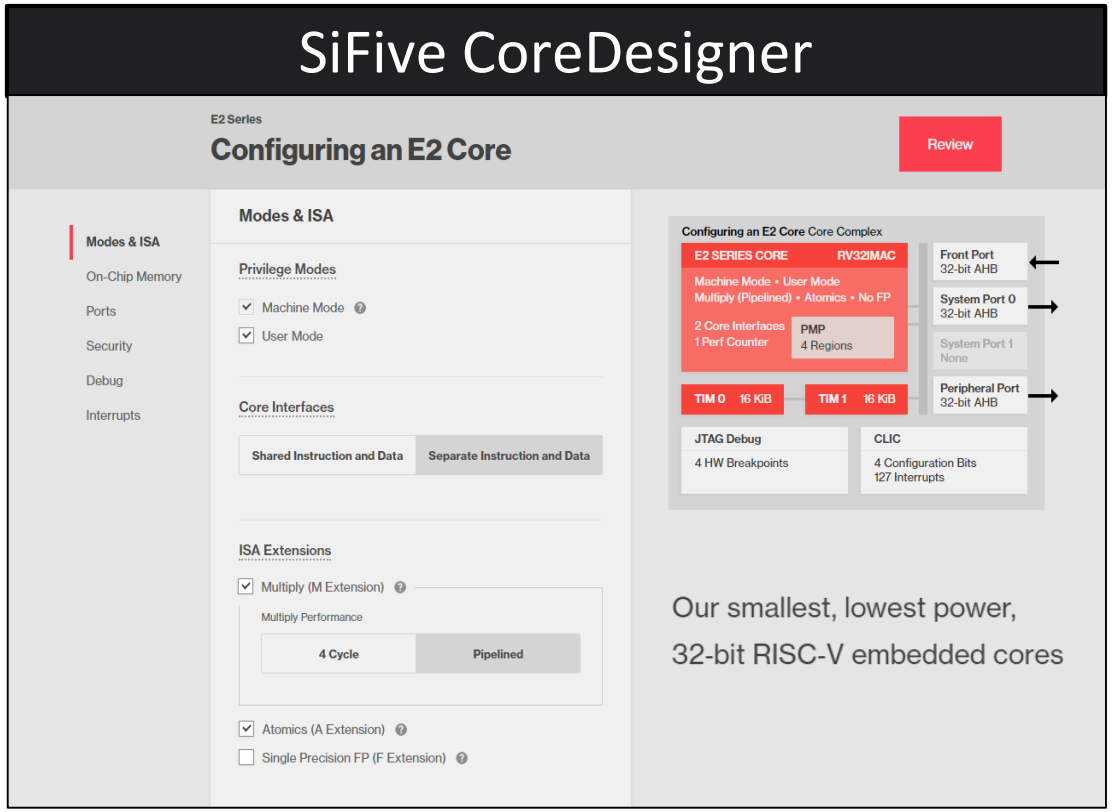
High performance, 64-bit Application Processors

- Linux applications
- Datacenter Accelerators
- Storage system controllers
- Networking baseband

- **Lowest Risk, Fastest Time to Market**
  - SiFive IP is silicon-proven and our licensees are shipping
  - Leaders in RISC-V standardization and new spec development
  - Broadest portfolio of mature cores and a well-funded roadmap
- **Unique features that scale across entire product portfolio**
  - Single delivery with multiple cores, coherent memory subsystems, buses, assembled and verified by SiFive
  - Highly Configurable, pre-integrated Verilog deliverables
- **Multiple Customization Options**
  - Highly configurable cores to achieve application specific requirements
  - Custom Instructions interface allows for differentiation enabled via the extensibility of the RISC-V ISA
  - Subsystem, memory map, etc.. are all customizable
- **Faster, Efficient Processors**
  - Measured higher total performance and performance/mW vs similar designs in the same process node

NEW IP PARADIGM : SiFive Core Designer

- Annual subscription allows a customer's engineers to access SiFive's entire processor portfolio via a simple web interface
- Configuring SiFive's processor IP is fast and easy
- A configured processor is generated in the cloud and the results are delivered to the user's SiFive dashboard (RTL, SDK, test bench, docs)



- *Explore Before* allows engineers to analyze their configured cores in their system simulations before committing to using them
- There is no processor modeling language to learn and no IP configuration tools to install
- FPGA bitstreams are provided to allow SW to run on a configured processor

RISC-V grants every user the right to modify their processor IP;
SiFive has made it incredibly easy to do so.

BUSINESS MODEL

- **Subscription-based license for SiFive Core Designer**
  - Annual fee is based on which core series are included
  - SaaS model significantly reduces your IT and EDA support requirements
  - The most cost effective way of creating your own custom RISC-V cores
  - Allows for exploration of different configurations
- **Predictable *usage* costs**
  - Pricing is determined upfront and is valid during subscription term
  - Prepaid upfront and/or negotiated usage table for follow-on projects

Custom and Cost Effective

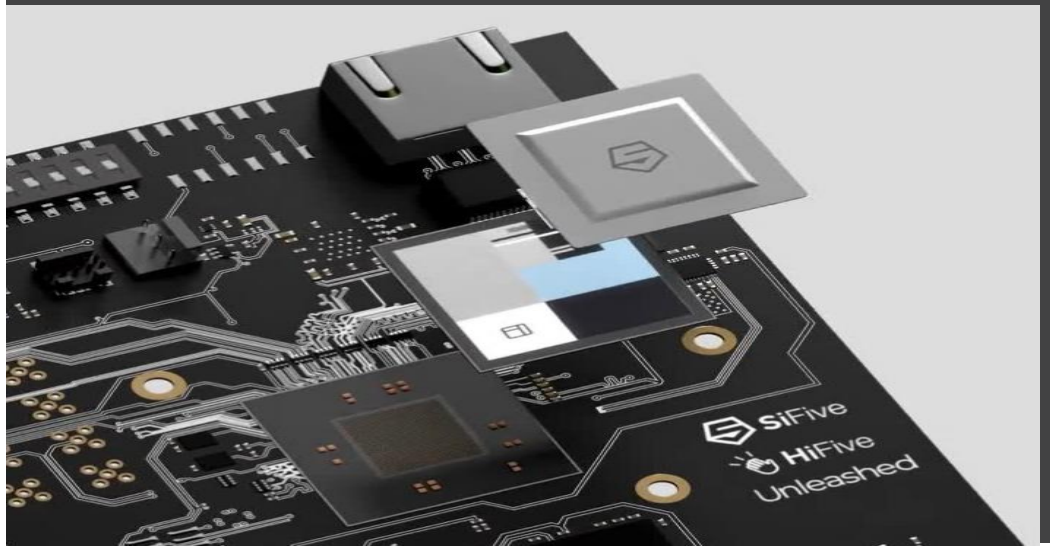
SiFive's business model delivers all the benefits and saves you money

SiFive IP Portfolio

Core Series

Choose your foundation

Core Series provide powerful capabilities for your product ideas. Choose one of our silicon-proven RISC-V Standard Cores – or customize a core to get the precise results that you need.



	Area	Standard Cores	ARM Comparison
E2 Series		E20, E21, E24	M0, M0+, M3, M4, M23, M33
E3 Series		E31, E34	R4, R5
E7 Series		E76, E76-MC	M7, R7, R8
S5 Series		S51, S54	R4, R5
S7 Series		S76, S76-MC	M7, R7, R8
U5 Series		U54, U54-MC	A5, A7, A35, A53
U7 Series		U74, U74-MC	A55

Get best-in-class processor IP developed by the inventors of RISC-V and configure it to your exact specifications

SiFive RISC-V Core IP Product Series

SiFive RISC-V Core IP

E Cores | S Cores

Industry leading 32-bit and 64-bit Embedded Cores

7 Series High Performance Embedded	Storage Networking Automotive	S76, S76-MC E76, E76-MC
3/5 Series Small, Efficient, Performance	Industrial Modems Storage	S51, S54 E31, E34
2 Series SiFive's Most Efficient Series	Microcontrollers IoT Wearables	E21, E24 E20

U Cores

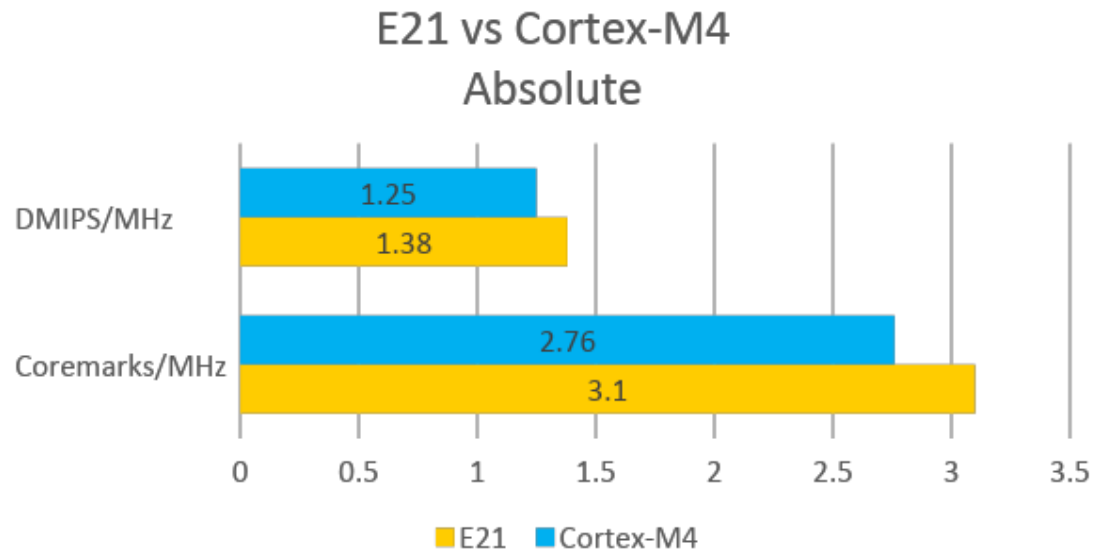
High performance 64-bit Application Cores

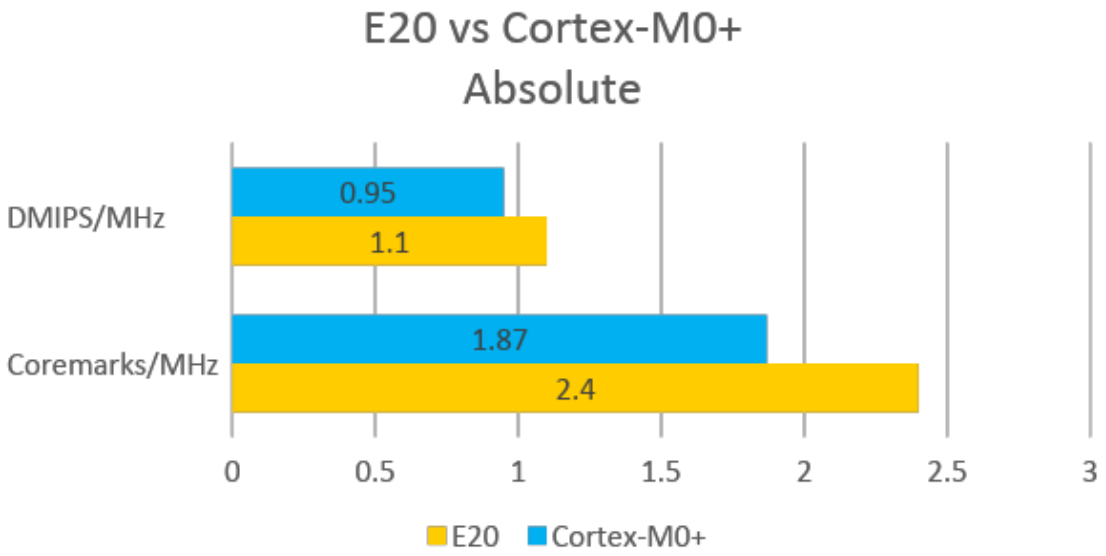
7 Series Optimized High-Performance	SBC Networking Consumer	U74 U74-MC
5 Series Multi-Core RISC-V Linux	Low Cost Linux Industrial Gateways	U54-MC U54

Core Series are customizable to meet your requirements
Standard Cores are pre-configured, silicon-proven implementations

Better than the Competition

- **SiFive Standard Core outperform ARM equivalent cores**
- **E21 is 12% higher performance per MHz vs Cortex-M4 in CoreMark**
  - When using equivalent GCC Compilers
- **E20 is 28% higher performance per MHz vs Cortex-M0+ in CoreMark**
  - When using equivalent GCC Compilers
- **E2 Series configurability allows for the core performance and area to be tuned to the exact application requirements**
  - The E2 Series can be configured smaller than the E20 Standard Core
  - The E2 Series can be configured with more features than the E21 Standard Core





Product Map

	E Cores — 32-bit embedded cores: MCU, edge computing, AI, IoT	S Cores — 64-bit embedded cores: Storage, AR/VR, machine learning	U Cores — 64-bit application cores: Linux, datacenter, network baseband
7 Series — **Highest performance:** 8-stage, dual-issue superscalar pipeline	**E7 Series**	**S7 Series**	**U7 Series**
	E76-MC — Compare to Cortex-M7 Quad-core 32-bit embedded processor	**S76-MC** — No 64-bit Cortex equivalent Quad-core 64-bit embedded processor	**U74-MC** — Compare to Cortex-A55 MP4 Multicore: four U74 cores and one S76 core
	E76 — Compare to Cortex-M7 High performance 32-bit embedded core	**S76** — No 64-bit Cortex equivalent High-performance 64-bit embedded core	**U74** — Compare to Cortex-A55 High performance LInux-capable processor
3/5 Series — **Efficient performance:** 5–6-stage, single-issue pipeline	**E3 Series**	**S5 Series**	**U5 Series**
	E34 — Compare to Cortex-R5F E31 features + single-precision floating point	**S54** — No 64-bit Cortex equivalent S51 features + single-precision floating point	**U54-MC** — Compare to Cortex-A53 Multicore application processor with four U54 cores and one S76 core
	E31 — Compare to Cortex-R5 Balanced performance and efficiency	**S51** — No 64-bit Cortex equivalent Low-power 64-bit MCU core	**U54** — Compare to Cortex-A53 Linux-capable application processor
2 Series — **Power & area optimized:** 2–3-stage, single-issue pipeline	**E2 Series**	**S2 Series**	
	E24 — Compare to Cortex-M4F E21 + single-precision floating point	**S21** — No 64-bit Cortex equivalent Area-efficient 64-bit MCU core	
	E21 — Compare to Cortex-M4 E20 + User Mode, Atomics, Multiply, TIM		
	E20 — Compare to Cortex-M0+ Our smallest, most efficient core		

RISC-V®

E Cores

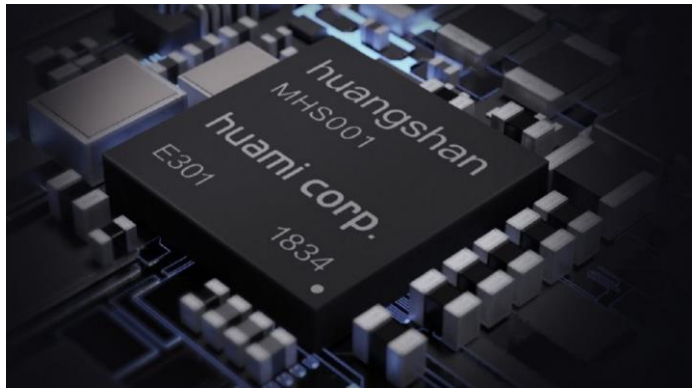
32-bit Embedded Processors

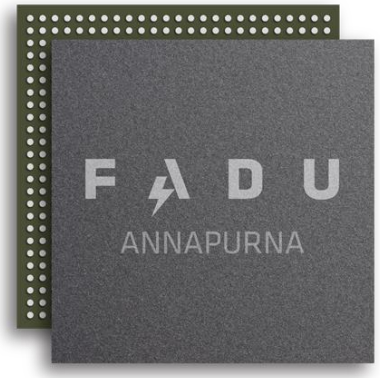
S Cores

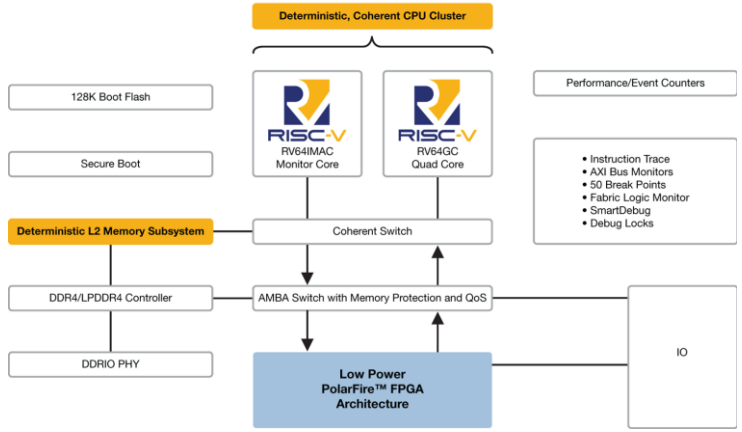
64-bit Embedded Processors

U Cores

64-bit Application Processors







"SiFive's RISC-V Core IP was **1/3 the power** and **1/3 the area** of competing solutions, and gave FADU the flexibility we needed in optimizing our architecture to achieve these groundbreaking products."

-J. Lee, FADU CEO

"SiFive's **64-bit S Cores** bring their hallmark efficiency, configurability and **silicon-proven** Core IP **expertise** to 64-bit embedded architectures"

-Ted Speers, Head of Product Architecture and Planning, Microsemi, a Microchip Company

U Cores

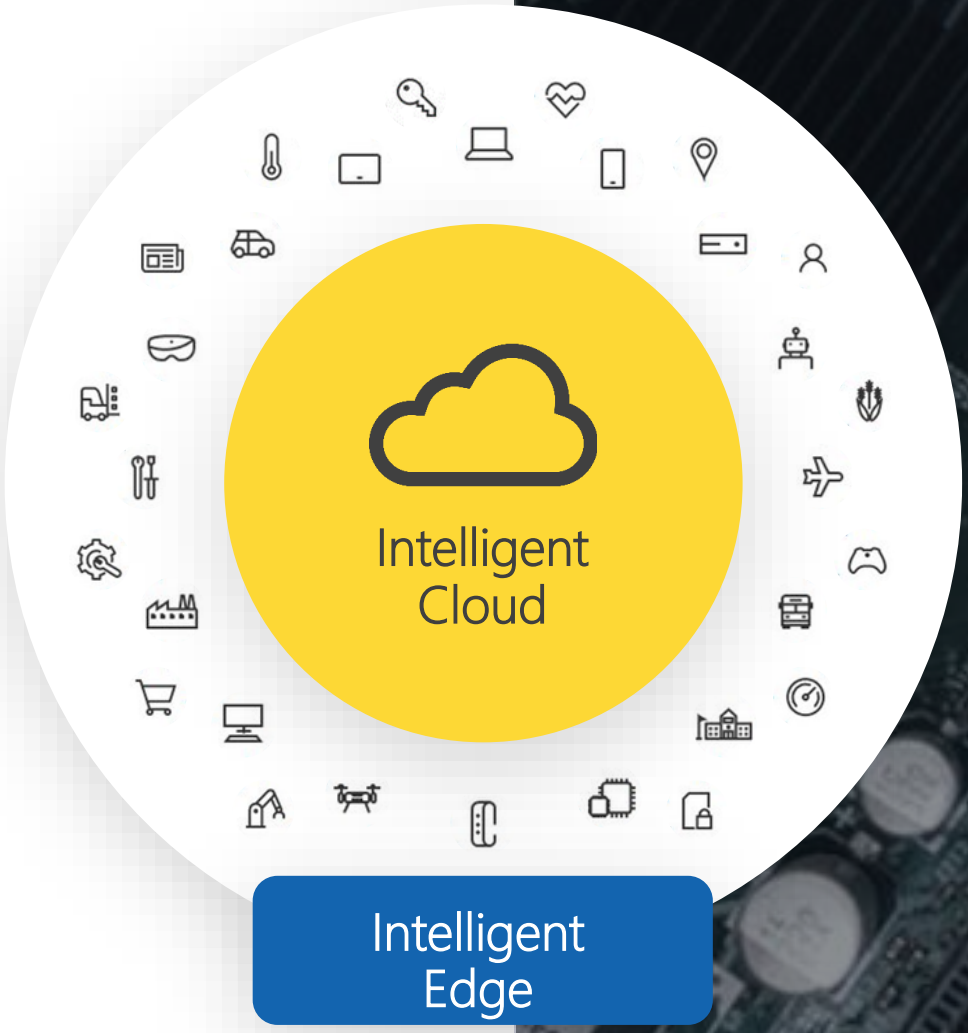
64-bit Application Processors

S Cores

64-bit Embedded Processors

E Cores

32-bit Embedded Processors



Embedding Intelligence from the Edge to the Cloud

SiFive Core IP
Embedding Intelligence Everywhere

Modern compute workloads require scalability, efficient performance and customizations

Consumer

AR/VR/Gaming devices

Smart Home

Imaging/Wearables

Storage/Networking/5G

SSD, SAN, NAS

Base Stations, Small cells, APs

Switches, Smart NICs, Offload cards

ML/Edge

Sensor Hubs, Gateways

Autonomous machines

IoT devices

SiFive

SiFive Core IP

Embedding Intelligence Everywhere

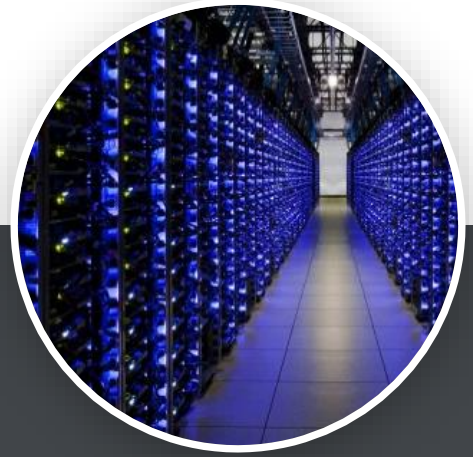
SiFive realizes modern compute requirements with scalable, efficient and customizable IP

Consumer

Efficient Performance

Optimized power consumption

Differentiated products



Storage/Networking/5G

Scalable portfolio

Total cost of operation (TCO)

64-bit addressability

ML/Edge

Custom instructions and coprocessors

Tightly coupled accelerators

Low power consumption

SiFive

SiFive Core IP 7 Series:

Embedded Intelligence Everywhere

Efficient Performance

- **~60% improvement** in CoreMarks/MHz*
- **~40% improvement** in DMIPS/MHz*
- **~10% improvement** in Fmax*

Scalability

- **8+1 coherent CPUs** in a cluster
- **512 coherent on-chip CPUs** via **TileLink**
- **2048 multi-socket coherent CPUs** via **ChipLink**

Compelling Feature Set

- **In-cluster heterogeneous compute** for Application + Real-time processors
- **64-bit architectures** across portfolio
- **Innovative L1 Memory microarchitecture**

*Compared to SiFive Core IP 5 series

SiFive RISC-V Core IP - 7 Series

SiFive 7 Series RISC-V Core IP

E7 Series

Ultra-High Performance 32-bit Embedded Processors

Unprecedented Performance/Watt/mm2
Scalable Multi-Core with Coherency
Determinism for Hard Real-Time
Fast, Deterministic, Interrupt Response
Fast IO Access
Tightly Coupled Accelerators

S7 Series

Ultra-High Performance 64-bit Embedded Processors

Unprecedented Performance/Watt/mm2
Scalable Multi-Core with Coherency
Determinism for Hard Real-Time
Fast, Deterministic, Interrupt Response
Fast IO Access
Tightly Coupled Accelerators

U7 Series

Ultra-High Performance 64-bit Application Processors

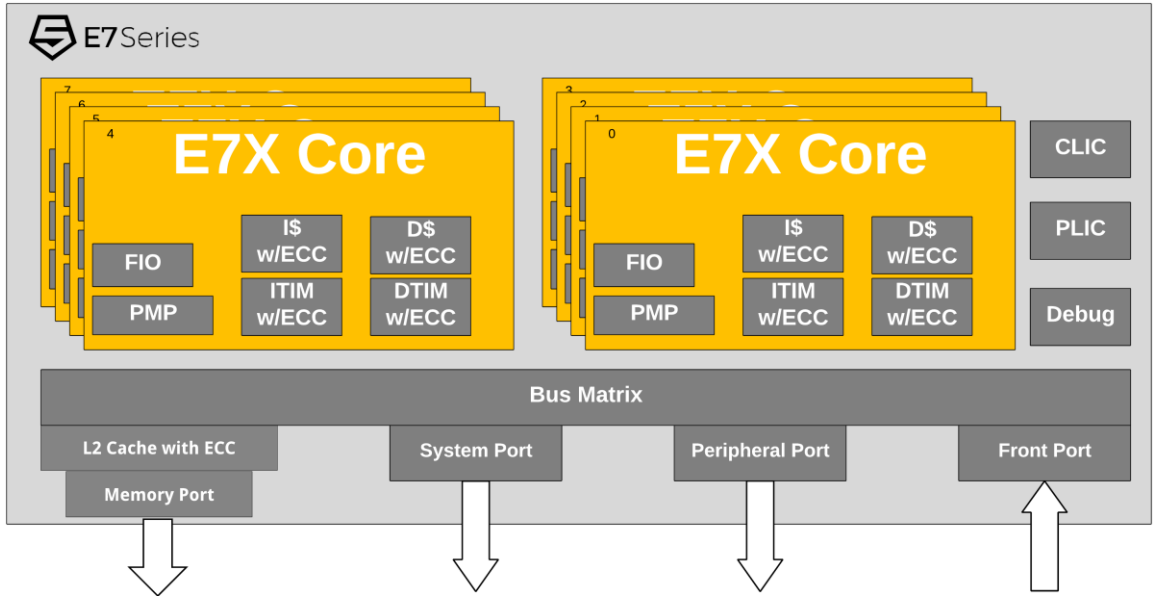
Unprecedented Performance/Watt/mm2
Scalable Multi-Core with Coherency
Determinism for Hard Real-Time
Fast, Deterministic, Interrupt Response

Common Feature Sets

Compared To SiFive 3 and 5 Series

- **Greater than 50% performance uplift**
- **Improved L1 Memory System**
- **10% frequency uplift**

E7 Series Features



- E7 core architectural features
  - RV32GCV capable core
  - Dual Issue, in-order 8-stage Harvard Pipeline
- Very flexible memory system
  - Optional I$ and D$
  - Optional I and D TIM interfaces
  - Optional Fast IO Port (FIO) per core
- Multi-core capable with coherency and optional L2
- Deterministic fast interrupt responses
- Higher throughput and efficiency vs Cortex-M7
  - **2.3 DMIPS/MHz**
  - **5.1 CoreMarks/MHz**

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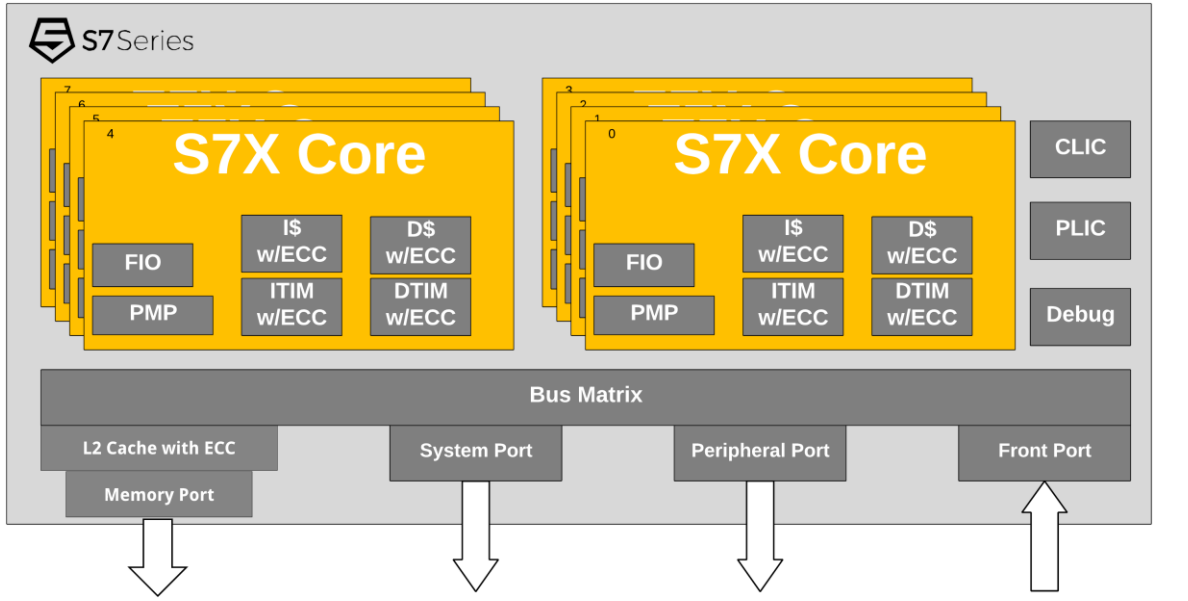
S7 Series Features



- S7 core architectural features
  - RV64GCV capable core
  - Dual Issue, in-order 8-stage Harvard Pipeline
- Very flexible memory system
  - Optional I$ and D$
  - Optional I and D TIM interfaces
  - Optional Fast IO Port (FIO) per core
- Multi-core capable with coherency and optional L2
- Deterministic fast interrupt responses
- Higher throughput and efficiency vs Cortex-R8
  - **2.5 DMIPS/MHz**
  - **5.1 CoreMarks/MHz**

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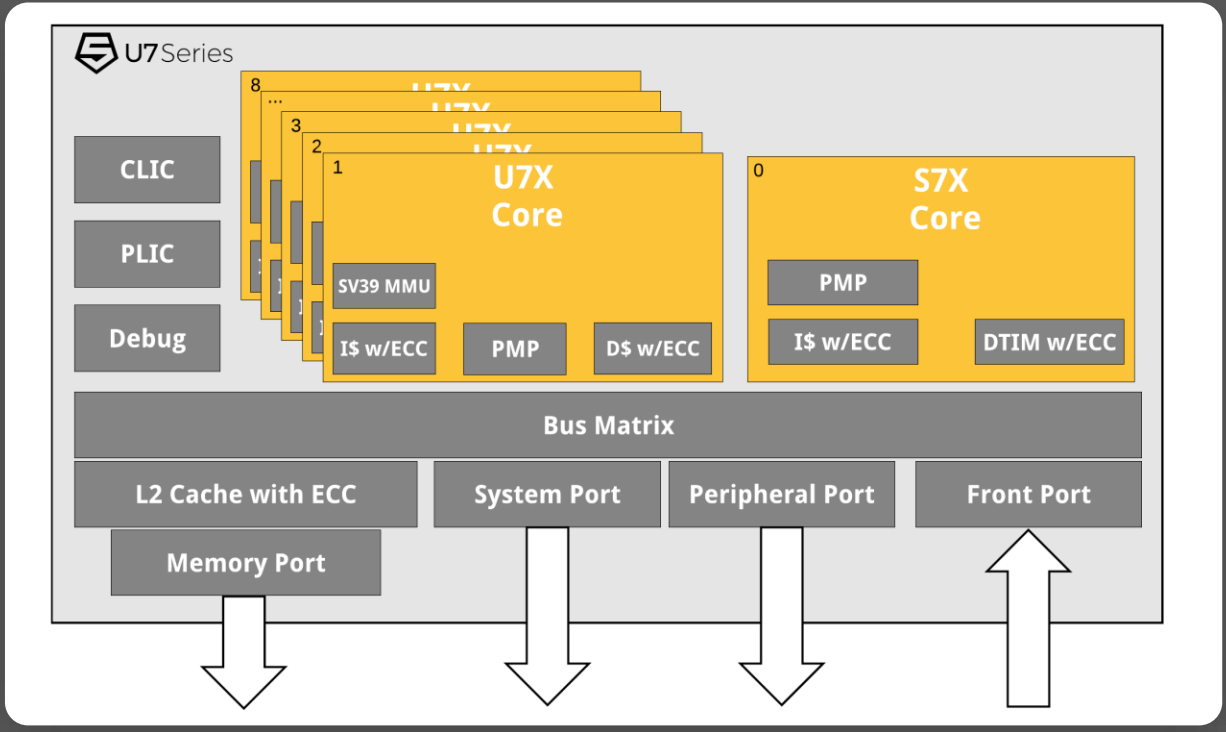
U7 Series Features



- U7 Core Architectural Features
  - RV64GCV capable core
  - Sv39 Virtual Memory Support
  - Dual Issue, in-order 8 stage Harvard Pipeline
- Heterogenous in-cluster combination of applications processor and real-time processor supported
- Configurable Level 2 Cache with cache lock capability and Tightly Integrated Memory available
- Functional Safety and Security and Real Time features
  - SECDED ECC on all L1 and L2 memories
  - PMP and MMU for memory protection
  - **Programmatically clear and/or disable dynamic branch prediction** for deterministic execution and enhanced security
- Extremely competitive performance vs Cortex-A55 with higher efficiency and throughput
  - **2.5 DMIPS/MHz**
  - **5.1 CoreMarks/MHz**

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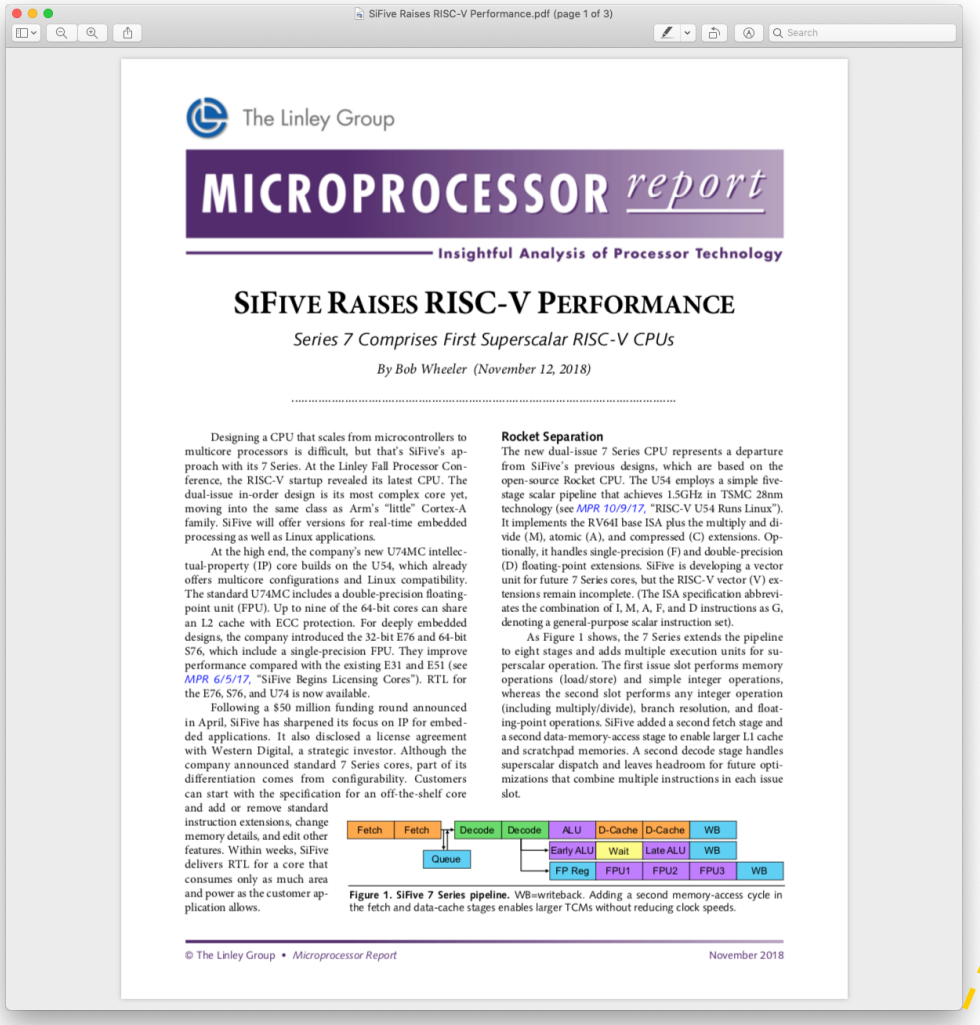
7 Series Core IP - More Efficient Performance than M7 and A55


SiFive Raises RISC-V Performance.pdf (page 1 of 3)

The Linley Group

MICROPROCESSOR report

Insightful Analysis of Processor Technology

SiFive Raises RISC-V Performance

Series 7 Comprises First Superscalar RISC-V CPUs

By Bob Wheeler (November 12, 2018)

Designing a CPU that scales from microcontrollers to multicore processors is difficult, but that's SiFive's approach with its 7 Series. At the Linley Fall Processor Conference, the RISC-V startup revealed its latest CPU. The dual-issue in-order design is its most complex core yet, moving into the same class as Arm's "little" Cortex-A family. SiFive will offer versions for real-time embedded processing as well as Linux applications.

At the high end, the company's new U74MC intellectual-property (IP) core builds on the U54, which already offers multicore configurations and Linux compatibility. The standard U74MC includes a double-precision floating-point unit (FPU). Up to nine of the 64-bit cores can share an L2 cache with ECC protection. For deeply embedded designs, the company introduced the 32-bit E76 and 64-bit S76, which include a single-precision FPU. They improve performance compared with the existing E31 and E51 (see *MPR 6/5/17*, "SiFive Begins Licensing Cores"). RTL for the E76, S76, and U74 is now available.

Following a $50 million funding round announced in April, SiFive has sharpened its focus on IP for embedded applications. It also disclosed a license agreement with Western Digital, a strategic investor. Although the company announced standard 7 Series cores, part of its differentiation comes from configurability. Customers can start with the specification for an off-the-shelf core and add or remove standard instruction extensions, change memory details, and edit other features. Within weeks, SiFive delivers RTL for a core that consumes only as much area and power as the customer application allows.

Rocket Separation

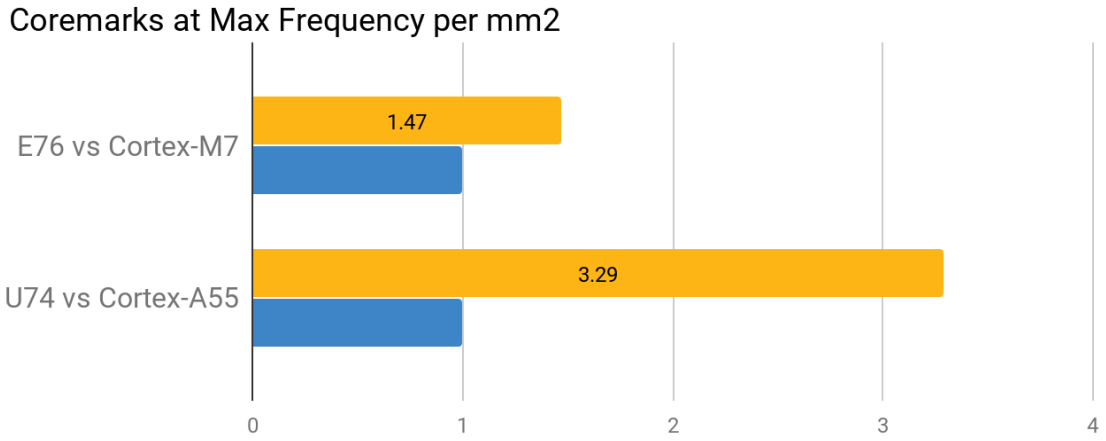
The new dual-issue 7 Series CPU represents a departure from SiFive's previous designs, which are based on the open-source Rocket CPU. The U54 employs a simple five-stage scalar pipeline that achieves 1.5GHz in TSMC 28nm technology (see *MPR 10/9/17*, "RISC-V U54 Runs Linux"). It implements the RV64I base ISA plus the multiply and divide (M), atomic (A), and compressed (C) extensions. Optionally, it handles single-precision (F) and double-precision (D) floating-point extensions. SiFive is developing a vector unit for future 7 Series cores, but the RISC-V vector (V) extensions remain incomplete. (The ISA specification abbreviates the combination of I, M, A, F, and D instructions as G, denoting a general-purpose scalar instruction set).

As Figure 1 shows, the 7 Series extends the pipeline to eight stages and adds multiple execution units for superscalar operation. The first issue slot performs memory operations (load/store) and simple integer operations, whereas the second slot performs any integer operation (including multiply/divide), branch resolution, and floating-point operations. SiFive added a second fetch stage and a second data-memory-access stage to enable larger L1 cache and scratchpad memories. A second decode stage handles superscalar dispatch and leaves headroom for future optimizations that combine multiple instructions in each issue slot.

Figure 1. SiFive 7 Series pipeline. WB=writeback. Adding a second memory-access cycle in the fetch and data-cache stages enables larger TCMs without reducing clock speeds.

	SiFive E76	Arm Cortex-M7	SiFive U74	Arm Cortex-A55
Instruction Set	32-bit RISC-V	32-bit Arm v7-M	64-bit RISC-V	64-bit Arm v8
Max Clock Freq	1.6GHz†	1.1GHz	1.6GHz†	1.6GHz†
Max IPC	2 IPC	2 IPC	2 IPC	2 IPC
CoreMark Perf	4.9CM/MHz	5.0CM/MHz	4.9CM/MHz	4.4CM/MHz†
Die Area*	0.065mm²	0.067mm²	0.22mm²	0.65mm²†

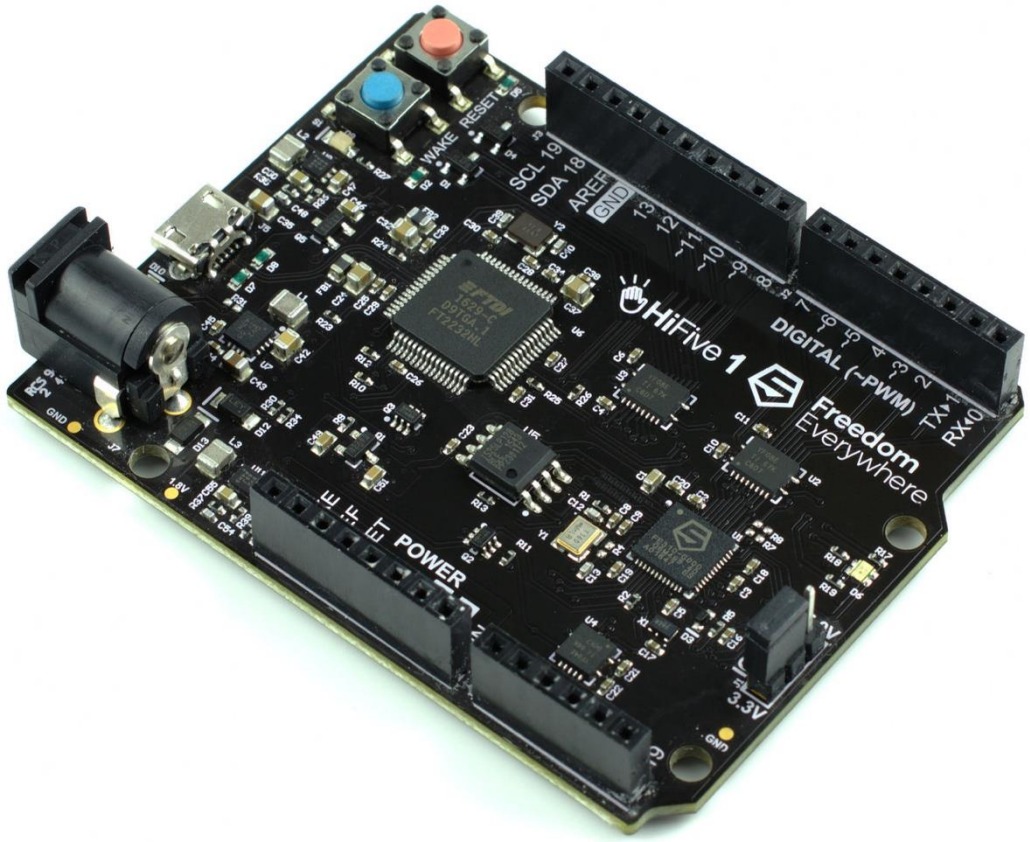
Table 1. SiFive-versus-Arm CPU comparison. The new dual-issue 7 Series delivers integer performance on a par with that of Arm's comparable CPUs. All metrics assume TSMC 28nm HP technology. *Without memories. (Source: vendors, except †The Linley Group estimate)



source : https://www.linleygroup.com/mpr/

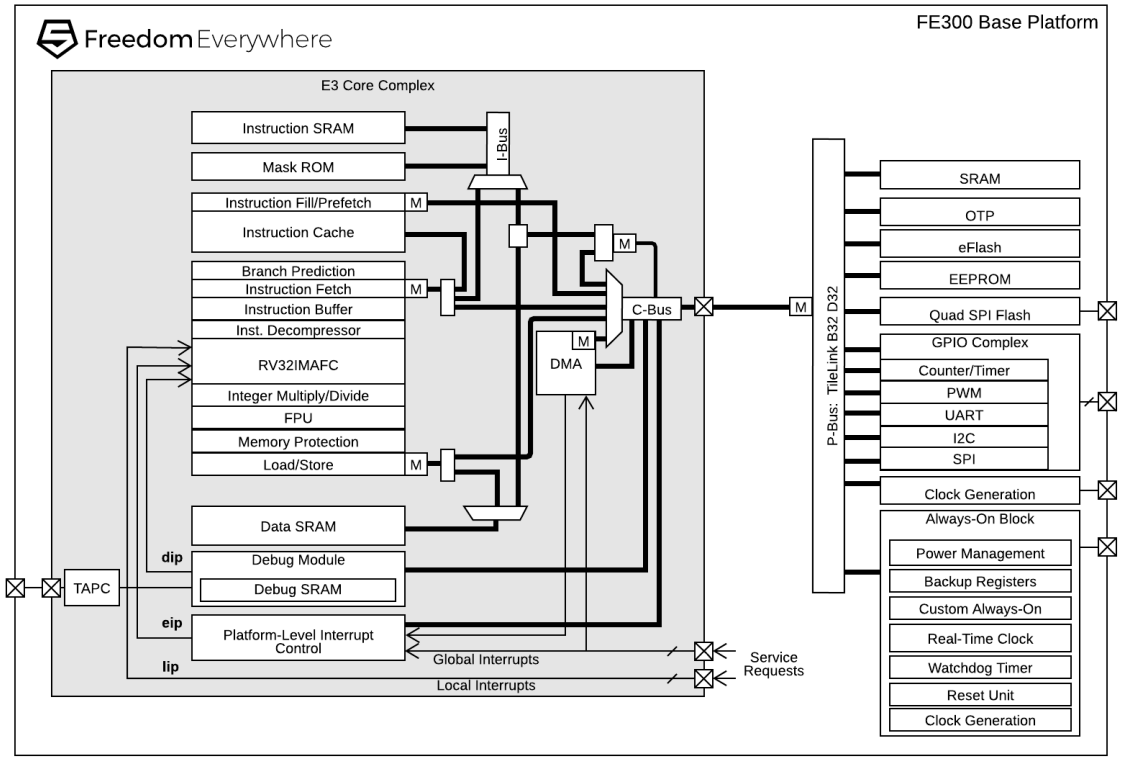
SiFive Silicon and Development Platforms

HiFive1: Arduino-Compatible RISC-V Dev Board

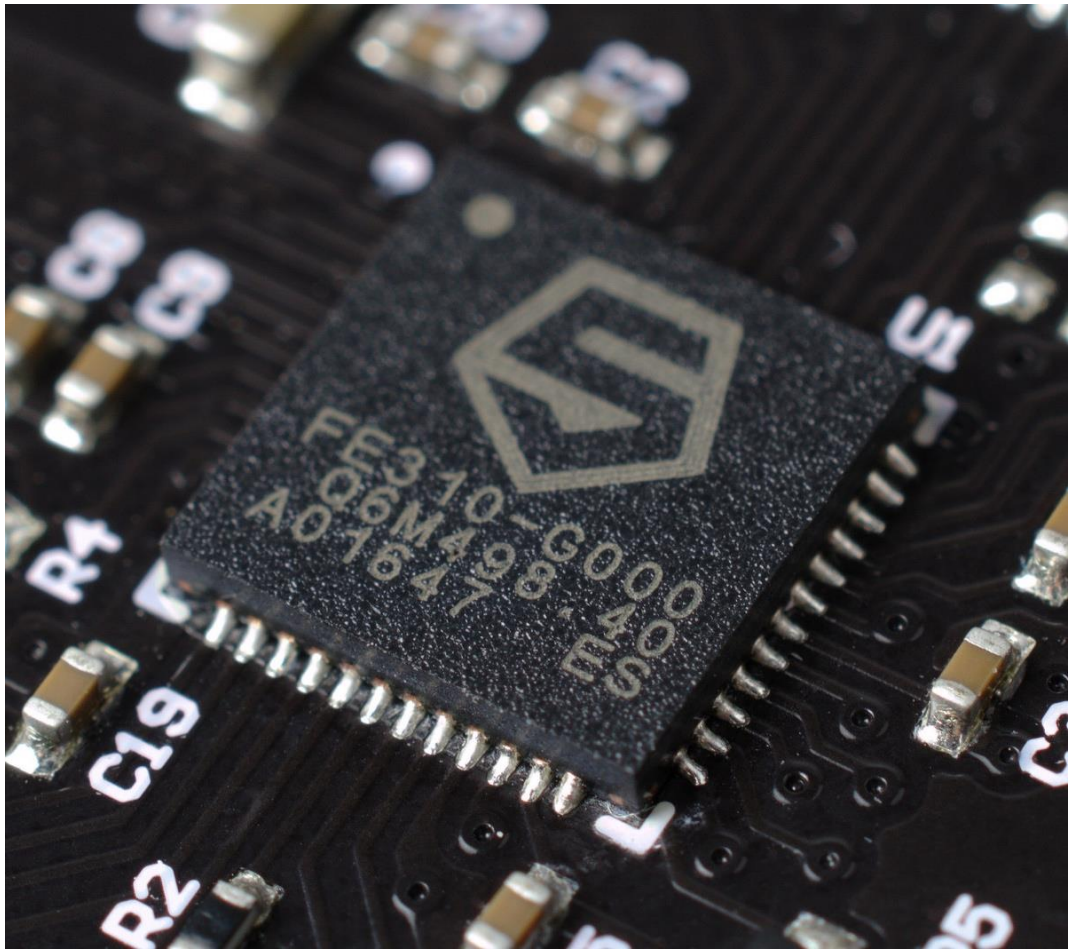


- SiFive FE310-G000 (built in 180nm)
- Operating Voltage: 3.3 V and 1.8 V
- Input Voltage: 5 V USB or 7-12 VDC Jack
- IO Voltages: Both 3.3 V or 5 V supported
- Digital I/O Pins: 19
- PWM Pins: 9
- SPI Controllers/HW CS Pins: 1/3
- External Interrupt Pins: 19
- External Wakeup Pins: 1
- Flash Memory: 16 MB Quad SPI
- Host Interface (microUSB): Program, Debug, and Serial Communication

Freedom Everywhere 32-bit Low-power microcontroller platform

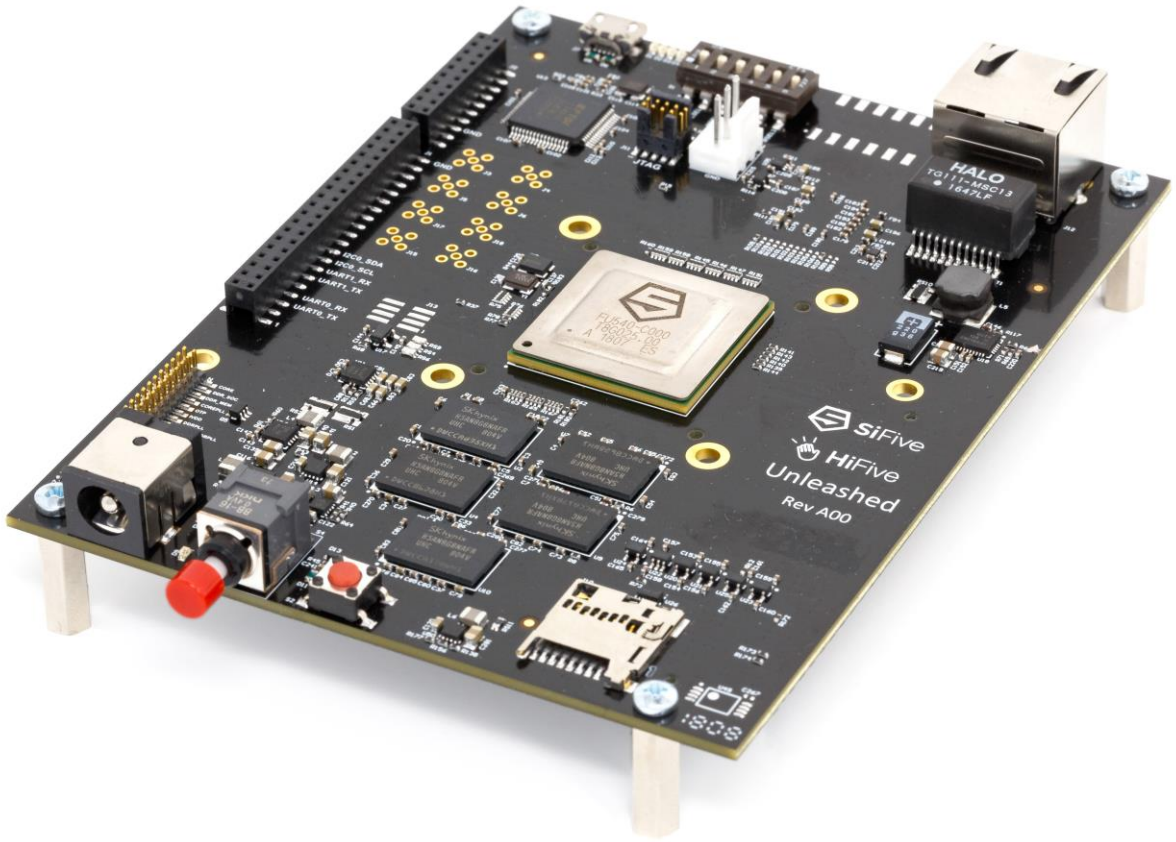


- 320+ MHz SiFive E31 CPU
  - 16KB L1I$, 16KB Data Scratchpad
  - Hardware Multiply/Divide, Debug Module
- Multiple Power Domains
- Low-Power Standby
- Wide Range of Clock Inputs



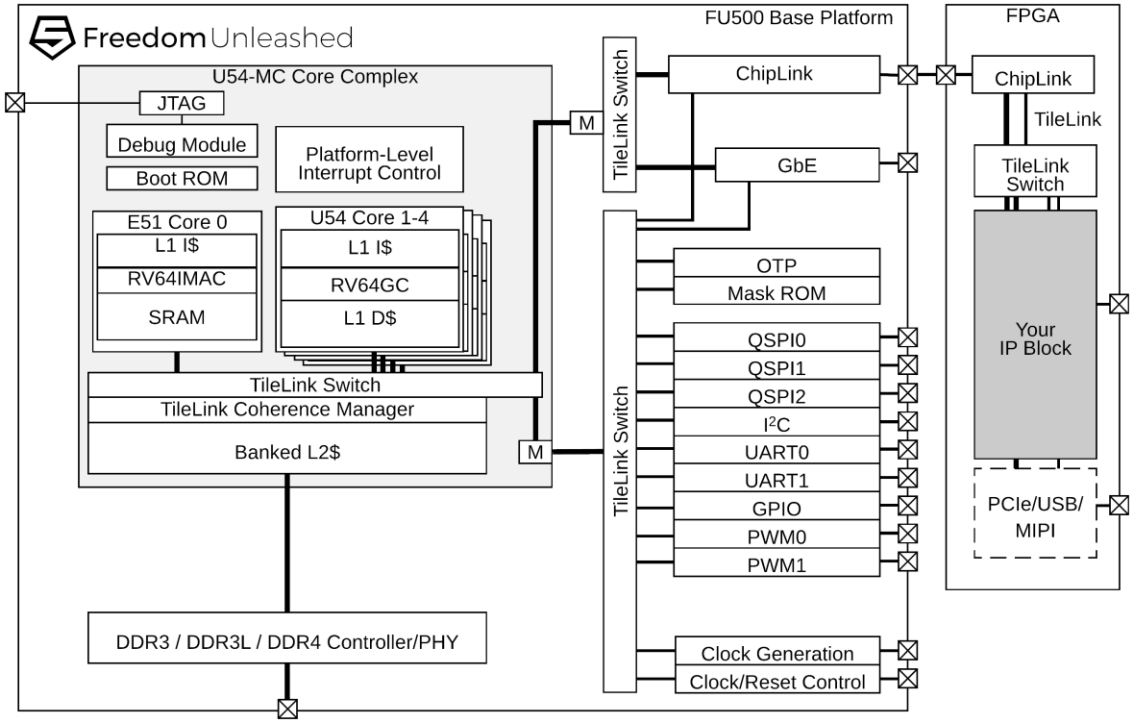
Freedom E310, QFN48, manufactured in TSMC 180nm

HiFive Unleashed: World's First Multi-Core RISC-V Linux Dev Board



- SiFive FU540-C000 (built in 28nm)
- 8 GB 64-bit DDR4 with ECC
- Gigabit Ethernet Port
- 32 MB Quad SPI Flash
- MicroSD card for removable storage
- MicroUSB for debug and serial communication
- Digital GPIO pins
- FMC connector for future expansion with add-in cards

Freedom Unleashed 64-bit Multi-Core RISC-V Linux Platform



- 1.5+ GHz U54-MC SiFive CPU
  - 1x S51: 16KB L1I$, 8KB DTIM with ECC support
  - 4x U54: 32KB L1I$, 32KB L1D$ with ECC support
  - Single- and Double-precision floating-point support
  - 2MB Banked L2$ with directory-based cache-coherence & ECC support
- ChipLink
  - Serialized Chip-to-Chip Coherent TileLink Interconnect
- DDR3/4, GbE, Peripherals

Freedom U540, FCBGA, manufactured in TSMC 28nm