VDECとAI拠点とRISC-V
VDEC, AI Chip Design Center, and RISC-V

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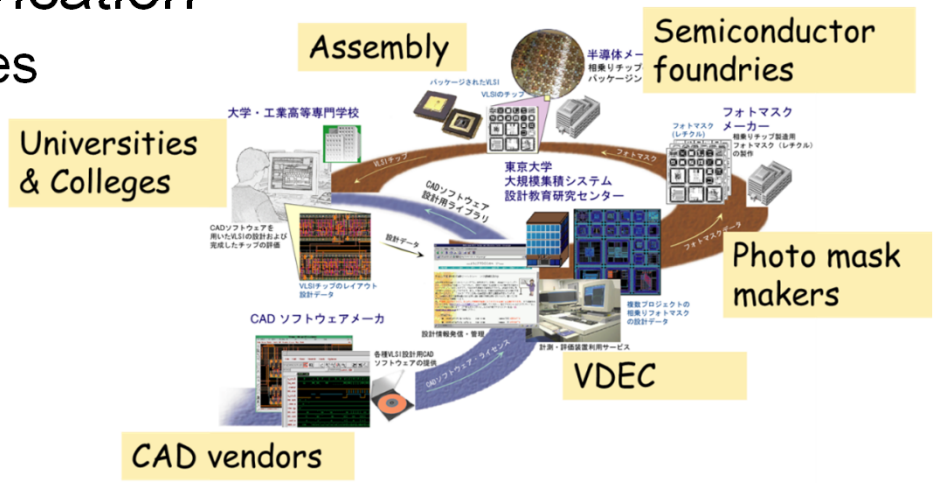
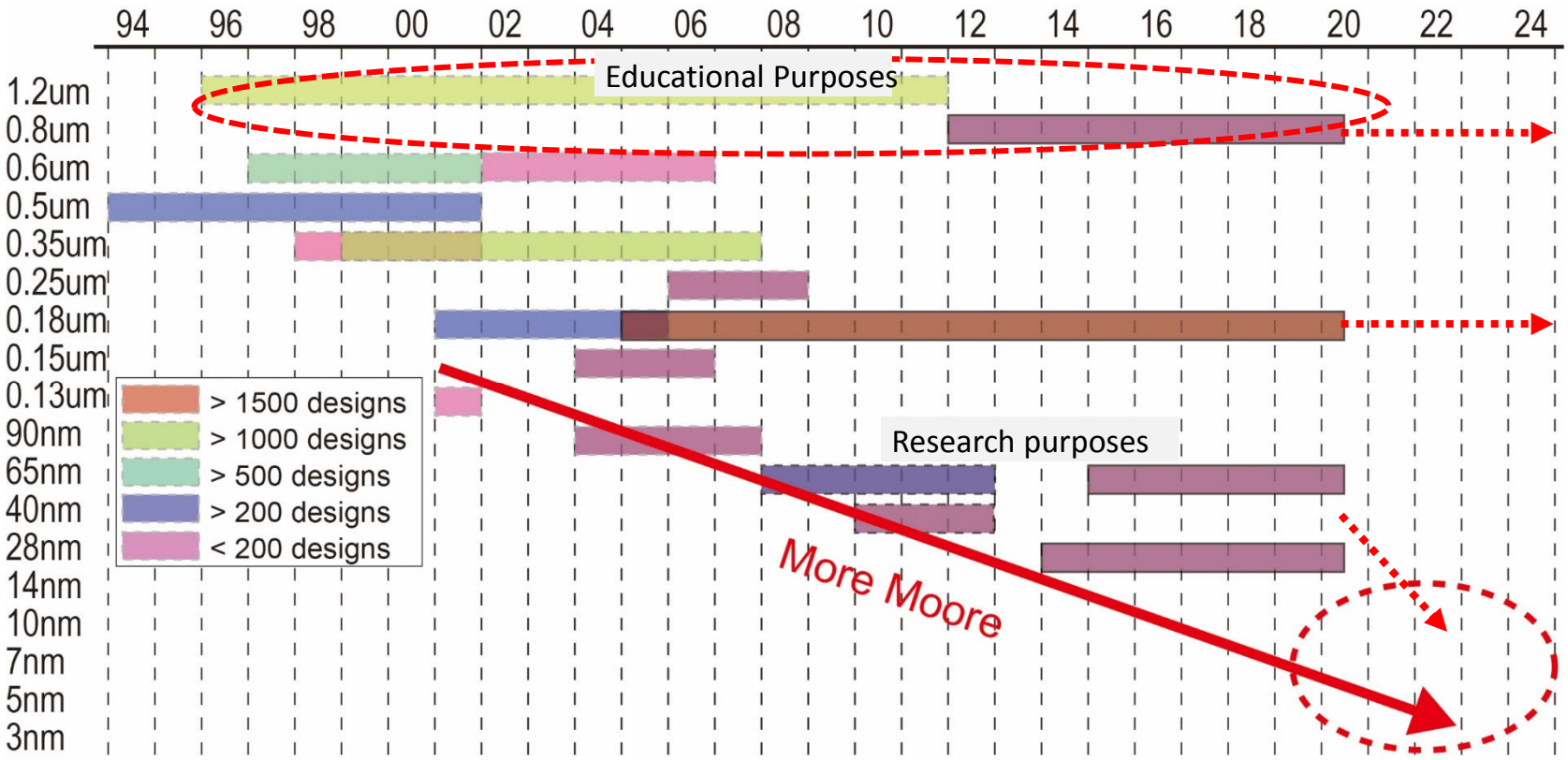
Mission & Organization of VDEC

- Provide platform for chip fabrication
  - Provide chip fabrication services
  - Provide CAD tools
  - Provide up-to-date design methodologies/seminar

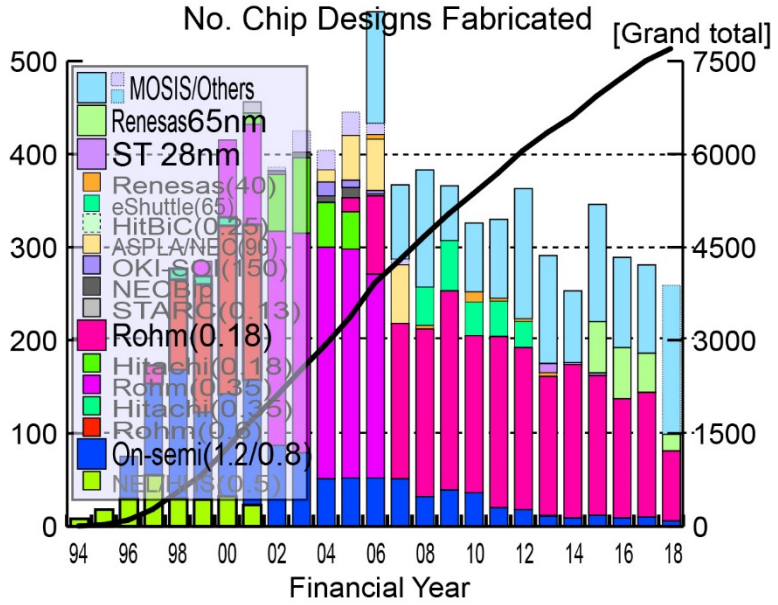


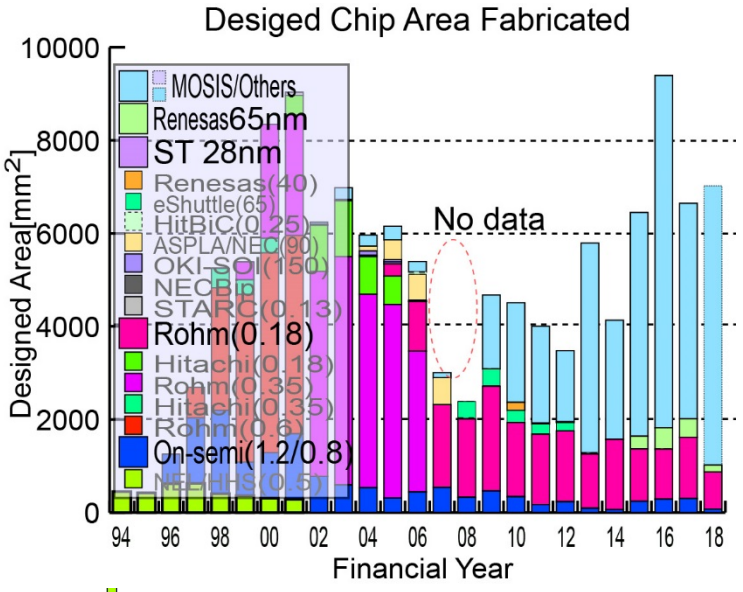
- Foundation: May 1996
  - As inter-university facilities in University of Tokyo.
- Staffs(Sept. 2019)
  - Prof. :**2**, Assoc. Prof. :**2**, Lecturer: **2**, Asst. Prof. :**2**
  - Visiting Prof. : **1** （NEC）
  - Supporting Staffs: Prof. **1**, Assoc. Prof.: **1**
- Steering Committee, Advisory Committee
- Registered users (Professors): ~800

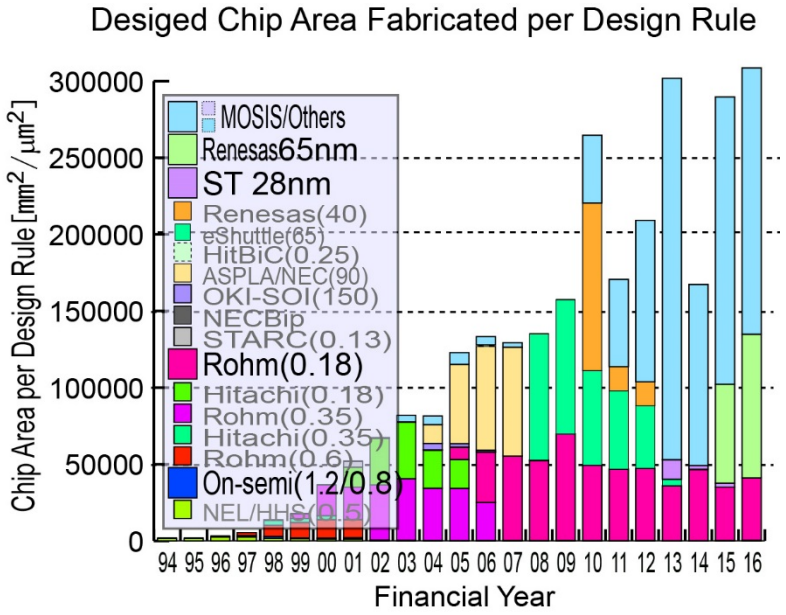
Chip Fabrication Services

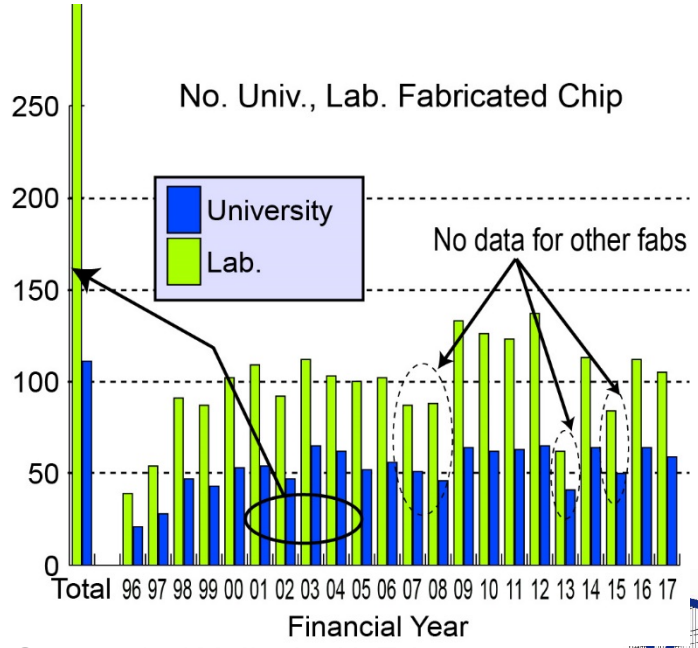


Trends of Chip fabrication





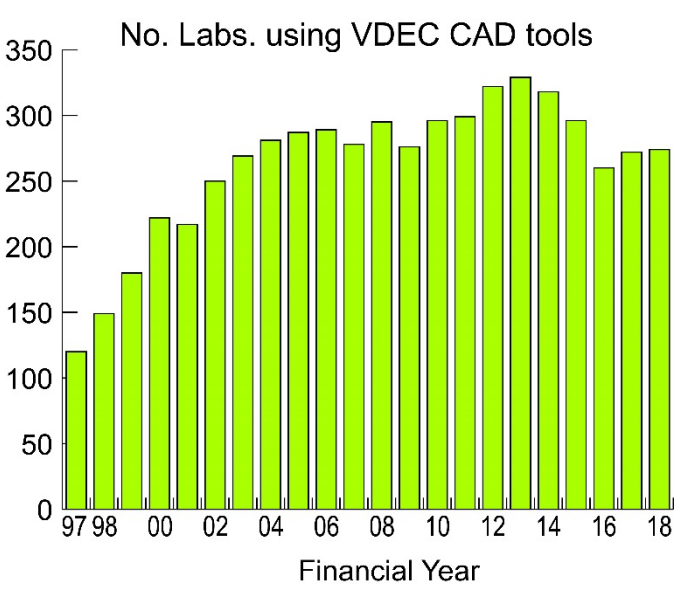


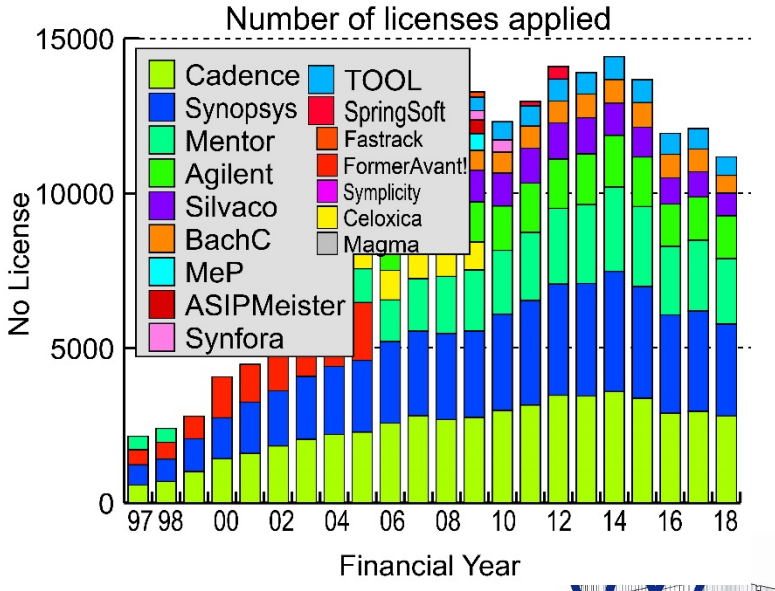


CAD tools

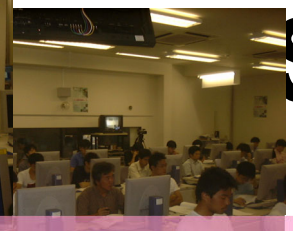
- CADENCE
  Logic Design, P&R, Interactive Design
- Synopsys
  Logic Design, Timing/Power, Simulators, P&R, HSPICE, TCAD

  500 ~ 1000 licenses for each to cover all the Japanese Universities & College
- Mentor HEP
- Silvaco/SmartSpice
- Keysight RFDE/ADS
- Sharp Bach C
- TOOL Lavis



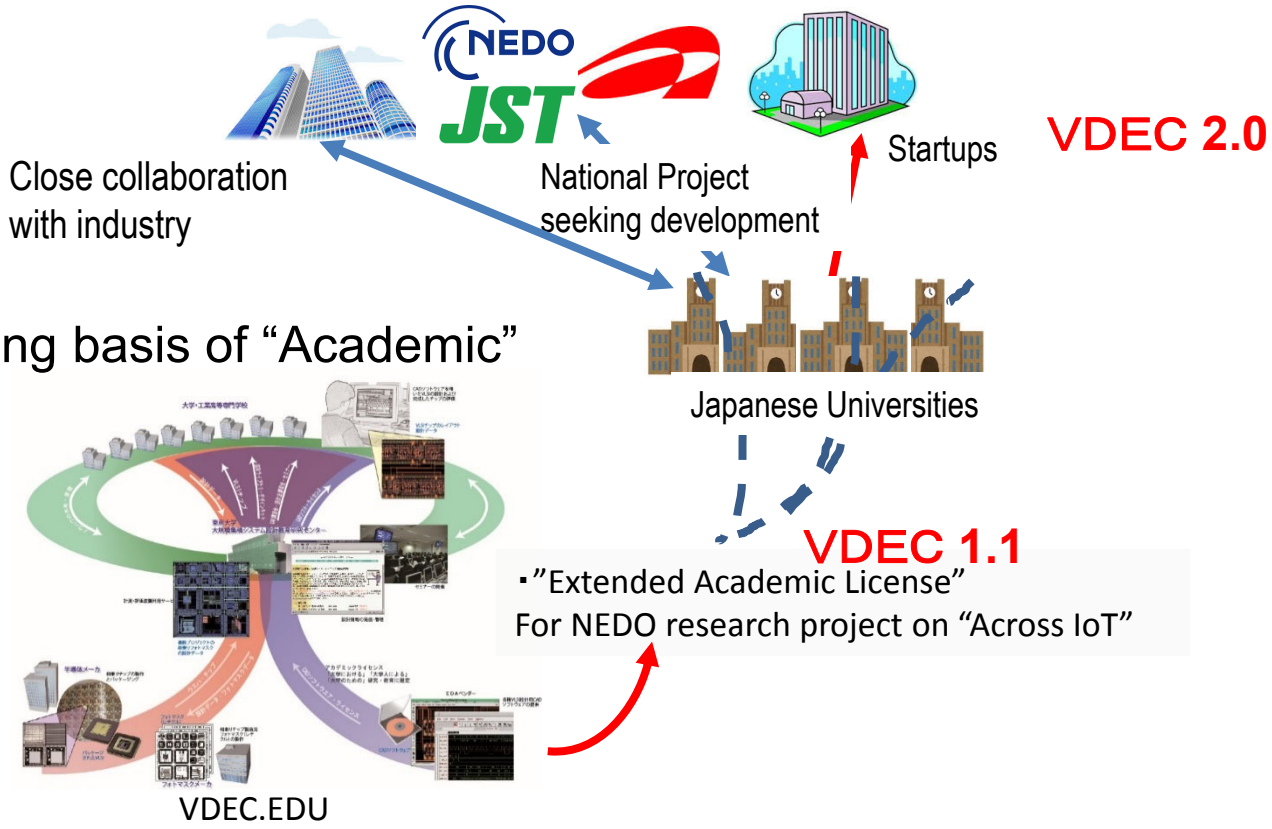


Seminars



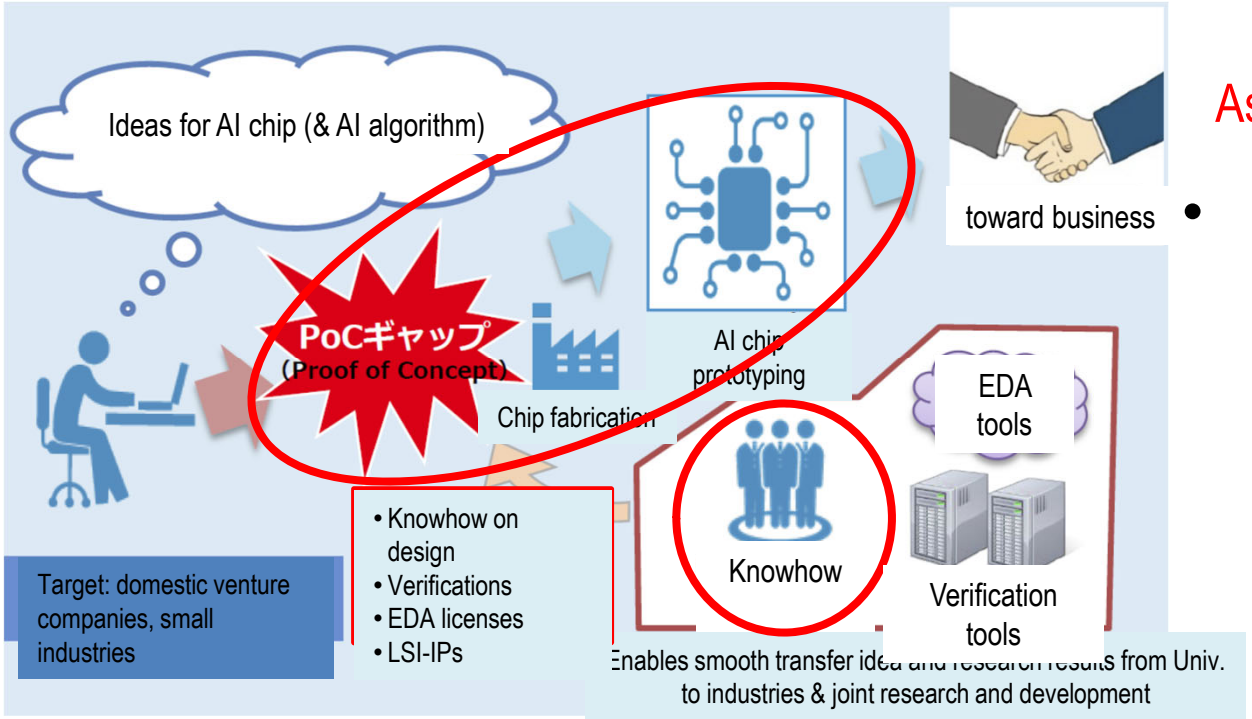
- CAD tool seminars（Aug. ～Sep. & Jan. ～Mar.）
  Tokyo area & Video streaming for Satellite campus
- VDEC Refresh Seminar（June~July）
  Analog course, RF course, Digital course & Advance design course
- VDEC Designer Forum（Sep.）
  2-day workshop （97 Kyoto, 98 Kyushu, 99 Sendai,
  00 Hiroshima, 01 Kanazawa, 02 Okinawa, 03 Hokkaido, 04 Fukuoka,
  05 Yugawara, 06 Kochi, 07 Hokkaido, 08-13 Tokyo,
  14-15 Kanazawa, 16 Tokyo, 17 Fukuoka, 18 Hokkaido, 19 Yamagata）

Step Toward VDEC 2.0
Platform for Advanced Chip design



- Maintaining basis of “Academic”

AI Chip Design Platform



As a part of VDEC 2.0 activities

- AI is fast growing area
  - Fast idea-to-chip implementation for larger design is essential
  - Time-lag for chip implementation is not preferable
  - Huge chip with high-memory bandwidth
    → Larger design efforts

AI Chip Design Center

- Established by VDEC & AIST in 2018, by METI & NEDO funding
  - Platform for AI chip design in small company and startups
  - EDA tools for engineering samples
  - Verification platform by logic emulator
  - LSI-IP for AI chip design
  - Forum, seminars & materials for AI chip design
  - Chip fabrication gateway for the Advanced process for AI chip

RISC-V: Open Core Hardware

- RISC-V & Agile design
  - Important for hardware design in rapid growing area...
- RISC-V project (by NEDO)
  - TEE
- ... May be RISC-V emulation model on Hardware emulator for further architecture design evaluation
- Open hardware
  → Will have Evening discussion at coming ISSCC 2020, Feb. 2020 in San Francisco

Future plan of VDEC

the University of Tokyo

School of Engineering
School of Science
....
Institute of Industrial Science (IIS)
....
VDEC

May 1996 ~ Sept. 2019

- VDEC has been a independent organization in the University of Tokyo
- Faculties in VDEC also belong to School of Engineering

the University of Tokyo

School of Engineering
Dept. of EE
....
Institute of Engineering Innovation
System Design Center (d.lab)

Oct. 2019 ~

- The University of Tokyo decided to empower "Semiconductor/design" research area, and establish a new center "d.lab" in the School of Engineering
- VDEC will be one division of "d.lab"
- Functionality of VDEC will be continue & empowered

東京大学 THE UNIVERSITY OF TOKYO