Hennessy and Patterson, Computer Architecture: A Quantitative Approach: Benefits its Japanese Translation Brought and Final 6th Edition

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Outline

- Pater-Henne and Henne-Pater
- Transition of the original and translated book of Computer Architecture a Quantitative Approach
  - 1st Edition and Historical translation
  - 2nd and 3rd Edition
  - Then, 4th Edition
  - Struggle on 5th Edition
  - Agony on 6th Edition
- Concluding remarks

Pater-Henne and Henne-Pater

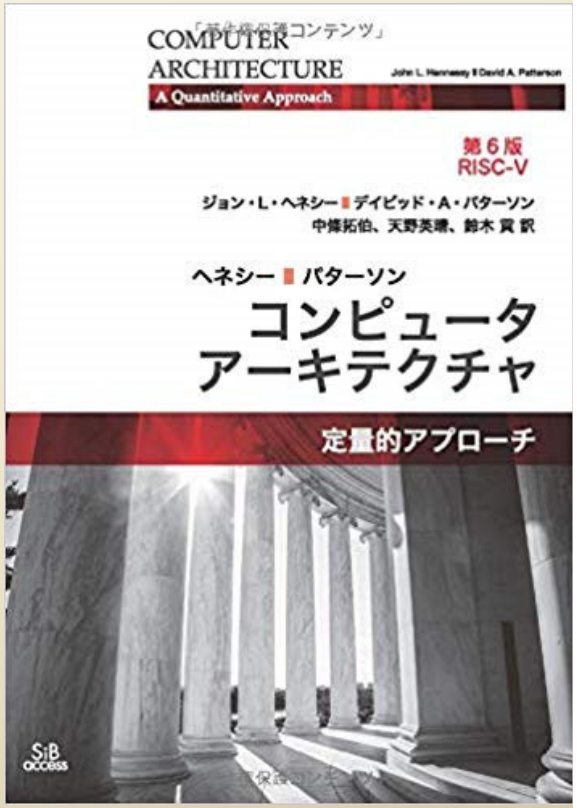
Computer Architecture, Sixth Edition: A Quantitative Approach

John L. Hennessy and David A. Patterson

コンピュータアーキテクチャ [第6版]定量的アプローチ

- H.Nakajo,H.Amano,M.Suzuki
- RISC-V based
- For graduate students

So-called Henne-Pater

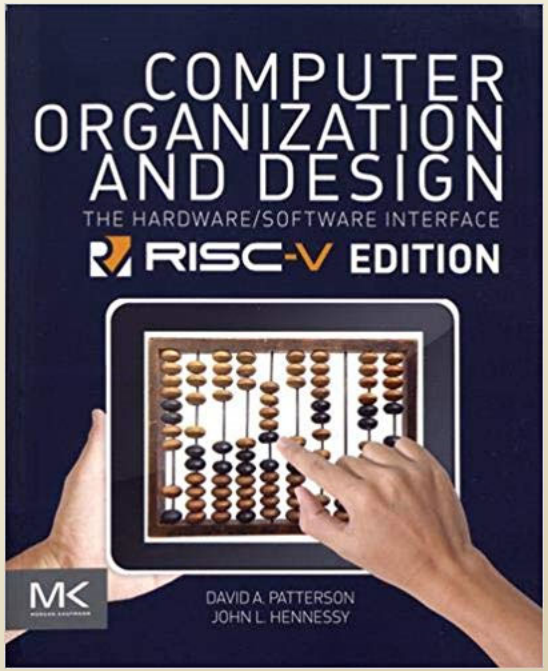


Pater-Henne and Henne-Pater

Computer Organization and Design RISC-V Edition: The Hardware Software Interface

コンピュータの構成と設計 第5版

- Mitsuaki Narita
- MIPS based
- Undergraduates
- When RISC-V version?

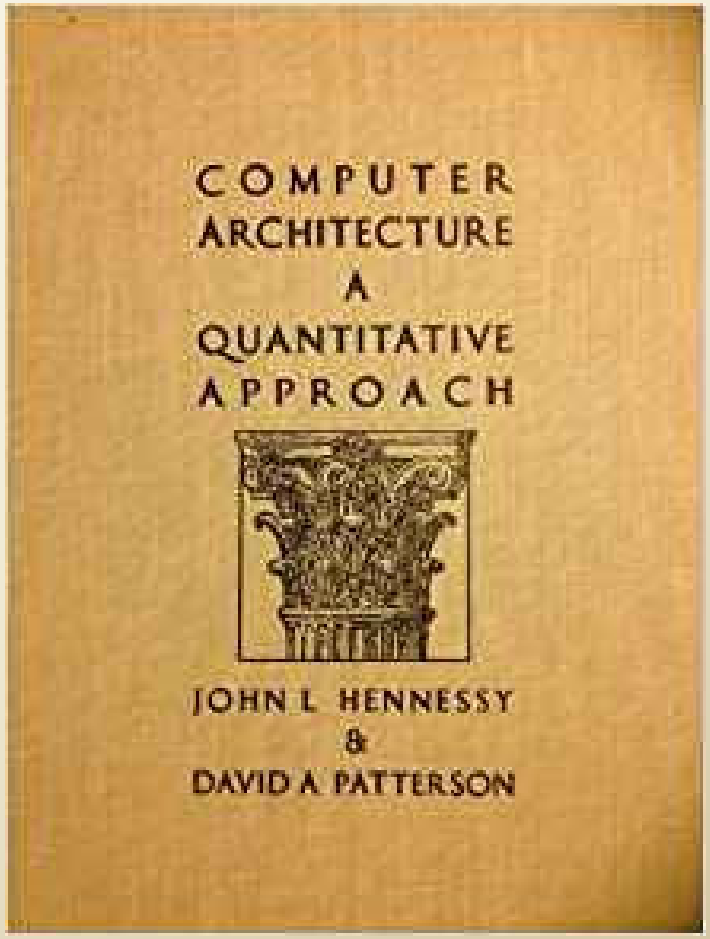


Transition of Henner-Pater

Computer Architecture
a Quantitative Approach

- ✓April 1990
- ✓784 pages

- ✓First of all …
  “Read H & P!”
- ✓In confusion …
  “Read H & P!”



Historical Translation of 1st Edition

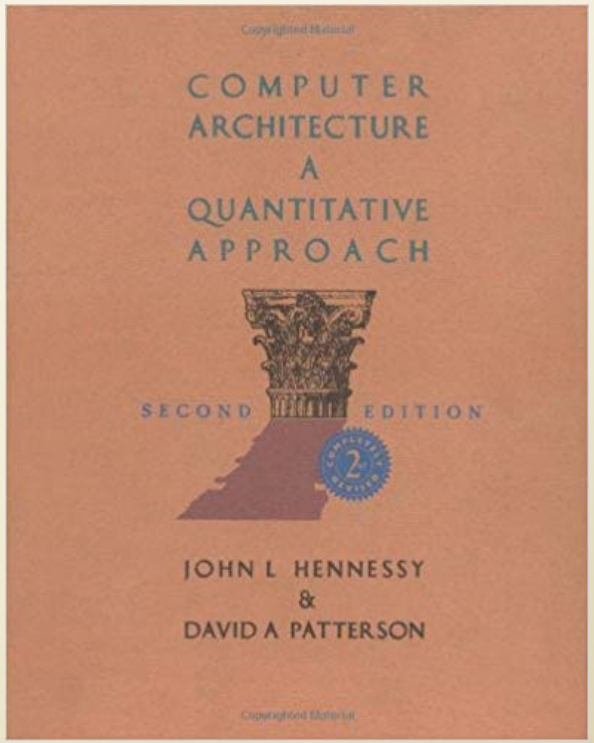
◆Translation of 1st Edition

- ✓May 1993
- ✓S.Tomita,H.Niimi,K.Murakami
- ✓Price：12,233 JPY

1 コンピュータ設計の基礎
2 性能とコスト
3 命令セットの設計-種々の方式と原理
4 種々の命令セットと使用状況の測定
5 プロセッサ実現技術の基本
6 パイプライン処理
7 ベクトル・プロセッサ
8 記憶階層の設計
9 入出力
10 今後の方向
付録(コンピュータの演算法
命令セットの一覧表
命令実行頻度分布の詳細
命令実行時間分布と命令実行頻度分布
RISCアーキテクチャのサーベイ

2nd Edition

◆Computer Architecture a Quantitative Approach, 2nd Edition



✓August 1995

1. Fundamentals of Computer Design
2. Instruction Set Principles and Examples
3. Pipelining
4. Advanced Pipelining and Instruction-Level Parallelism
5. Memory-Hierarchy Design
6. Storage Systems
7. Interconnection Networks
8. Multiprocessors

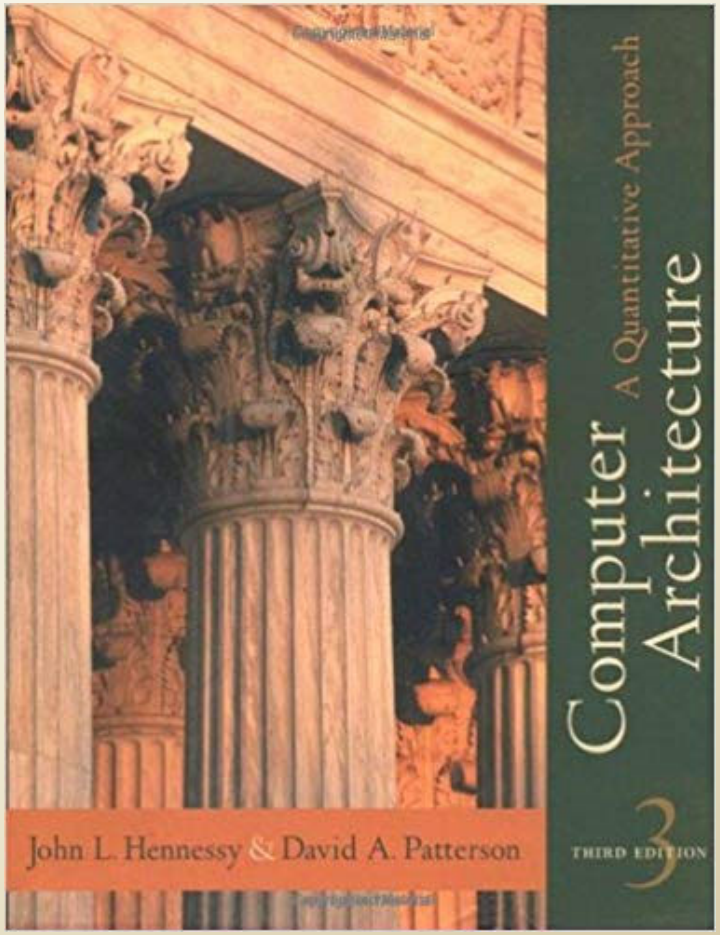
Appendix: A: Computer Arithmetic, B: Vector Processors, C: Survey of RISC Architectures, D: An Alternative to RISC: Intel 80x86 E: Implementing Coherence Protocols

3rd Edition

◆Computer Architecture a Quantitative Approach, 3rd Edition

✓May 2002

✓1,136 pages



3rd Edition ToC

1. Fundamentals of Computer Design
2. Instruction Set Principles and Examples
3. Instruction-Level Parallelism and its Dynamic Exploitation
4. Exploitation Instruction-Level Parallelism with Software Approach
5. Memory-Hierarchy Design
6. Multiprocessors and Thread-Level Parallelism
7. Storage Systems
8. Interconnection Networks

Appendix: A: Pipelining: Basic and Intermediate Concepts
B: Solution and Selected Exercises
C: Survey of RISC Architectures for Desktop, Servers and Embedded Computers
D: An Alternative to RISC: Intel 80x86
E: Another Alternative to RISC: VAX Architecture
F: The IBM 360/370 Architecture for Mainframe Computers
G: Vector processors
H: Computer Arithmetic
I: Implementing Coherence Protocols

Added chapters

2nd and 3rd Edition were not translated.

Then, 4th Edition

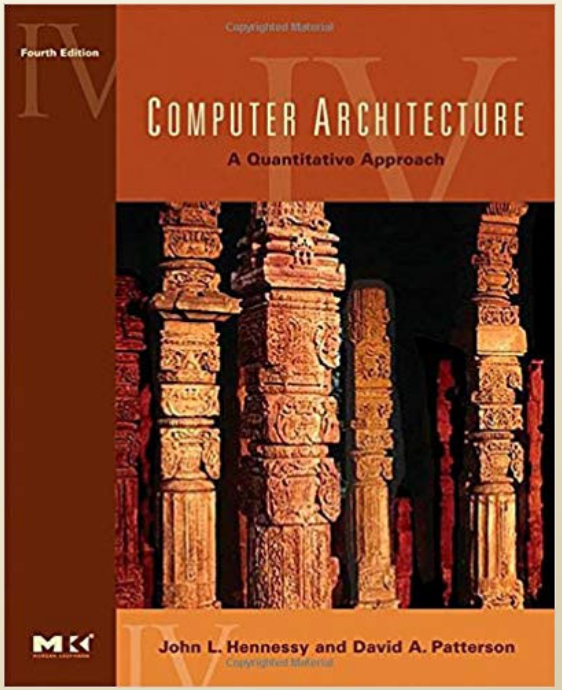
◆Computer Architecture a Quantitative Approach, 4th Edition

✓September 2006

✓Translation right in Nikkei BP

✓Shoei-sha might get the translation right

⇒ Exciting!



4th Edition ToC

✓704 pages (shortened?)

1. Fundamentals of Computer Design
2. Instruction-Level Parallelism and Its Exploitation
3. Limits on Instruction-Level Parallelism
4. Multiprocessors and Thread-Level Parallelism
5. Memory Hierarchy Design
6. Storage Systems

Appendix
- A: Pipelining: Basic and Intermediate Concepts
- B: Instruction Set Principles and Examples
- C: Review of Memory Hierarchy

4th Edition ToC

✓704 pages ⇒ more pages in CD-ROM

1. Fundamentals of Computer Design
2. Instruction-Level Parallelism and Its Exploitation
3. Limits on Instruction-Level Parallelism
4. Multiprocessors and Thread-Level Parallelism
5. Memory Hierarchy Design
6. Storage Systems

Appendix
- A: Pipelining: Basic and Intermediate Concepts
- B: Instruction Set Principles and Examples
- C: Review of Memory Hierarchy

CD-ROM:
- D: Embedded Systems
- E: Interconnection Networks
- F: Vector Processors
- G: Hardware and Software for VLIW and EPIC
- H: Large-Scale Multiprocessors and Scientific

Applications
- I: Computer Arithmetic
- J: Survey of Instruction Set Architectures
- K: Historical Perspectives and References

Translation Team

- ✓Started in Dec. 2006
  - ➢ Hironori Nakajo (Chief)
  - ➢ Kenji Kise
  - ➢ Toshinori Sato
  - ➢ Hideharu Amano

  Editor: Noboru Tomizawa of SiB Access

What shall we do for the CD-ROM?

Call for Translators

Biggest Mailing-List(SWoPP-ML)

To all SWoPP-ML members：

This is not “Call for Papers” nor “Call for Participation!”
This is “Call for Translators!”

Last year, Hennessy & Patterson’s Computer Architecture: A Quantitative Approach 4th Edition was published, and the translation is currently underway. However, the CD-ROM in the original is not a target to be translated.

Call for Translators

This CD-ROM is copyright free in the original, but it is regrettable to keep it in English. So we will recruit translation members to translate, edit, and attach them as an appendix.

Please entry and join the translator team!

Qualification：

1. Young and Familiar in computer architecture related to computer science
2. Enthusing in advancing computer research
3. Punctual
4. Approved from a supervisor if students

Call for Translators

Benefit：

1. List your name in the book
2. 2 translated books will be given
3. Will nvite you to our party for publish

Those who meet the above qualifications, those who think that they deserve it, those who have already translated some to bring them to the world, and those who are currently holding resources, etc.

Would you like to challenge?

Translation volunteers for the CD-ROM

Appendix

D：Kiyofumi Tanaka and Takefumi Miyoshi
E：Michihiro Koibuchi and Hiroki Matsutani
F：Shoichi Hirasawa and Yuri Nishikawa
G：Hajime Shimada and Noriaki Suzuki
H：Takashi Toyoshima, Shuji Yamamura and Akihiro Chiyonobu
I：Naoki Yonezawa and Masato Yoshimi
J：Hidetsugu Irie
K：Mitsugu Suzuki

Thank you very much!

Started to work

- Careful of mis-translation
- Difficult expressions for non-native

  ⇒ help from friends in US
- Cannot figure out the intentions

  ⇒ Ask an ex-student of Hennessy

  ⇒ The ex-student could not get it

Looks like scribbling with insufficient editorial work

The last work.. Finally

- Worked in an apartment in Hakone with Onsen (hot spring)
  (Thanks to the late Mr. Masaki Kudo)

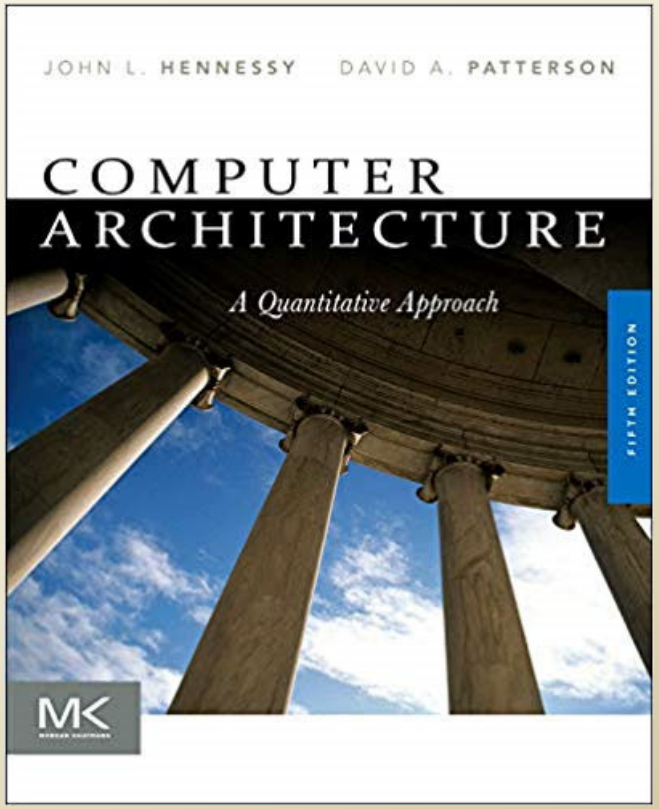
- Feb. 20th 2008

- At a party for publish
  ⇒ Everybody signed on blank pages

Don't care of severe criticism in Amazon!

5th Edition

- Computer Architecture a Quantitative Approach, 5th Edition
  - ✓September 2011
  - ✓From Shoei-sha again
  - ✓Not CD-ROM but Online
  - ✓Already known know-how to translate



5th Edition ToC

✓856 pages

1. Fundamentals of Quantitative Design and Analysis
2. Memory Hierarchy Design
3. Instruction-Level Parallelism and Its Exploitation
4. Data-Level Parallelism in Vector, SIMD, and GPU Architectures
5. Thread-Level Parallelism
6. Warehouse-Scale Computers to Exploit Request-Level and Data-Level Parallelism

Added chapters

Appendix
- A: Instruction Set Principles
- B: Review of Memory Hierarchy
- C: Pipelining: Basic and Intermediate Concepts

New translation team

- Hironori Nakajo (Chief)
- Hideharu Amano (Chief)
- Kenji Kise
- Toshinori Sato
- Mitsugu Suzuki

Editor from Shoei-sha

Big trap…

Awful editing by the editor

- Sophisticated sentences from translation
- The editor's way

  ⇒ ignoring translators' opinion

  ⇒ technical bugs
- Divided figures into tables and figures and re-number them

  ⇒ Different numbers from the original

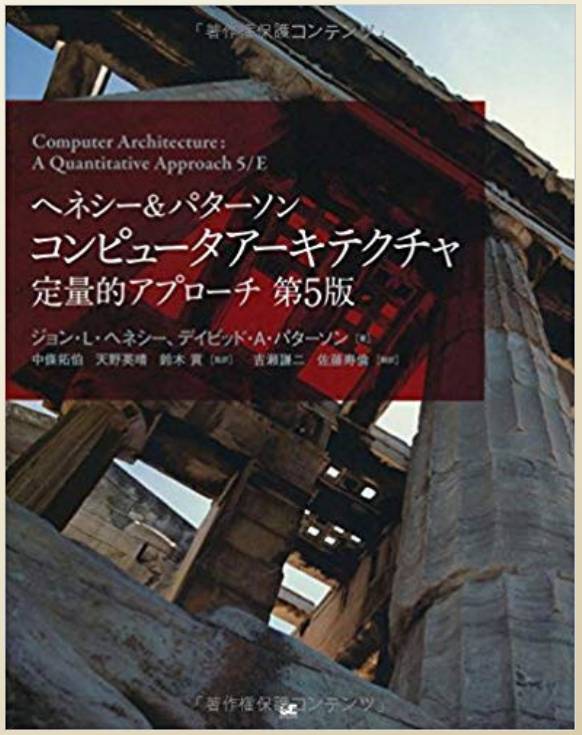
Put up with anger!

Then published

- March 2014
- Claim to anonymous opinion

If you want to critique the translation of this book, at least check it against the original, and don't swallow bitter anonymous reviews.

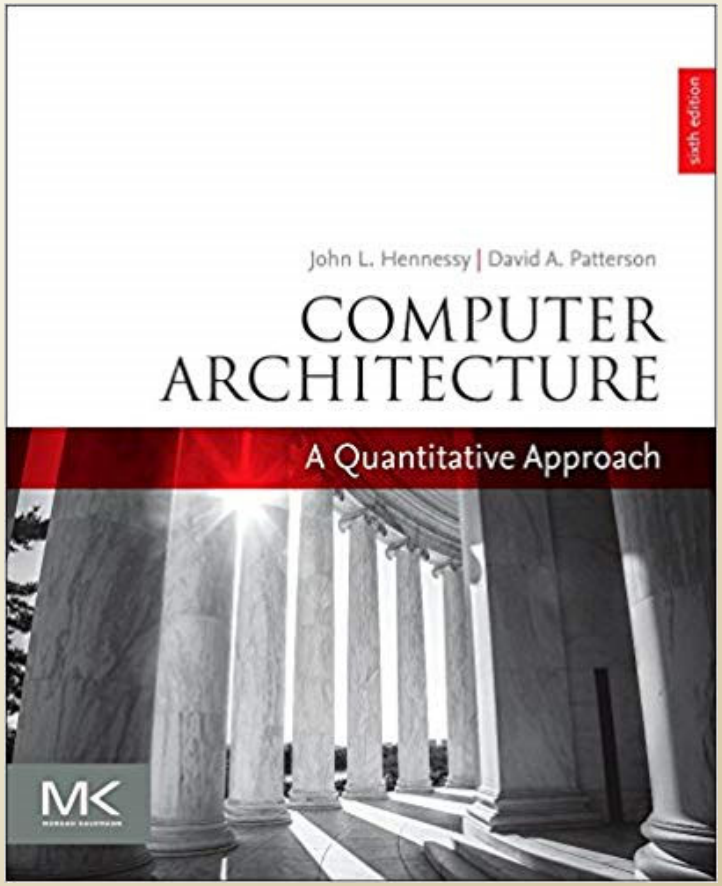
In order to convey the true value of the book to the world, we will continue to send information as long as time permits to correct misunderstanding in the world.



Final 6th Edition

◆Computer Architecture a Quantitative Approach, 6th Edition

- ✓December 2017
- ✓From MIPS to RISC-V
- ✓SiB Access got the translation right
- ✓The originalauthors got Turing Prize!



6th Edition ToC

✓936 pages

1. Fundamentals of Quantitative Design and Analysis
2. Memory Hierarchy Design
3. Instruction-Level Parallelism and Its Exploitation
4. Data-Level Parallelism in Vector, SIMD, and GPU Architectures
5. Multiprocessors and Thread-Level Parallelism
6. The Warehouse-Scale Computer
7. Domain Specific Architectures

Added chapter

Appendix
- A: Instruction Set Principles
- B: Review of Memory Hierarchy
- C: Pipelining: Basic and Intermediate Concepts

Easier way than before?

Shrink translation team

- Hironori Nakajo
- Hideharu Amano
- Mitsugu Suzuki

Mr. Tomizawa is the editor again

Start to get diff from 5th Edition

However, too optimistic …

Agony to bugs in the original and translation of 5th Edition

- Technical errors in 5th translation
  - ⇒ Dangerous in copying and pasting
- Unbelievable errors in the original
  - ⇒ Ex.: A figure in 5th Edition as it is

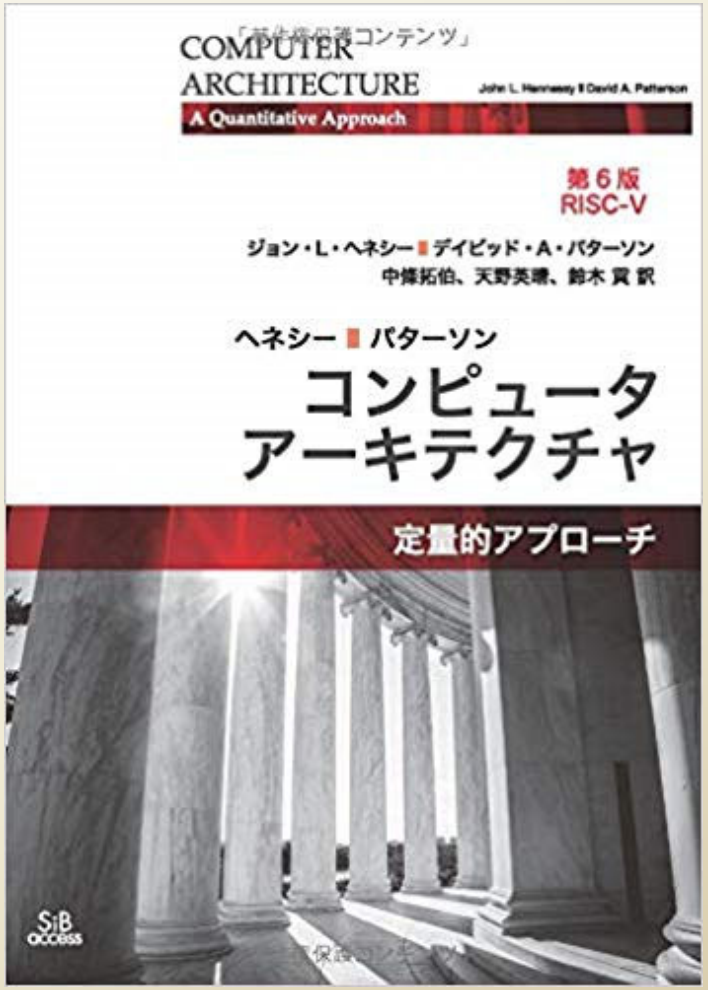
Please visit the following site.

http://am.ics.keio.ac.jp/wp/caqa6thproblem/

Doubts beget doubts in working

Thanks to RISC-V Day

- Spur towards today
  - ⇒ Sep. 25th 2019
- Sorry for remaining errors
- Will remove bugs from now on



Conclusion

- In my heart…
  - Is H & P a bible?
  - Should H & P be a textbook?
  - What is the next to H & P?

⇒ We will leave these answers to those who have purchased and read it.

We are all hoping the books will be sold fairly to avoid deficit of SiB Access.