Open Source EDA

Status, arguments, possibilities

Symbiotic EDA

- Yosys, open source synthesis tool for FPGA and ASIC
- SymbiYosys, open source formal verification tool
- free formal verification IP to verify RISC-V cores
- formal verification IP for verifying AXI interfaces

Symbiotic EDA

Symbiotic EDA & me

- Team of 10 engineers
- We write tools for digital circuit designers
- We sell support and development contracts
- clients in Silicon Valley

- Edmund Humenberger
- Open Source since 1993
- I try to make chip design fun again

Status of industry

- Cadence, Synopsys, Mentor
- Massive consolidation of chip industry
- Very few big employers
- No cool chip jobs
- App and web development gets all the attention, chip design is not interesting
- success in SW is much faster and much more likely than with chips
- Good students go for SW, not for chip design
- Funding available for SW, not for chip startups

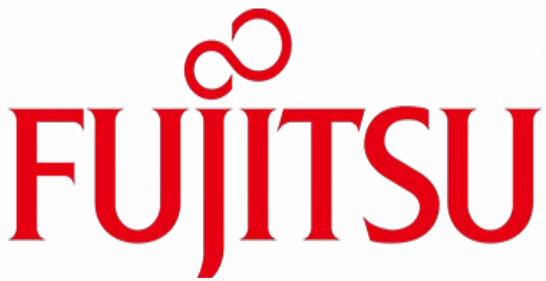
Status of industry

- Chip designs per year decrease, needed invest per chip designs increases.
- Very few chip startups
- Chip design errors are very costly.
  No experimentation.
  Industry very reluctant to try out new things.
- No innovation at design languages
- Only chips with a market volume of
  more than 1 Mio get manufactured.
- Chip industry is a stagnant, elite industry.

Learn from Linux

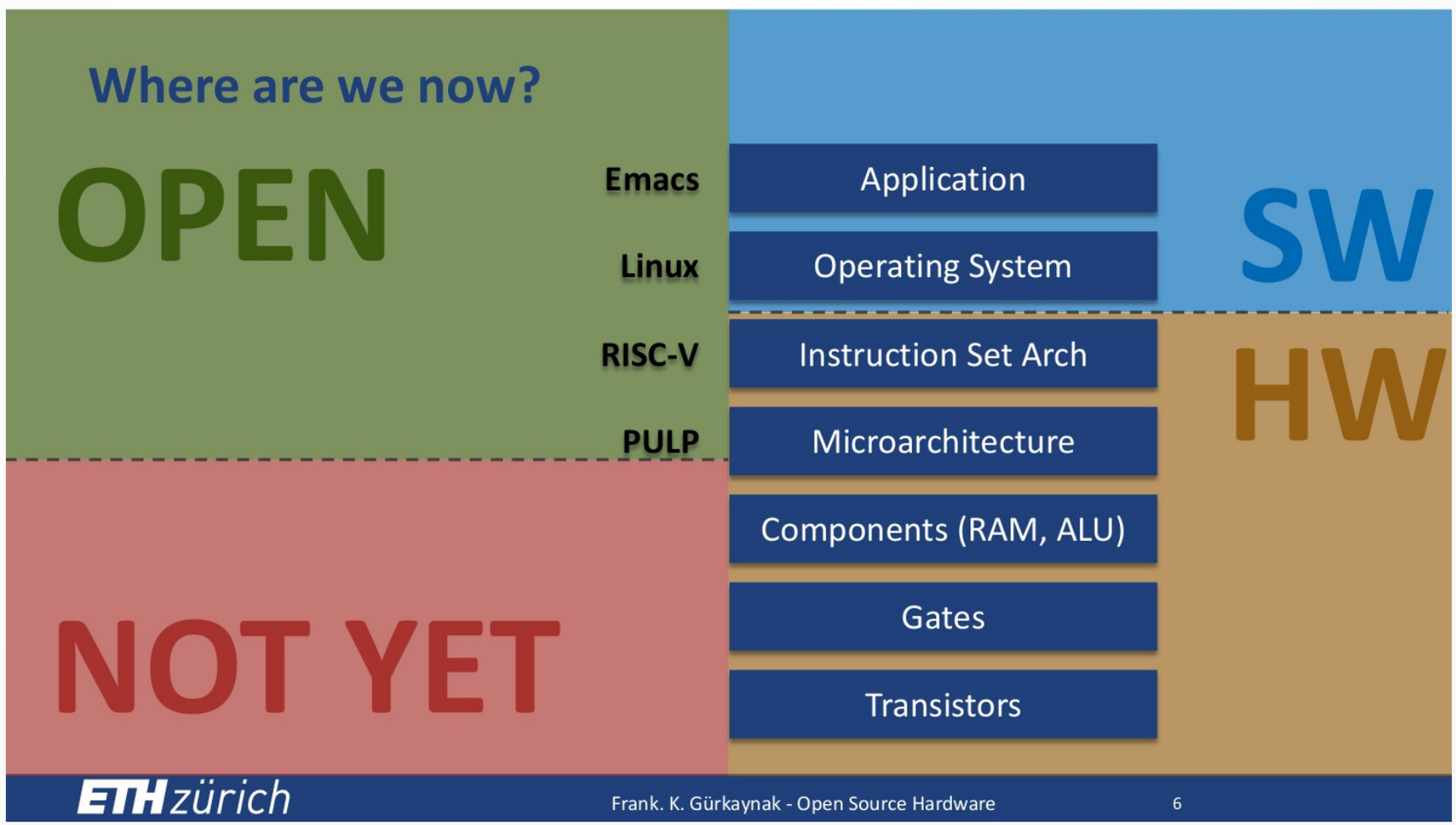
- open source facilitates innovation
- Linux, Python, git, … Facebook, Google, Amazon would not exist without OSS
- Open Source principles today do dominate the SW industry, for business reasons.
  Microsoft embraces Open Source
- Factor of success: synergy through transparency, depth and speed of cooperation.

Members of Linux Foundation



RESTART THE CHIP INDUSTRY

- Open standards



RESTART THE CHIP INDUSTRY

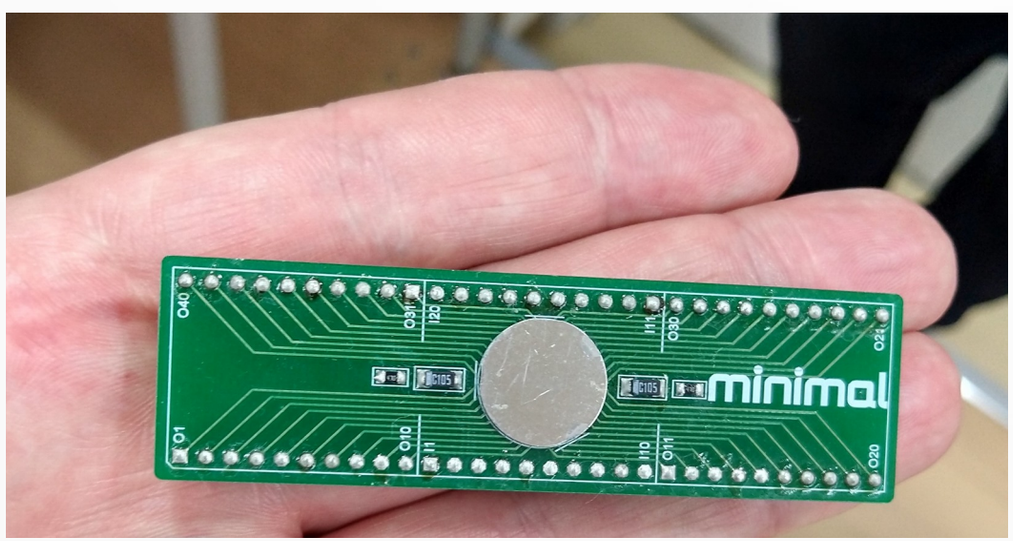
- Open design components
  - open access to PDKs and design blocks for everyone (Students, Makers, Innovators, self-funded Startups)
  - Share freely results and designs between Universities
  - Share commodity design blocks like analog blocks, RISC-V cores, interface blocks
  - share verification tools like riscv-formal

RESTART THE CHIP INDUSTRY

- Open tools
  - open access to EDA tools for everyone
  - make source code available of the tools so that innovators can adapt the tools themselves specific to their needs.
    - Symbiotic EDA
    - openROAD Darpa
    - many others

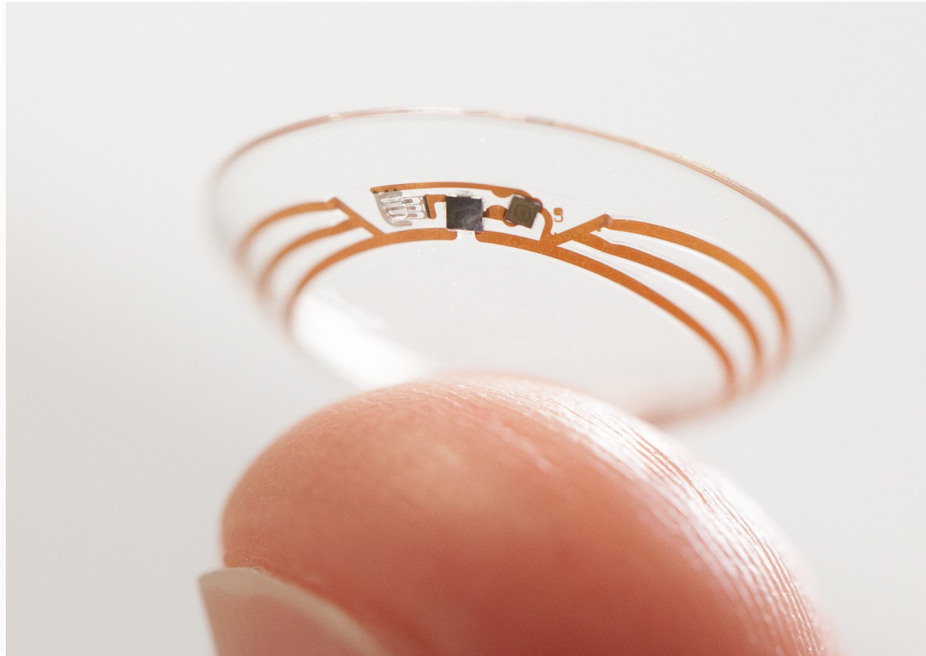
RESTART THE CHIP INDUSTRY

- new manufacturing
  - offer one up to many chips production fast and cheap



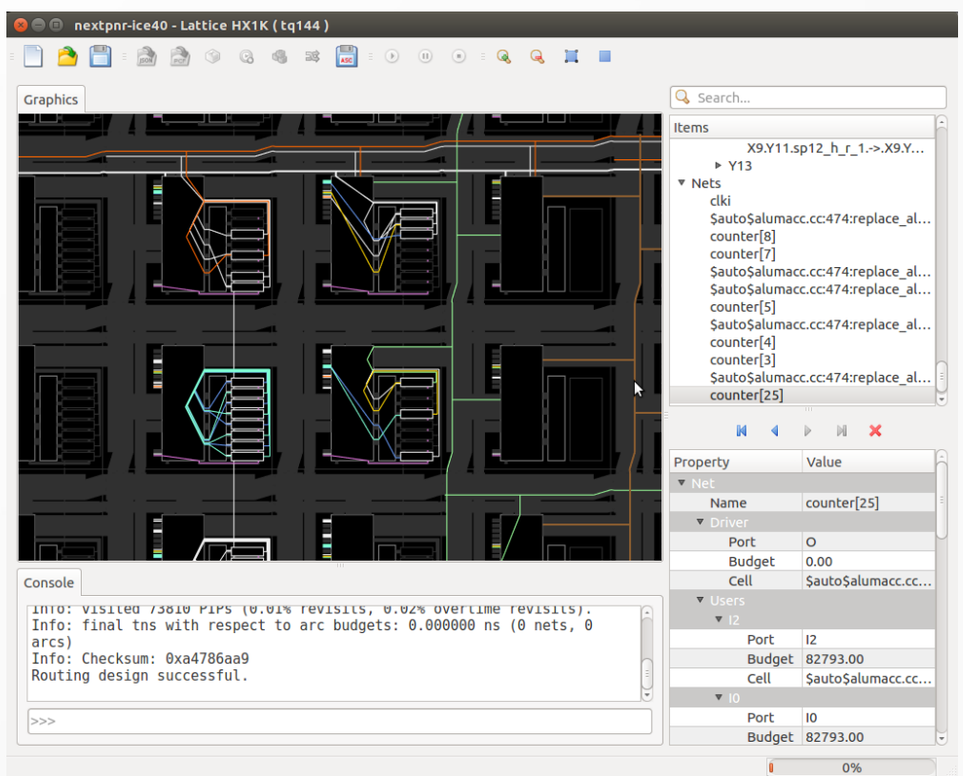
RESTART THE CHIP INDUSTRY

- Result will be a wave of new products
  - experimentation and fast learning about technology, products and markets
  - tailored to individual needs
  - manufacturing volume between 100 and 100.000 devices
  - IoT, Medical, Aerospace, Military, automotive, wearables

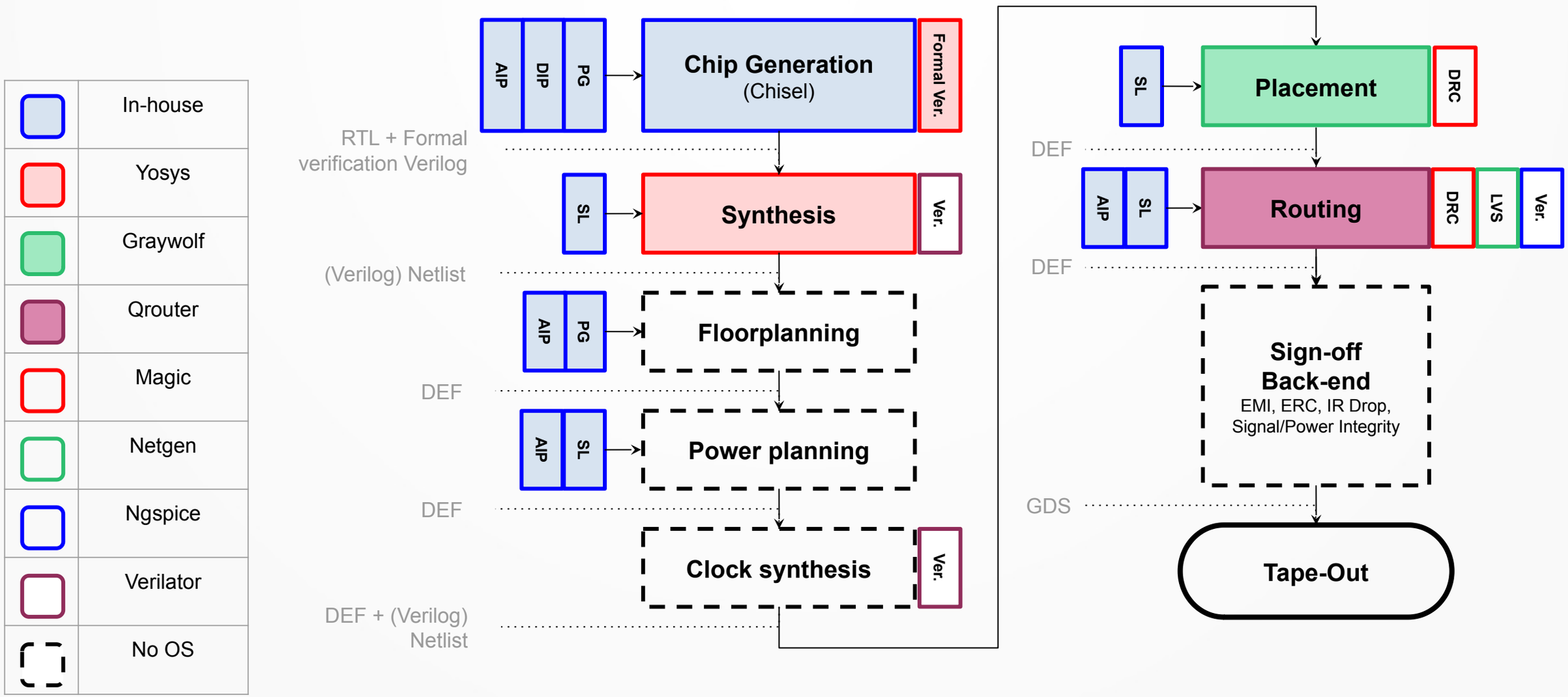


OS tools for FPGA

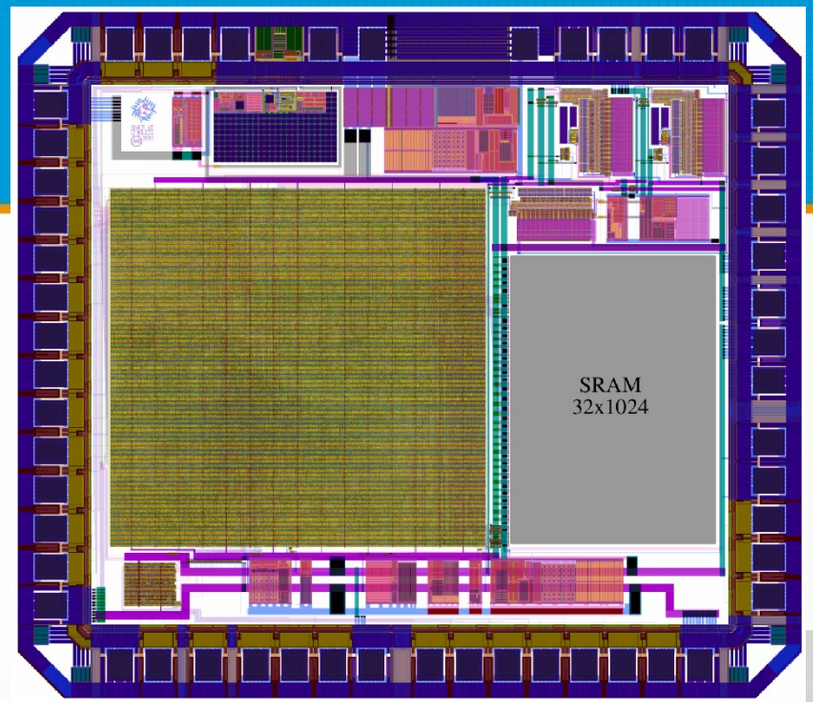
- maker-grade open source toolchain
  - Yosys, nextpnr, Icarus Verilog, Verilator, ...
- 10.000 designers
- Academia is using it
- large number of boards with Lattice FPGAs
- community is healthy and in full swing



OS TOOLS FOR FPGA



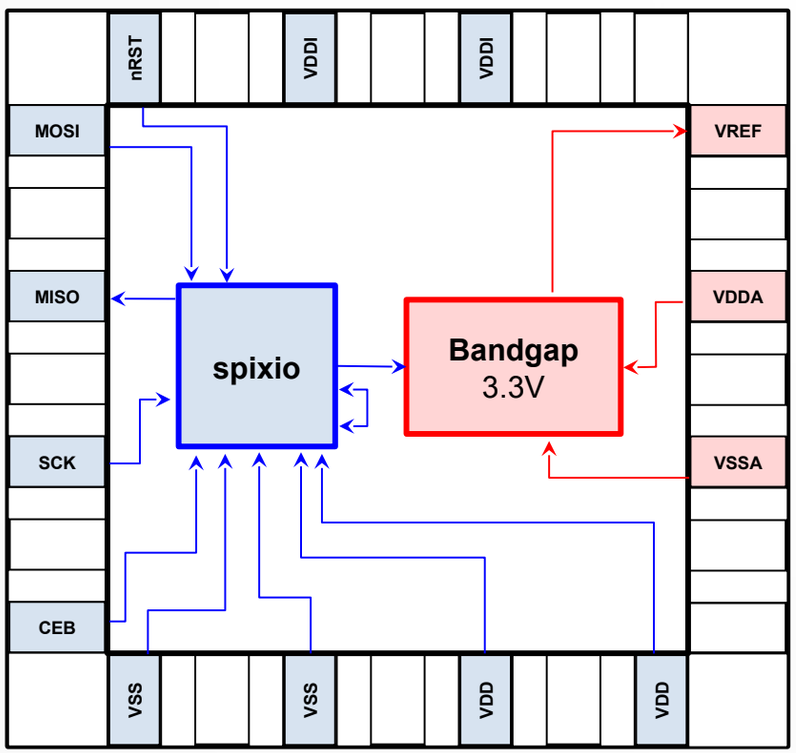
Raven Sept 2018

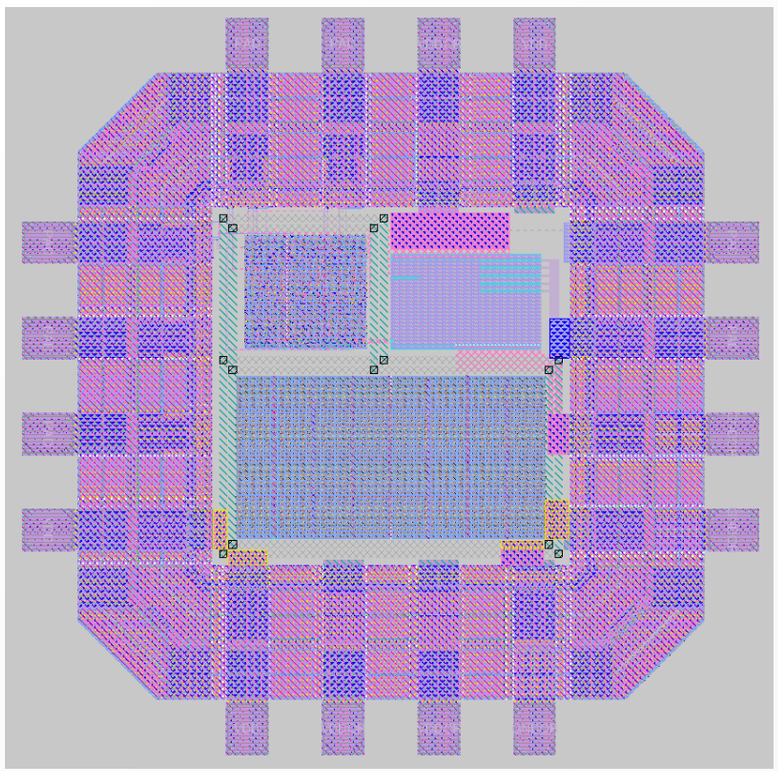


- Working microprocessor SoC:
  Designed and verified
- Chip simulated and layout drawn with
  all open-source tools
- PicoRV32 RISC-V core by Clifford Wolf
- QSPI

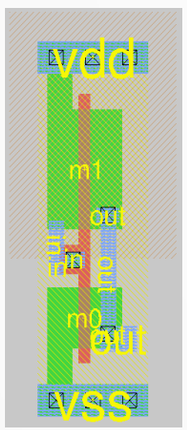
- X-Fab digital standard cells
- X-Fab padframe I/O (3.3V with both 3.3V and 1.8V core)
- X-Fab analog IP
- X-Fab 4kB-SRAM

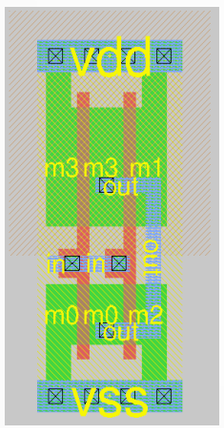
ASICone Nov 2019

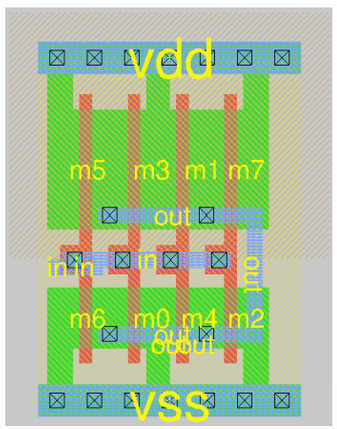


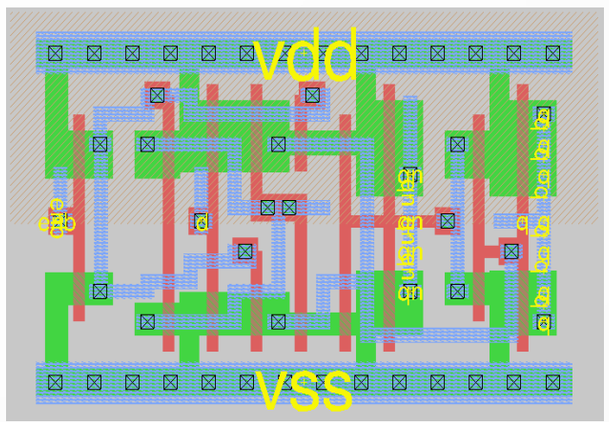


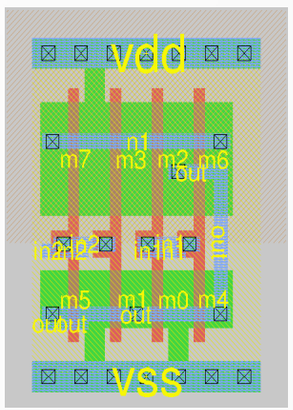
ASICone own std cells and analog blocks

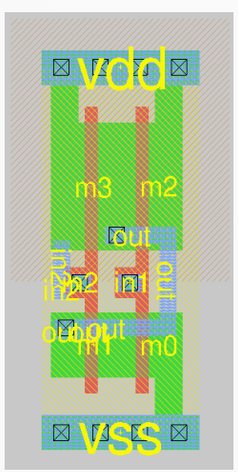


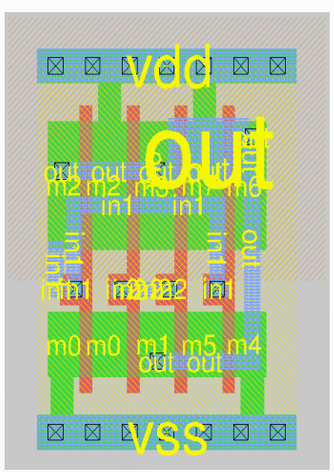


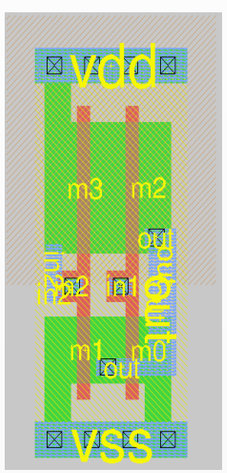


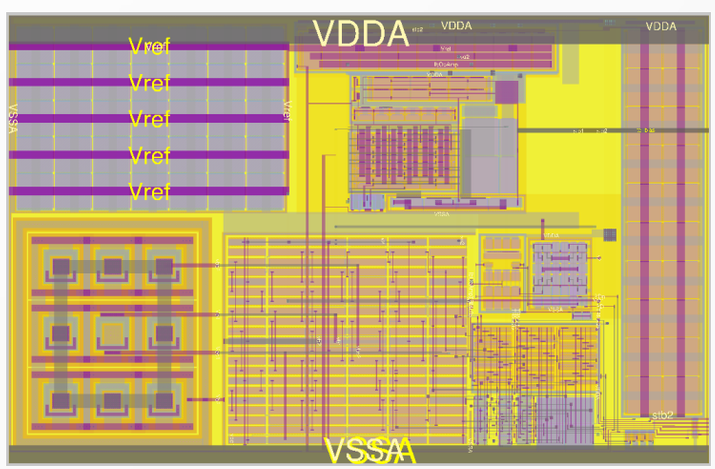




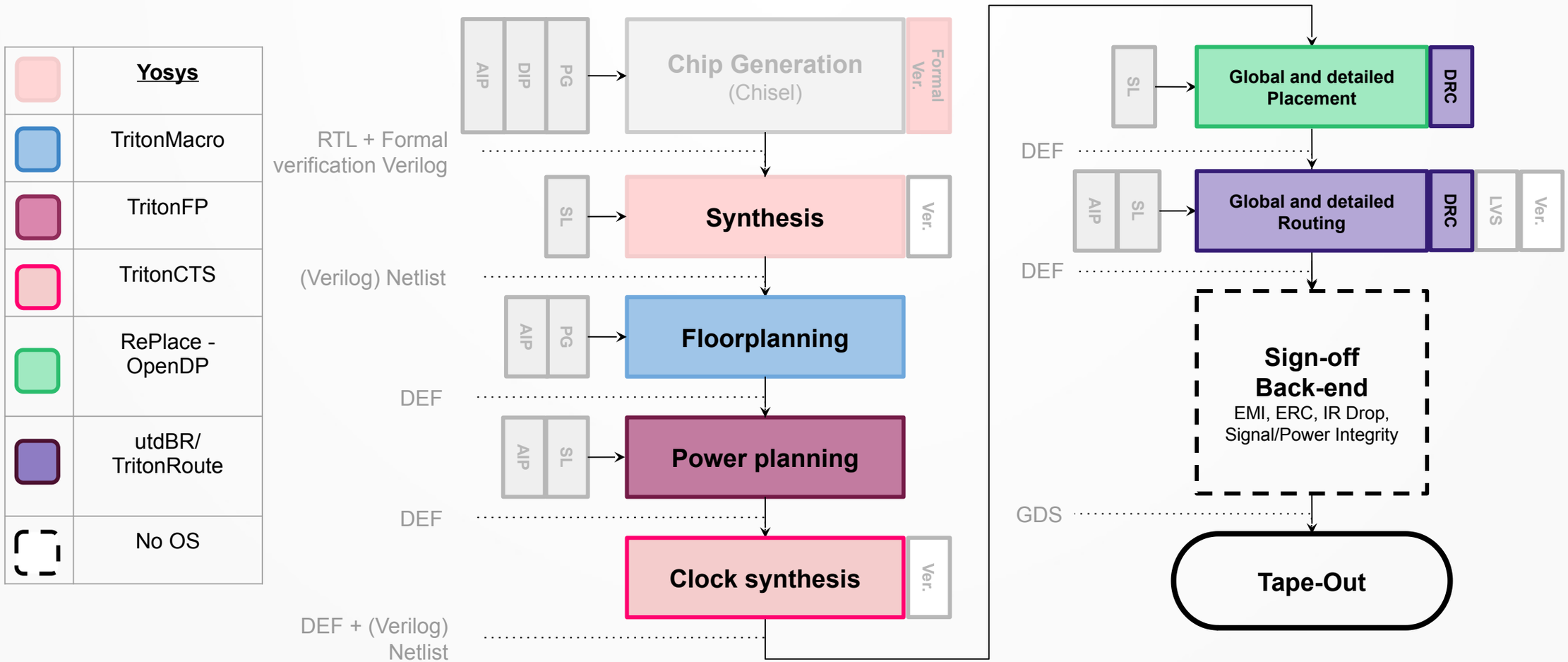








DARPA IDEA openROAD



Our future ASIC activities

- more analog blocks
- continuous improvement of tools
- ongoing tape outs to enable student tape outs
- search for development funding

Your next step?

- Talk to me edmund@symbioticeda.com
- Become partner in the endeavor to kickstart the electronics industry using tailor made chips

Thank you