CloudBEAR

Russian MCU / CPU History: How did we come to adopt RISC-V?

Denis Ivanov, Senior engineer

CloudBEAR introduction 1/2

- IP company:
  - was founded in **2015** in Russia
  - silver member of the **RISC-V** foundation
  - key team members have solid processor design experience in global companies
- Offers products:
  - Processor IP (MCU, Linux-capable cores)
  - Infrastructure IP (Interconnects, DMA, …)
- Provides services:
  - Processor IP customization
  - System-on-Chip integration
  - Custom SoC design with partner company

CloudBEAR introduction 2/2

Russian IC design centers	Arch license	Own micro-arch	Soft ecosystem
Baikal (ARM, MIPS)	needed	no	yes
Elvees (ARM, MIPS)	needed	no	yes
MCST (Elbrus, SPARC)	in-house	yes	no
NIISI (MIPS)	needed	yes	yes
Module (ARM)	needed	no	yes
Milandr (before on ARM)	needed	no	yes
CloudBEAR (RISC-V)	open	yes	yes

Milandr recognized RISC-V and invested into CloudBEAR in 2017!

Partner introduction

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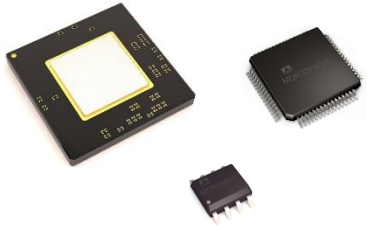
Milandr

- 130 IC design engineers
- Full cycle ASIC design
  - Analog RF design
  - Power management
  - Backend design
  - Digital design
  - IP design
  - Package design



- 150+ completed ASICs
- Experience with 22nm-180nm
- MCUs, Ethernet, Transceivers, ADC/DAC, RF
- **New SoCs based on RISC-V!**

tsmc GLOBAL FOUNDRIES

X-FAB MIXED-SIGNAL FOUNDRY EXPERTS TOWERJAZZ

HHGrace

- Assembly and test house
- 50 engineers

Custom SoC platforms

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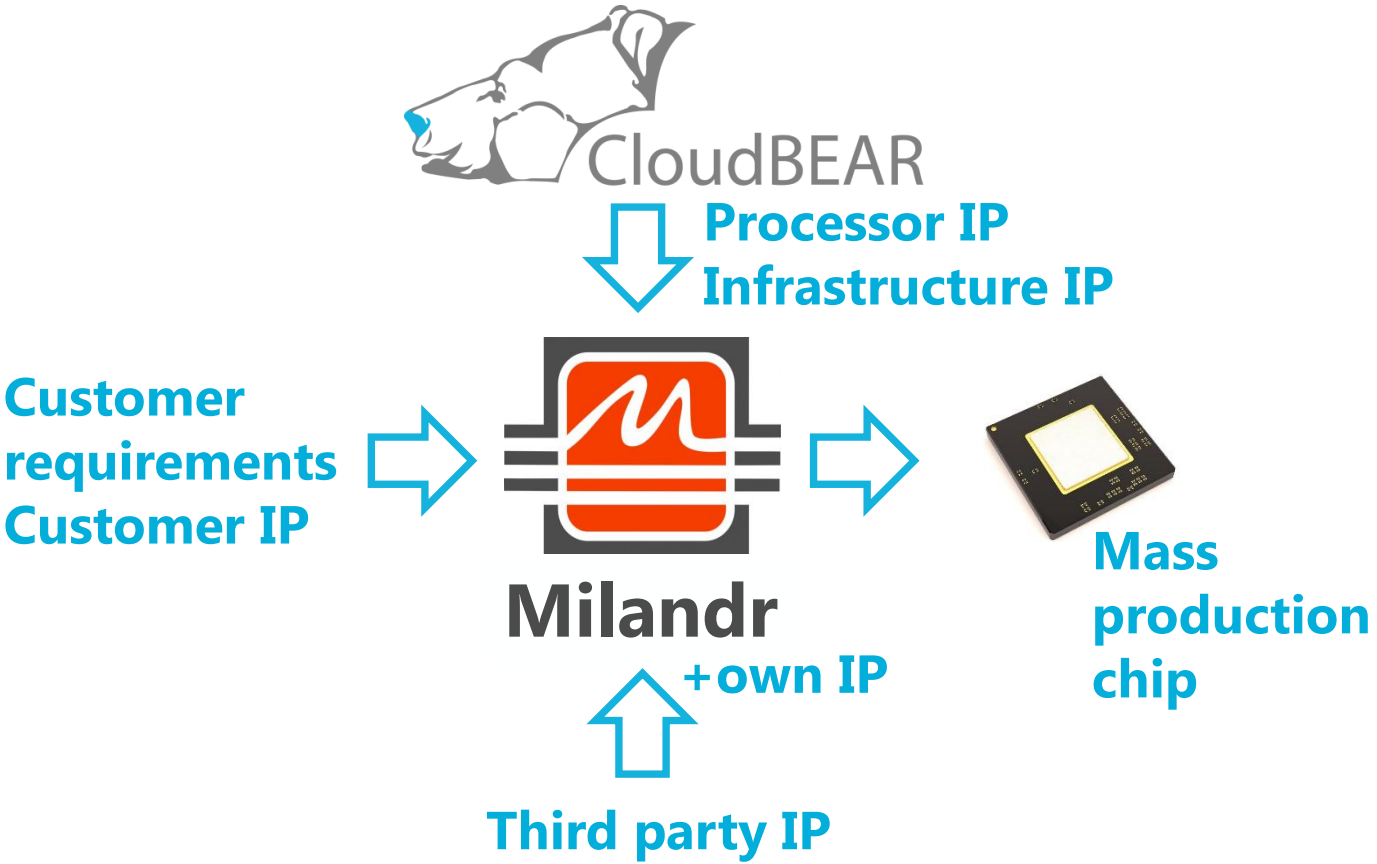
Low Power MCU / Sensor Hub	Motor control / Predictive maintenance	Application processor / AI edge processor
BM Series based	**BR Series based**	**BI Series based**

Milandr

Custom SoC turnkey design service



Low power MCU / Sensor hub platform

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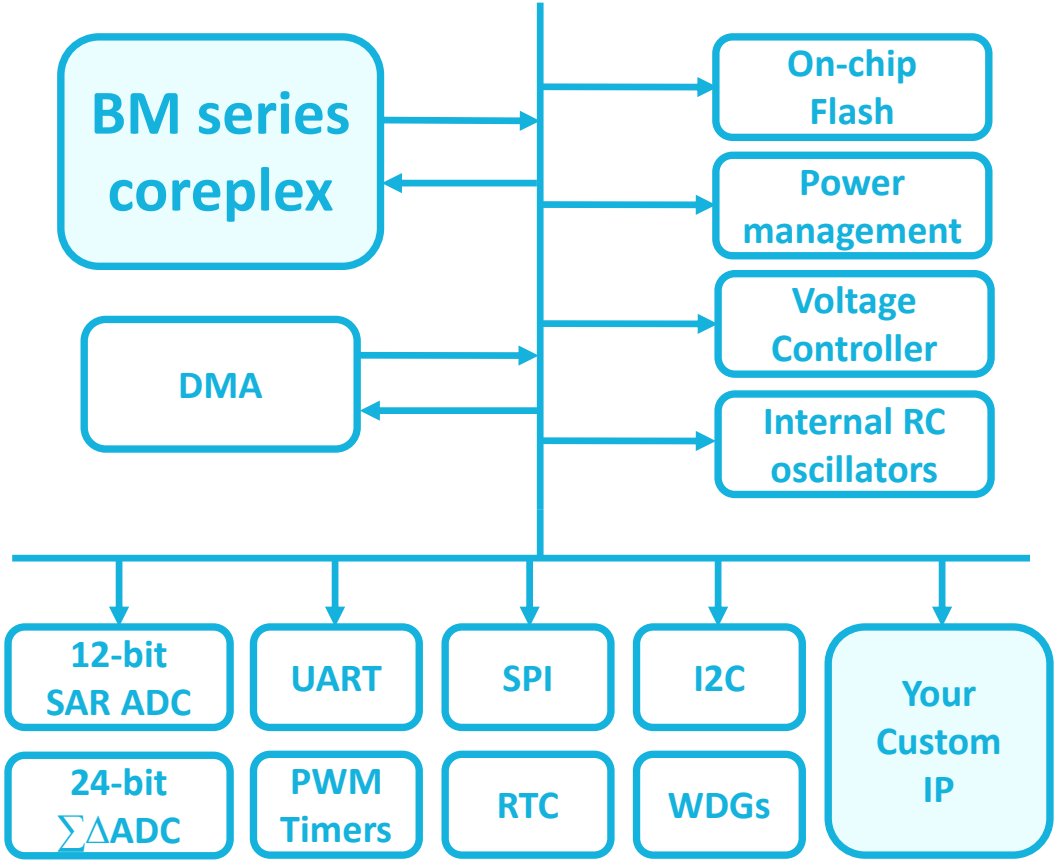
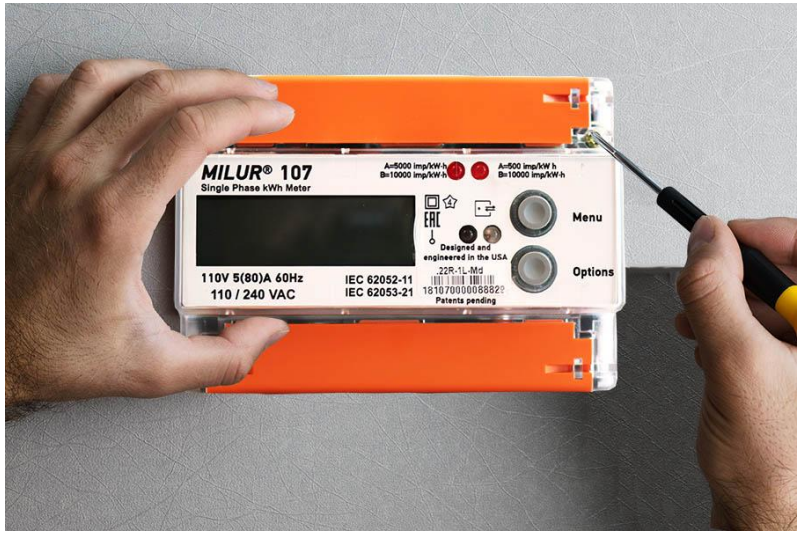


- TSMC 90nm LP
- Ships in millions
- New gen based on RISC-V

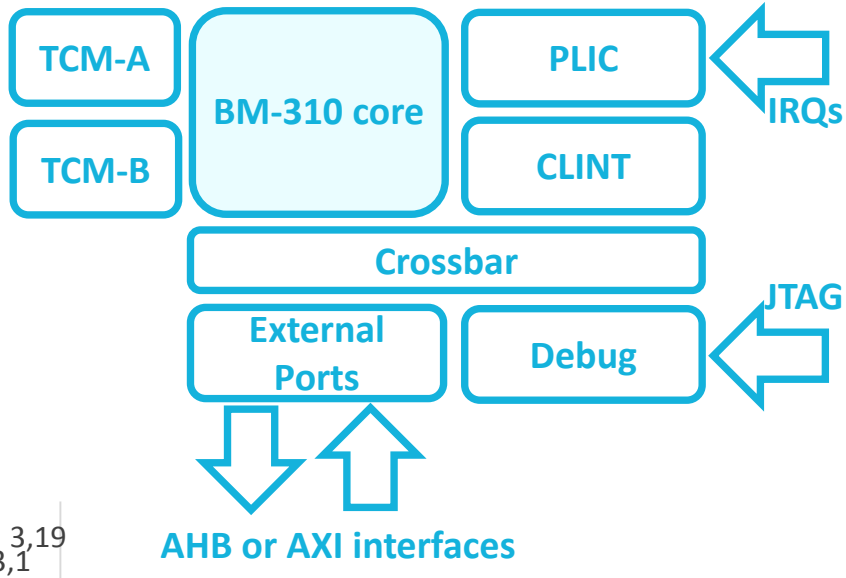
Milandr

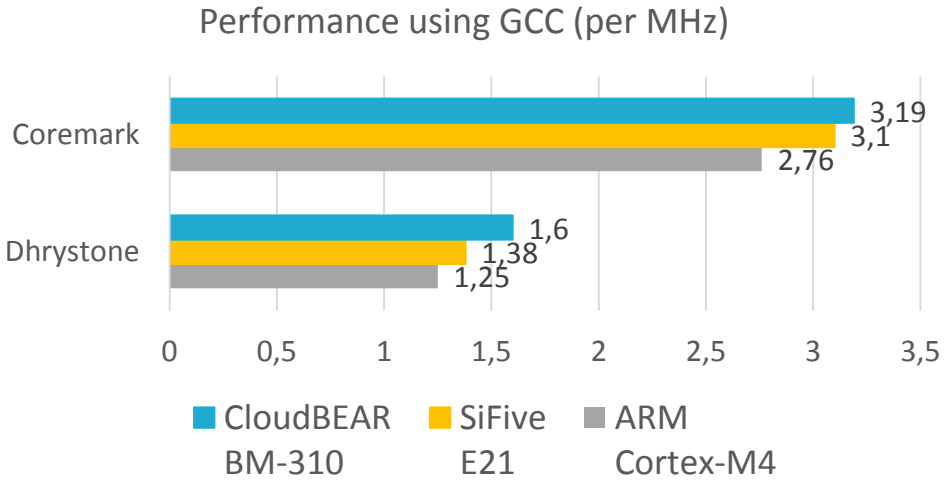


BM-310

Microcontroller core

- Small, Low power microcontroller
- RV32IMC
- Machine/User privilege levels
- 3-stage pipeline
- Configurable interrupt controller



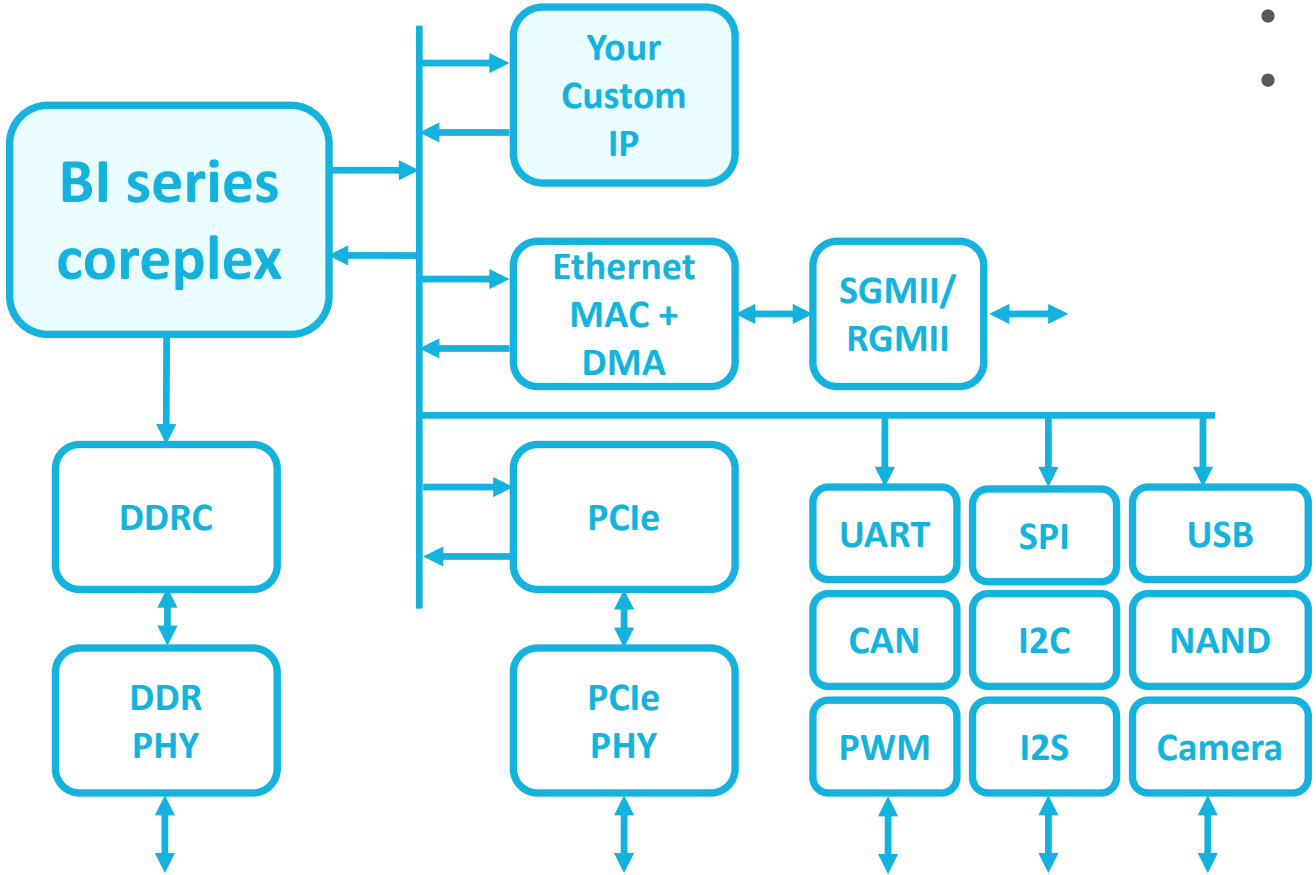


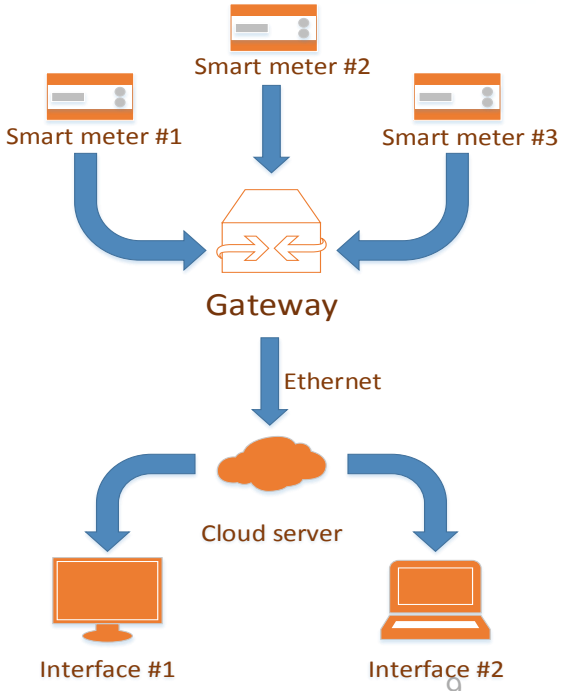
	TSMC 40LP, 9t
Frequency @ worst	200 MHz
Complex area (w/o TCM)	0.05 mm^2
Worst setup corner	SS, -40C, 0.81V

Application processor platform

- TSMC 28nm
- TSMC 40nm

Milandr





BI series

Linux capable application cores

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BI-350

RV32IMAC[F]

32-bit Tiny Linux capable core targeting IoT applications

BI-651

RV64GC

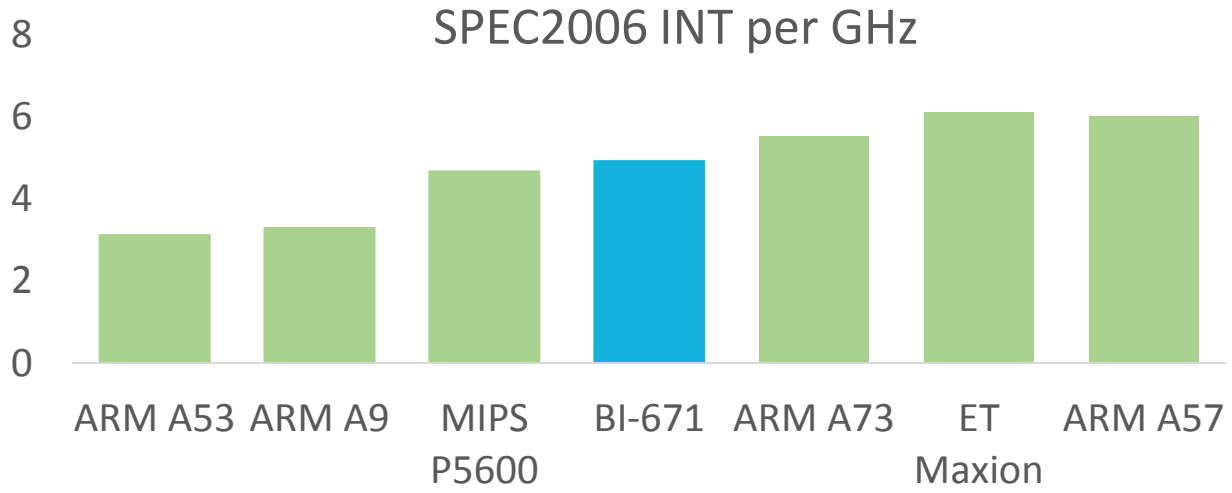
64-bit Linux capable core targeting high performance in power constrained environment

BI-671

RV64GC

64-bit Mid-range application core for maximum single thread performance

BI-671 at a glance

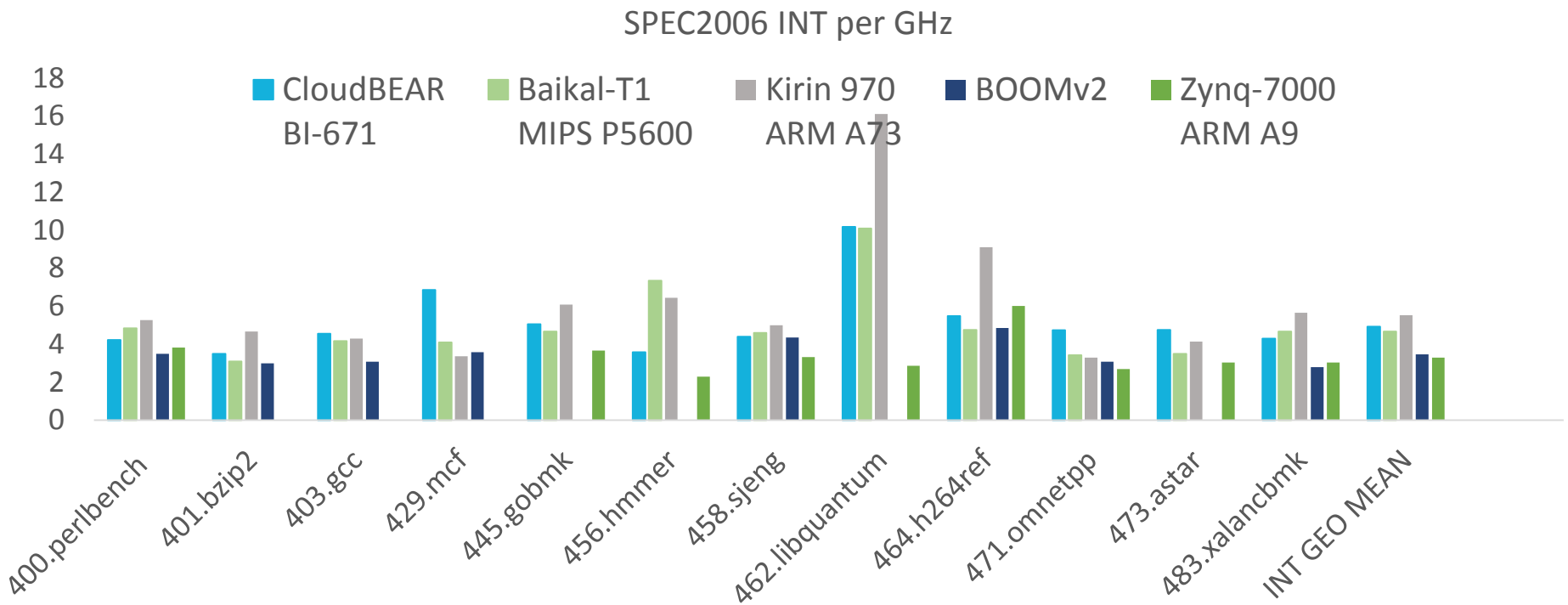


- >1.5x better performance than ARM Cortex-A9, ARM Cortex-A53
- On the same performance level with MIPS P5600
- 80-90% of ARM A73, ARM A57, ET Maxion performance

Benchmark	Score/MHz
Dhrystone	**3.58***
Coremark	**5.36**

* Dhrystone ground rules

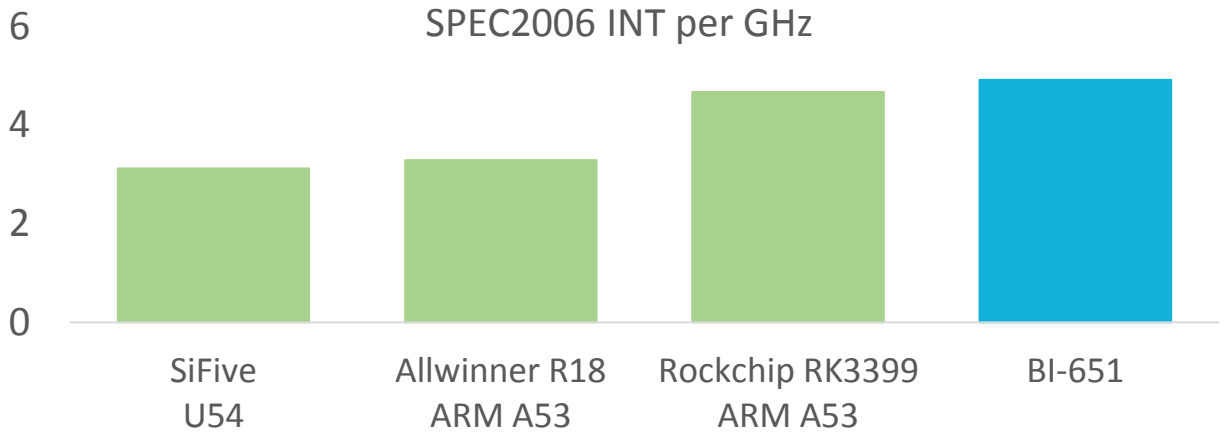
BI-671 SPEC2006 performance



BI-671 data is preliminary and collected on FPGA prototype

bzip2, gcc, mcf – missing data for Zynq-7000 since require 2GiB RAM
gobmk, hmmer, libquantum, astar – missing data for BOOMv2

BI-651 at a glance

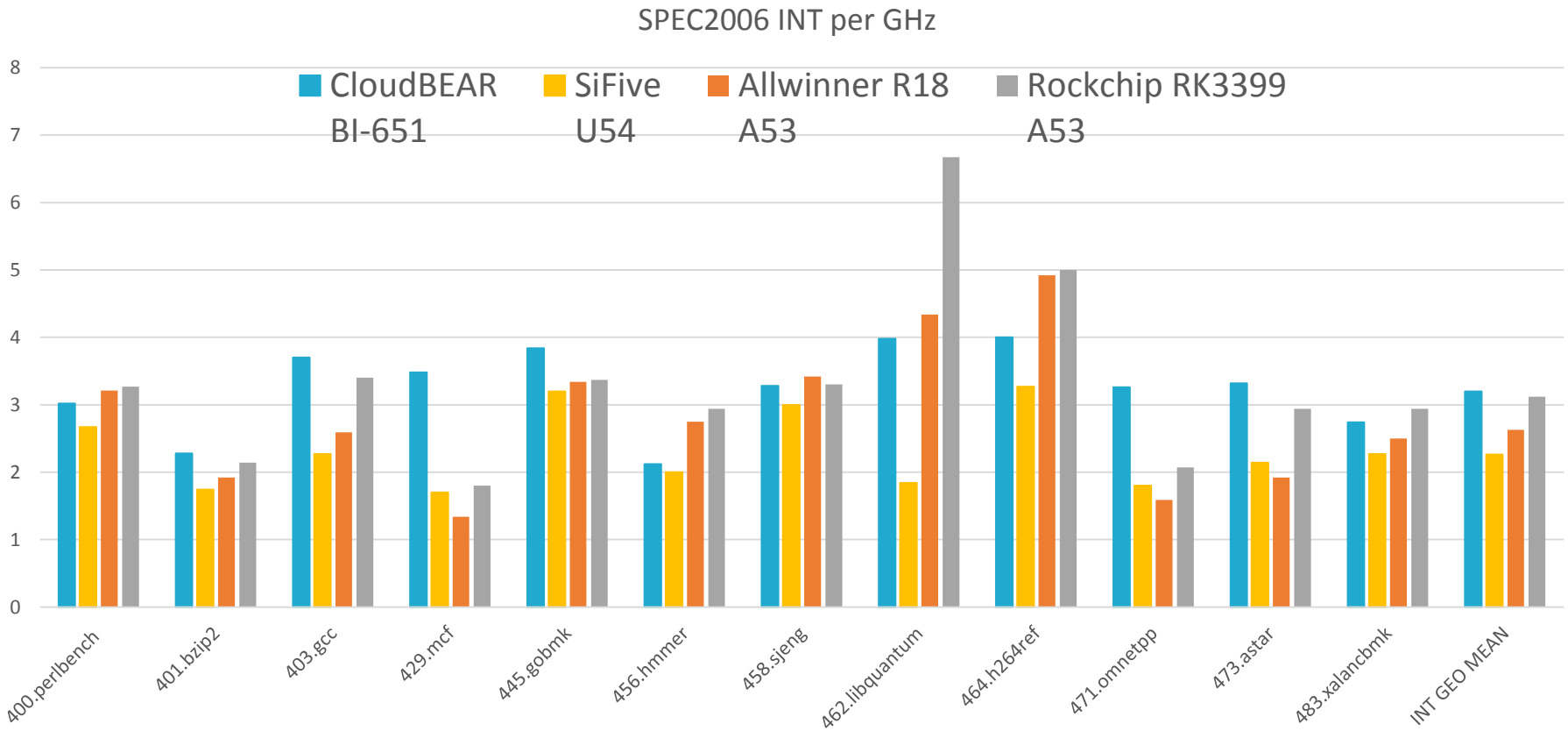


- >1.4x better performance than SiFive U54
- On the same performance level or better then ARM A53

Benchmark	Score/MHz
Dhrystone	**2.44***
Coremark	**4.15**

* Dhrystone ground rules

BI-651 SPEC2006 performance



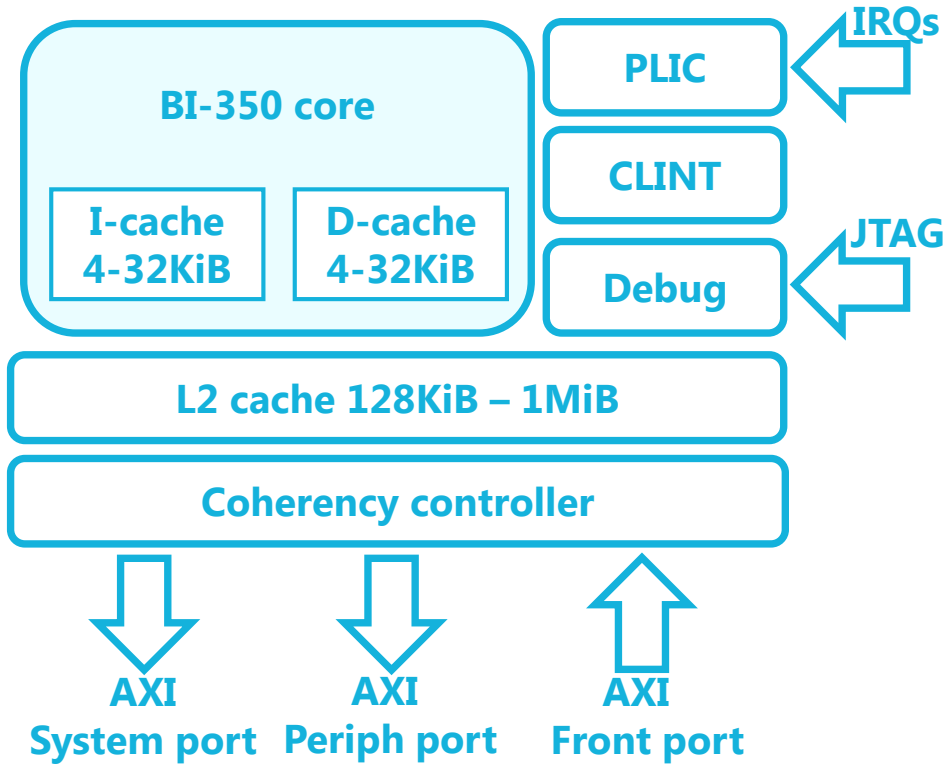
BI-651 data is preliminary and collected on FPGA prototype

BI-350 small Linux capable core

- Architecture: RV32IMAC[F]
- Single instruction issue
- Machine, Supervisor and User modes
- Configurable caches
  - Smaller size
  - Shorter cache line
  - Narrow memory interfaces
- L2 optional
- Tiny coherency controller configuration
- Configurable BTB, BHT, RAS

Benchmark	Score/MHz
Dhrystone	1.6*
Coremark	2.9

* Dhrystone ground rules



Motor control / Predictive maintenance platform

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BR series coreplex

Isolated security/crypto subsystem

- BM-310
- TRNG
- Key RAM
- Crypto Acc

- On-chip Flash 1 MiB
- 12-bit 3xADC 32 channels
- 12-bit 3xDAC
- Your Custom IP
- High Freq PWM
- UART, SPI, CAN, I2C
- Ethernet
- PMU 3xLDO + DC-DC
- Motor Control Acc
- USB 2.0 PHY
- Battery domain

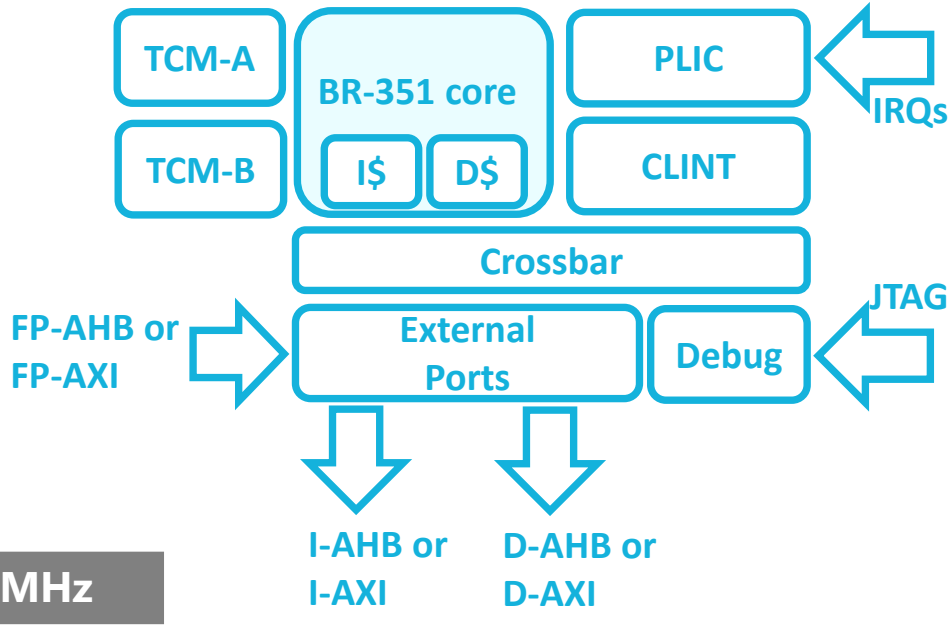
- TSMC 90nm LP

Milandr

BR-351

Embedded core

- RV32IMC
- Machine/User privilege levels
- 10-stage pipeline
- Dual-issue in-order
- TCMs and caches



Benchmark	Score/MHz
Dhrystone	**2.2***
Coremark	**4.15**

* Dhrystone ground rules

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