

The new reality and tremendous opportunity of open source processing

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1980s

Battle of unique, special-purpose and simple general-purpose chips. Rise of Intel x86 CISC chips for general purpose and slower adoption of RISC chips.

Drawbacks of patent license costs with high barriers to entry

1990s

The lifespan of CPU designs began to shrink from years to months, as performance demands accelerated. Moore's law often cited to double transistors every 12-18 months relative to cost.

In parallel, computing needs diverged across implementations, from servers to cars. ARM became strong for embedded.

2000s

Performance is critical as physical limits are in sight, age of accelerators and io innovation.

Mobile drives innovation.

World's first 2-billion transistor microprocessor Intel Itanium announced in 2008.

Grass roots of open cores such as OpenRISC and OpenSPARC.

Today

Exponential growth driven by diverse computing need (IoT, AI, 5G), solved by custom processor development.

Low barriers to entry with open processor IP (OpenPOWER, RISC-V, and MIPs).

RISC-V specification is free and open with extensions, tools, implementations, and software underway.

Evolution of the processor industry

Global trends driving processor growth



Cloud and data center applications top cloud providers like Amazon and Google are designing their own chips.



Mobile and wireless continue rapid evolution with each generation of hardware and increased capability.



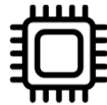
Automotive is transforming from autonomous vehicles to infotainment to safety, the whole vehicle relies on innovative electronics.



Consumer and IoT devices bring incredible innovation and volume with billions of connected devices being forecast in the next 5-10 years.

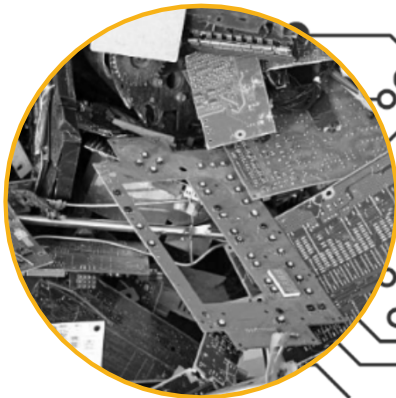


Industrial IoT incorporating artificial intelligence in manufacturing and industrial processes.

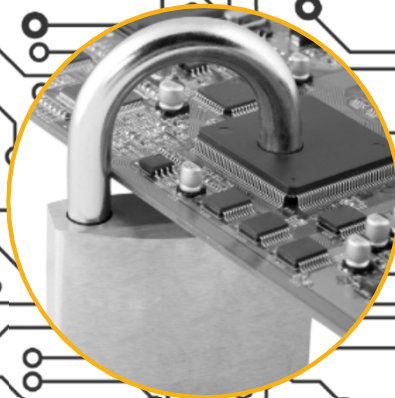


Memory was the largest semiconductor category by sales with \$158 billion in 2018, and the fastest-growing, with sales increasing 27.4%.

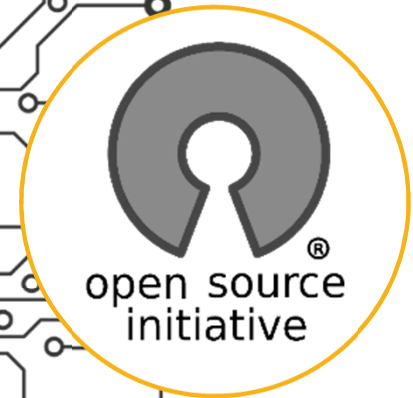
New workloads demand processor flexibility for innovation



Legacy ISAs Are
Decades Old



RISC-V Unlocks the
Architecture & Enables
Innovation



RISC-V is
Open Source,
transparent, and
royalty free

RISC-V Foundation



Welcome to the RISC-V revolution!

- **RISC-V** is the open-source hardware Instruction Set Architecture (ISA)
- Frozen base user spec released in 2014, contributed, ratified, and openly published by the RISC-V Foundation

The RISC-V Foundation is a non-profit entity serving members and the industry

Our mission is to accelerate RISC-V adoption with shared benefit to the entire community of stakeholders.

- ✓ Drive progression of **ratified specs, compliance suite, and other technical deliverables**
- ✓ **Grow the overall ecosystem / membership**, promoting diversity while preventing fragmentation
- ✓ Deepen **community engagement and visibility**

RISC-V Foundation



AWS Announces RISC-V Support in the FreeRTOS Kernel enabling embedded developers to create IoT applications on the officially supported FreeRTOS kernel for microcontrollers – AWS 26 February 2019

SERV CPU exemplifies the modularity of RISC-V to create an **extremely small CPU** running standard RISC-V software – Qamcom 15 Sep 2019

Alibaba announces roadmap of RISC-V SoC from Embedded to Cloud CPUs
– Alibaba. May 2019

SiFive Celebrates Historic 100 Design Wins Milestone
– SiFive 6 June 2019

GigaDevice launched world's first general-purpose microcontroller based on RISC-V for the IOT market
– EE Times 26 Aug 2019

The EU Is Progressing With The Processor For A European Supercomputer
RISC-V was chosen as the basis for the supercomputer, and the processor and platform developed with the European Processor Initiative (EPI) consortium. – TechNews. 5 June 2019

Western Digital releases their RISC-V Cores to the world... they will transition their consumption of silicon over to RISC-V, putting **one Billion RISC-V cores per year** into the marketplace – Hackaday. 13 February 2019

Right here.
Right now.

Mainstream
innovation
on RISC-V.

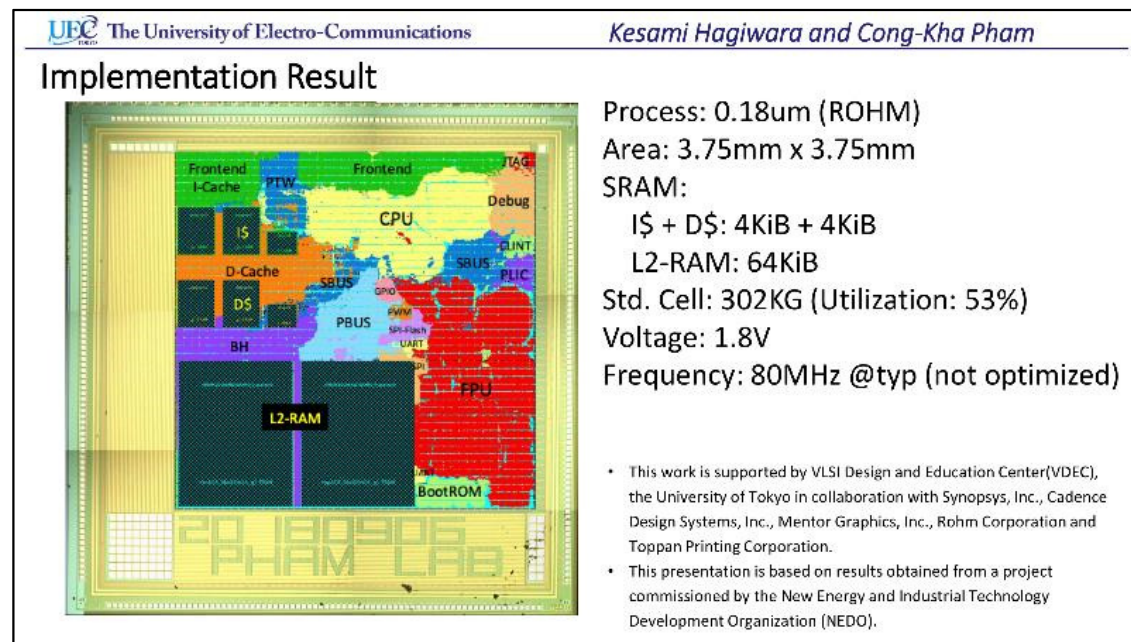
GreenWaves Technologies Named 2019 Cool Vendor in AI Semiconductors
– Gartner 29 April 2019

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... greatly
changed from the
MIPS architecture.

RISC-V has been
rewritten as a
base processor,
and **a new
chapter called
“Domain-Specific
Architectures” has
been created.**
- Translators

UEC Pham Lab. 64-bit Rocket U5 Experimental Chip January 2019



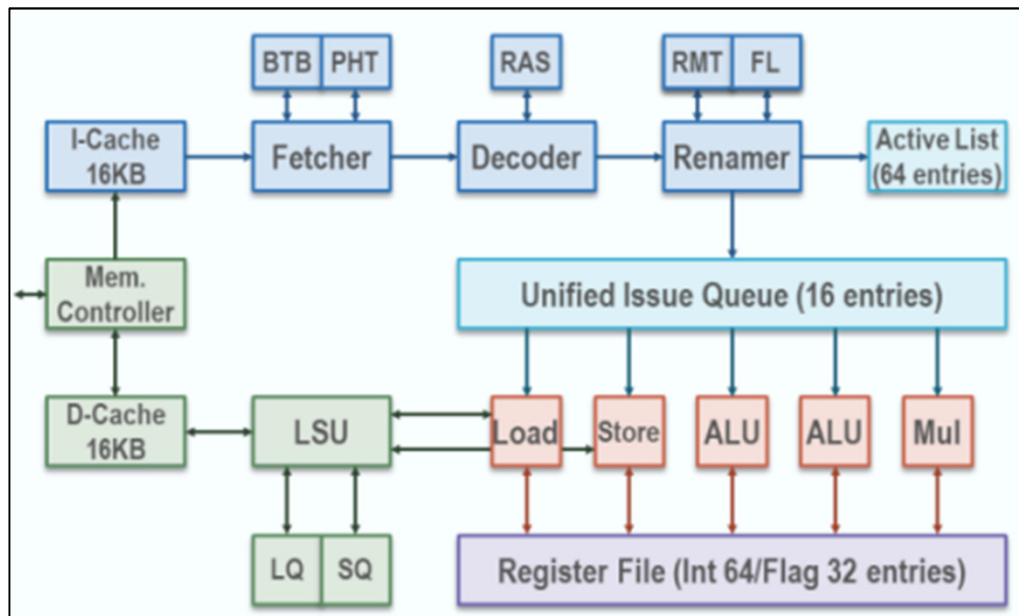
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University of Tokyo Shioya Lab.

Development of RISC-V compatible advanced CPU "RSD"



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RISC-V Instruction Set Architecture is gaining momentum, similar to Linux vs. closed OS.

University of Tokyo is conducting **research and development on Advanced RISC-V compatible CPU "RSD."**



Ubiquitous AI Corporation. TOPPERS-Pro/ASP RTOS for RISC-V June 2019

通常タスク	タスク起動・終了	タスク付属同期	タスク例外	セマフォ
イベントフラグ	データキュー	メールボックス	周期ハンドラ	固定長メモリアル
システム時刻	割込みハンドラ	CPU 例外ハンドラ	割込み サービスルーチン	アラームハンドラ
優先度データキュー	割込みラインマスク	割込み優先度マスク	(注) ミューテックス	メッセージバッファ
オーバーラン ハンドラ	動的生成	制約タスク		

■ : Extension 適用時の機能。

注 ミューテックス：優先度上限プロトコルのみサポートし、優先度継承プロトコルは未サポート。

Realtime Operating System conforms to μ ITRON4.0 Specification Standard
with available **Ubiquitous AI Corporation extensions**

Full support provided by Ubiquitous AI Corporation

- ✓ Middleware and tools support
- ✓ Maintenance service and technical support program available
- ✓ Additional services such as porting, customization and driver development



RISC-V is used as a vehicle to develop **secure open source, open architecture, and open silicon.**

New Energy
and Industrial
Technology
Development
Organization

NEDO. Secure Open Architecture Base Technology and AI Edge Application Research and Development 2018 Grant

Conclusions

Keio University



- We are developing an open RISC-V security system platform.
- Secure MCU complements RISC-V TEE development ongoing in TEE working group.
- Address supply chain lifecycle of an Iot / AI Edge device.
- We make disclosures from time to time.
- welcome collaboration and peer reviews.

This work is in part supported by New Energy and Industrial Technology Development Organization (NEDO) Grant P16007. The work leverages VDEC program and facilities.



HITACHI

2019/3/13

SECOM

AIST

NATIONAL INSTITUTE OF
ADVANCED INDUSTRIAL SCIENCE
AND TECHNOLOGY (AIST)



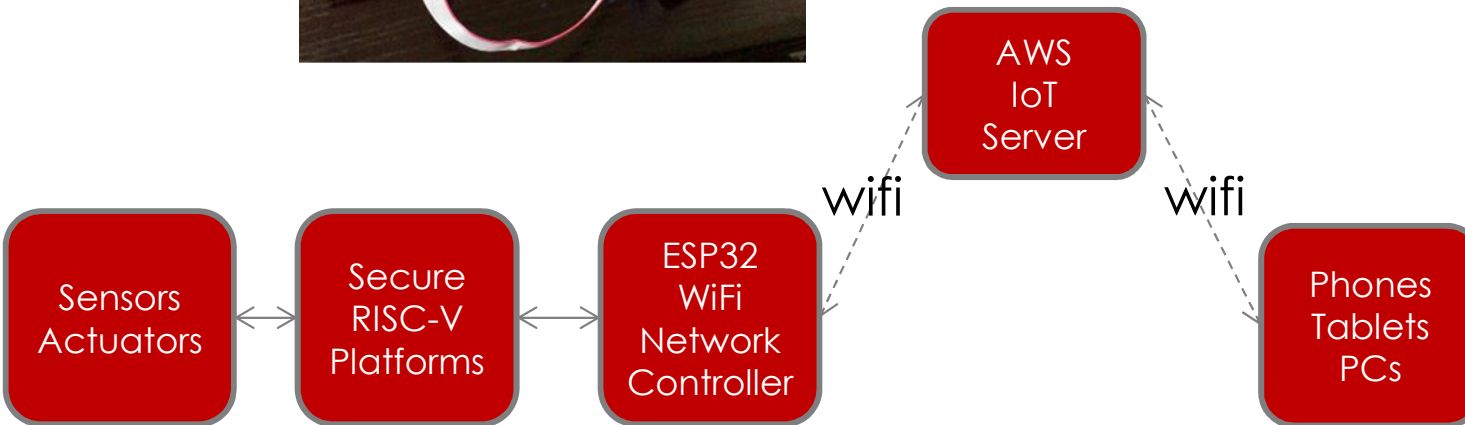
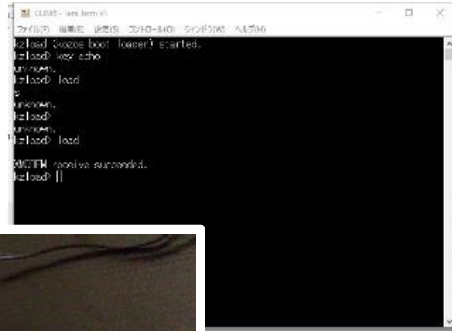
METI

Ministry of Economy, Trade and Industry

15

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SHC. RISC-V IoT Solutions

Amazon Web Services IoT Solution for RISC-V

RISC-V Distributions and Services growing in Japan

- ✓ SiFive Japan K.K. – DTS Insights SiFive IPs and Services
- ✓ Rambus Japan K.K. – Cybertrust CryptoManager
- ✓ Seeed K.K. – M1 AI Module, RISC-V 64 AI Module
- ✓ SWITCH SCIENCE K.K. – AI camera with RISC-V CPU, M5StickV



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SEMICONDUCTOR IP



FOUNDRY SERVICES

DEVELOPMENT TOOLS



SW AND CLOUD

RISC-V Foundation

CONSULTING/RESEARCH



MACHINE LEARNING/AI



COMMERCIAL CHIP VENDORS

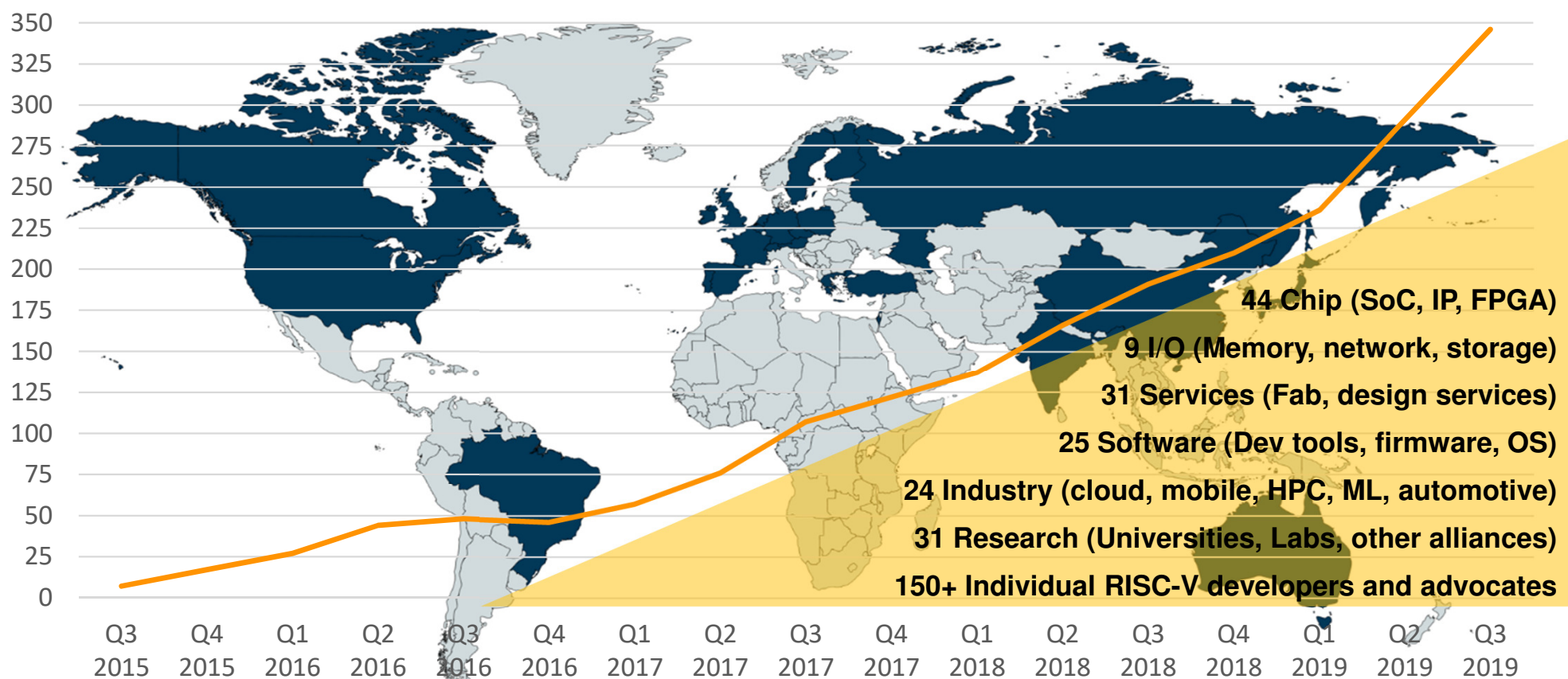
FPGA

BROAD MARKET

APPLICATION PROCESSORS, GRAPHICS

NETWORKING

More than 350 RISC-V Members in 28 Countries Around the World





RISC-V Foundation

RISC-V
Foundation
Members
from Japan
driving global
impact



RISC-V is
visibly
disrupting
the industry

1,183 attendees at 2018 RISC-V
Summit

2,262 press articles

8,589 LinkedIn Followers

9,835 @RISC_V Twitter Followers

34,200+ articles mentioning RISC-V
Foundation, member companies and
ISA since January 2016



RISC-V Foundation



RISC-V Foundation multiplies the investment members are making in RISC-V

Technical
Deliverables

Compliance +
Certification

Visibility

Learning + Talent

Advocacy +
Outreach

Marketplace

RISC-V Foundation



Engage!

Drive technical priorities in 20 focus areas

Technical Deliverables
Compliance

Opcode Space Mgmt Standing Committee

Software Standing Committee

Base ISA Ratification Task Group

Privileged ISA Spec Task Group

UNIX-Class Platform Spec Task Group

Formal Specification Task Group

Trusted Execution Env Spec Task Group

B Extension (Bit Manipulation) Task Group

J Extension (Dynam. Translated Lang) Task Group

P Extension (Packed-SIMD Inst) Task Group

V Extension (Vector Ops) Task Group

Cryptographic Extension Task Group

Debug Specification Task Group

Fast Interrupts Spec Task Group

Memory Model Spec Task Group

Processor Trace Spec Task Group

Sv128 Specification Task Group

Compliance Task Group

+ Security Committee and
proposed Safety Task Group

Japan RISC-V community 2019



RISC-V in Trade Shows

- ✓ Design Solution Forum 2019 Open Source Silicon Slot on 10/03
- ✓ ET 2019 Open Source Silicon Pavilion on 11/20-22

RISC-V Meetups

- ✓ Embedded Technologies Summer Workshop in Gifu Gero Hotspring 9/6
- ✓ Kumiko Meetups planned in Tokyo 10/23 and Osaka 10/25.

Japan RISC-V curriculum and learning

RISC-V Books in Japanese Language

- ✓ RISC-V READER, and Computer Architecture: Quantitative Approach translated to Japanese
- ✓ Local Electronics Magazines RISC-V Specials
 - November 2019 Released 10/10/2019 of Transistor Technology
 - FPGA Magazine Released 10/24/2018
 - Interface Magazine: Research on Open Source CPU RISC-V serial articles published 13 times 02/19/2019

RISC-V in University Research is rampant in Japan

- ✓ A proposal of scalable vector instruction set for RISC-V for embedded system 7/24/2019



Nikkei Business Publication RISC-V Reader Translation

I jumped on the Japanese translation of the RISC-V manual...nice to be able to read this book, as a quick explanation of the RISC-V design philosophy and basic specifications. This book may be unsatisfactory for those who try to implement a RISC-V

- Amazoness (an Amazon Customer Reviewer)

- Amazon Best Seller in Tech Category
October 2018
- 50 copies purchased by National Institute
of Technology College Libraries



SiB Publication.

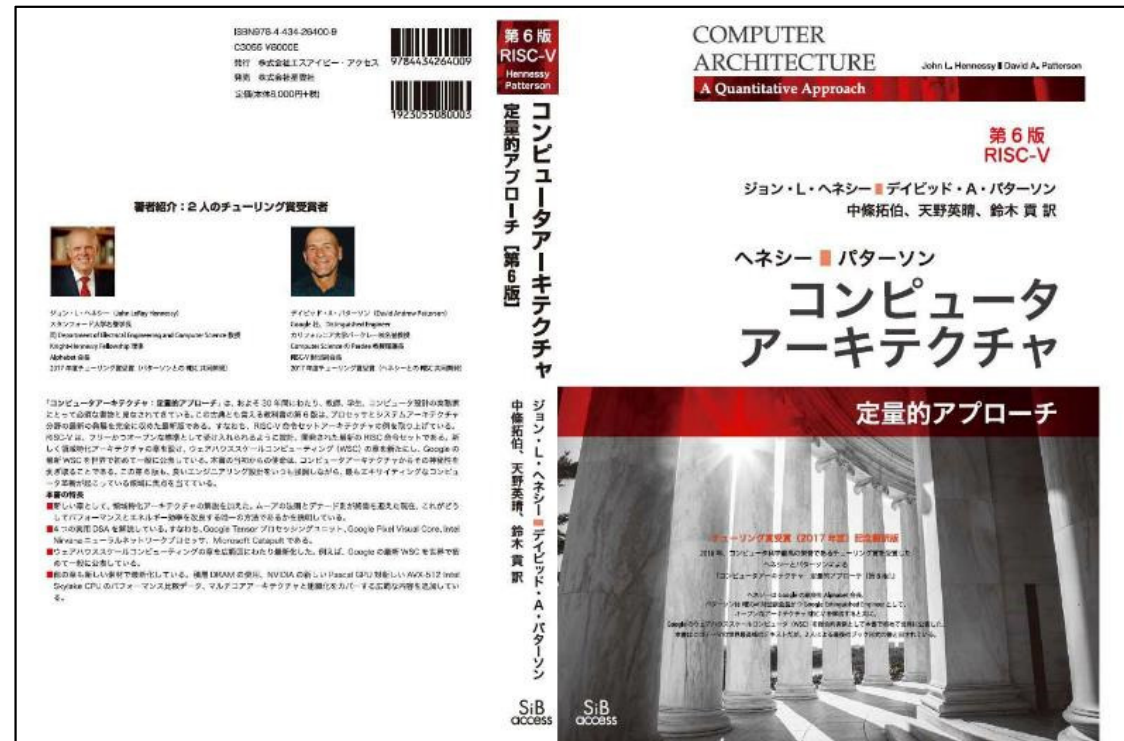
Computer Architecture: A Quantitative Approach



RISC-V Japanese Translation Edition
09/30/2019

All 5 copies are always checked out
of University of Tokyo library

... greatly changed from what was
previously based on the MIPS
architecture ... RISC-V has been
rewritten as a base processor, and a
new chapter "Domain-Specific
Architectures" has been created.
- Translators



RISC-V Foundation



Come together. Right Now.

Meetups (2,000+ Members)

Advocacy + Outreach

Austin Area RISC-V Group

<https://www.meetup.com/Austin-Area-RISC-V-Group/>

Bay Area RISC-V Group

<https://www.meetup.com/Bay-Area-RISC-V-Meetup/>

Bristol RISC-V Meetup Group

<https://www.meetup.com/Bristol-RISC-V-Meetup-Group/>

Cambridge RISC-V Meetup Group

<https://www.meetup.com/Cambridge-RISC-V-Meetup-Group/>

Israel RISC-V Meetups

<https://www.meetup.com/Israel-RISC-V-meetups/>

London RISC-V Meetup

<https://www.meetup.com/London-RISC-V-Meetup/>

Pune RISC-V Group

<https://www.meetup.com/Pune-RISC-V-Group/>

Rocky Mountain Area RISC-V Group

<https://www.meetup.com/Rocky-Mountain-Area-RISC-V-Group/>

San Diego RISC-V Meetup Group

<https://www.meetup.com/San-Diego-RISC-V-Group/>

Shanghai RISC-V Meetup

<https://www.meetup.com/shanghai-riscv/>

Vienna RISC-V Meetup

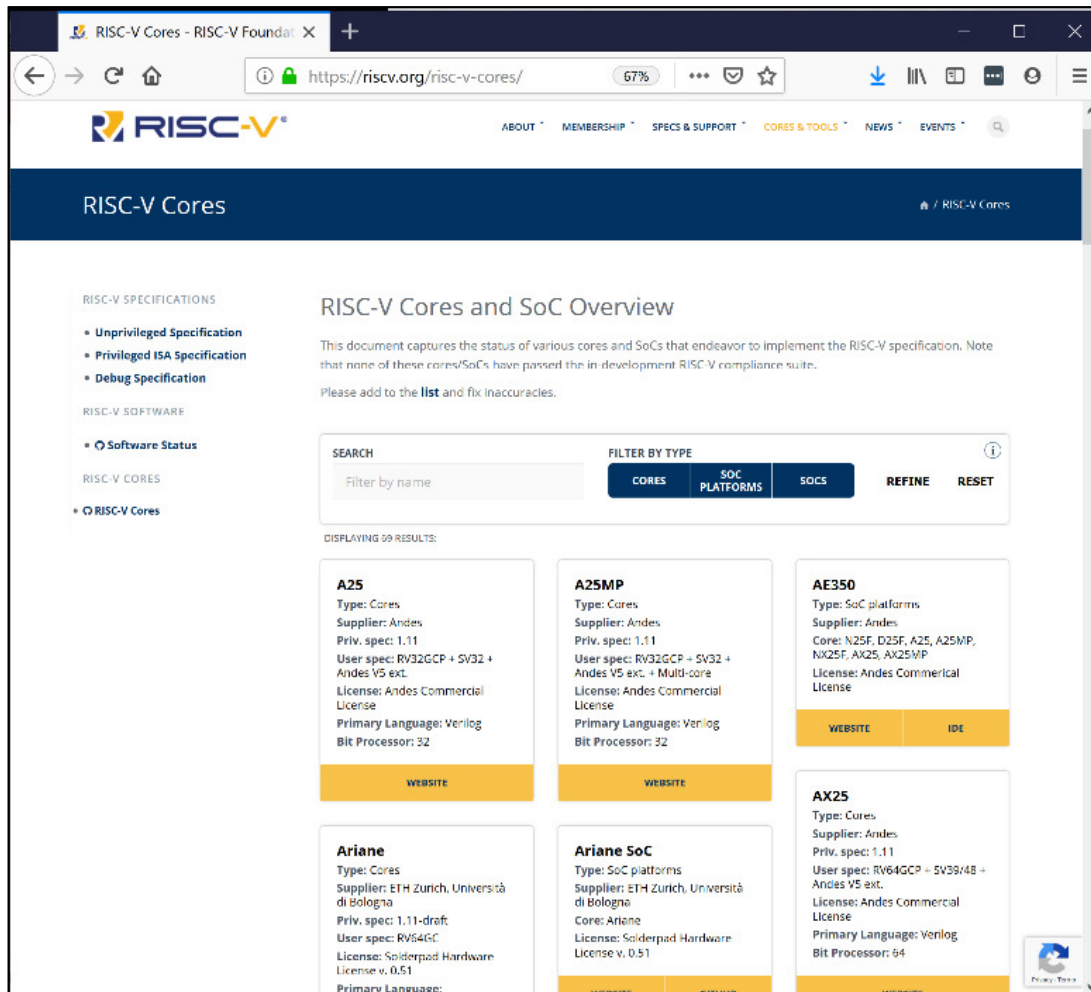
<https://www.meetup.com/Vienna-RISC-V-Meetup/>

RISC-V Japan Association

<https://riscv-association.jp>

RISC-V Foundation





Marketplace

Improving
online
marketplace
of RISC-V
offerings

RISC-V Foundation





RISC-V
Foundation
multiplies the
investment
members are
making in RISC-V

Value Proposition for Members

- Ability to drive standards and set direction on future specifications
- Exposure to a large client base, across global markets
- Strong, growing ecosystem for collaboration
- Invested programs across technical areas and more to accelerate your strategy
- Several RISC-V Foundation groups for support (technical, marketing, educational, etc.)
- Use of the RISC-V trademarks and logos

RISC-V Foundation

RISC-V is already disrupting the silicon industry



@risc_v
@riscvjp
@Calista_Redmond



risc-v-foundation



riscv.org
riscv-association.jp

Join the Revolution

References

<https://aws.amazon.com/about-aws/whats-new/2019/02/aws-announces-riscv-support-freertos-kernel/>

<https://technews.bg/article-116996.html>

<https://riscv.org/2019/05/getting-started-with-risc-v-china-roadshow-proceedings/alibaba-pushing-data-from-edge-to-cloud-with-risc-v-ecosystem/>

<https://hackaday.com/2019/02/13/western-digital-releases-their-risc-v-cores-to-the-world/>

<https://www.sifive.com/press/sifive-celebrates-historic-100-design-win-milestone>

Three RISC-V Foundation membership options



Premier Member Benefits

- Community level benefits plus...
- Board seat and Technical Steering Committee seat included for \$250k level
- Technical Steering Committee seat included for \$100k level
- Summit speaker session
- Solution provider listing
- 2 case study / blogs per year
- 4 social media spotlights
- Spotlight member profile
- Inclusion in event promotions

Strategic Member Benefits

- Community level benefits plus...
- 3 Board reps elected for tier, includes strategic members that do not otherwise have a board seat.
- Eligible to lead workgroup and/or committee
- Solution provider listing
- 1 social media spotlight

Community Member Benefits

- Accelerated development through open source, ratified ISA
- Reduced investment and development risk for adopting architecture
- Eligible to participate in workgroups, influence strategy and adoption
- Forum for dialogue and learning
- 1 voting Academic Board rep, 1 non-voting Community Board rep
- Member logo / name listing in website
- Event registration discount

Premier Requirements

- Membership open to any type of legal entity, not open to individual members
- \$250k Annual membership fee that includes Board seat and TSC seat
- \$100k Annual membership fee that includes TSC seat

Strategic Member Requirements

- Membership open to any type of legal entity, not open to individual members
- Annual membership fee based on employee size
 - 5,000+ employees \$35k
 - 500-5,000 employees \$15k
 - <500 employees \$5k

Community Requirements

- Membership open to academic institutions, non-profits, and individuals not representing a legal entity
- No annual membership fee

Note: An organization may not hold more than one seat on the Board or TSC

Chip
outlook
growing to
US\$490
billion in
2019

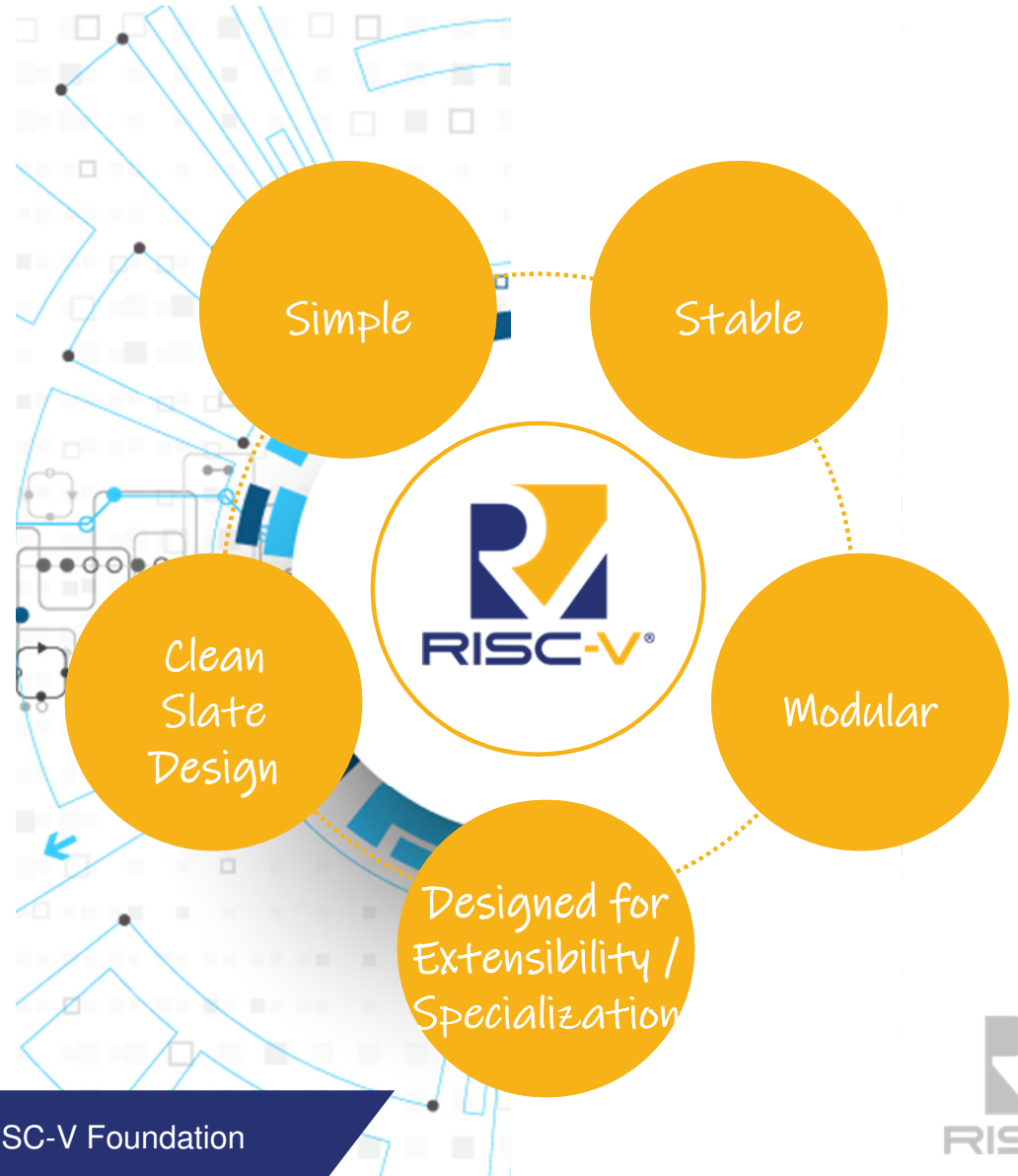
In addition to baseline growth, major technology shifts on the horizon include 5G, autonomous vehicles, AR/VR, and AI.

What is 5G all about?

5G expands the mobile ecosystem to connect IoT devices to the Internet with low latency and provide massive network capacity, for faster transfer data between IoT and the cloud. Consistent high speed data, even when users are moving, makes AI-enabled applications like autonomous cars a reality.



RISC-V ushers in new era of silicon design



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