

INTRODUCING THE ESP32-C3 Espressifs first RISC-V chip

About me

- Jeroen Domburg
- Senior Software / Technical Marketing Manager
- HW me SW

About Espressif

- Fabless chip company
- IoT silicon
- HQ in Shanghai
- Offices in China, India, Czech, Singapore

History of Espressif

- ESP8266
- ESP32
- ESP32S2



- 80/160MHz Xtensa
- WiFi
- 190'ish K of RAM
- External flash
- UART, SPI, GPIO, I2S, ADC
- 'WiFi coprocessor' / simple apps



- 80/160/240MHz Xtensa X 2
- WiFi, BT, BTle
- 520K of RAM
- External flash
- UART, SPI, GPIO, ADC, PCNT, MCPWM, LEDPWM, I2C, I2S, RMT, LCD, camera, timers...

- 80/160/240MHz Xtensa X 1
- WiFi
- 320K of RAM
- External flash
- USB, UART, SPI, GPIO, ADC, PCNT, MCPWM, LEDPWM, I2C, I2S, RMT, LCD, camera, timers...
- RISCV ULP

Software

- ESP32 and up: ESP-IDF
- FreeRTOS, LWiP, Cmake (+ many libs)
- Others in the works: Zephyr, NuttX

Software: We're Open!

- SDK: Fully open-source (Apache 2.0)
- TRM documents the hardware
- Exception: lower layers WiFi/BT

CPUs used

- ESP8266: Xtensa LX106
- ESP32: Xtensa LX7 Dual-core (SMP)
- ESP32S2: Xtensa LX7 Single-core

Xtensa CPU?

- Tensilica, now Cadence
- 32-bit RISC
- Some 'weirdness': windowed register file
- Extendable: custom CPU instructions
- Support tools from Cadence

Xtensa: Great!

- CPU optimization: custom instructions by profiling
- IP well-used and low on bugs
- Support tools from Cadence
- Digital team understands Xtensa

Xtensa: Not so great...

- We need general purpose computing
- ISA closed
- Documentation needs NDA
- Cadence tools closed source

New chip!

- WiFi, BTLE
- Cheap & cheerful
- Single-core
- Some GPIO, some RAM...
- RISC-V?

Core

- In-order 4-stage
- RISC-V 32bit IMC
- 160MHz
- We have RTL

Fix it!

- Take existing design, tweak peripherals
- Take out Xtensa
- Put in RISC-V
- ...
- Profit!



Thanks for listening!

Questions?

Issues



Issues



Interrupt controller

- Adapter to interrupt source mux
- Priorities, level/edge, ...
- Not PLIC/CLIC compatible

Debug subsystem

- New design
- Access HARTS & system bus
- RiscV debug spec compatible

The rest of the SoC





Software

- ESP-IDF
- Arduino
- NuttX
- ...?

Tools

- GCC
- LLVM
- TinyCCOpenOCD



Advantages of the RISC-V core



Source: Hackaday

Advantages of the RISC-V core



Source: Hackaday

Future plans

- More compliancy
- Faster core
- Instruction extensions
- Multicore

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	€ <u>Enlarge</u>	Mfr. Part # ESP32-C3 Mouser Part # 356-ESP32-C3	Espressif Systems	WiFi Modules (802,11) SMD IC ESP32-C3, single- core MCU, 2.4G Wi-Fi & BLE 5.0 combo, QFN 32- pin, 5*5 mm		Non-Stocked Lead-Time 6 Weeks	Cut Tape 1:¥118 Reel 5,000:¥118	Min.: 1 Mult.: 1 Reel: 5,000	RoHS Detai
	QEnlarge	Mfr. Part # ESP32-C3-DevKitM-1 Mouser Part # 356-ESP32-C3DEVKITM1	Espressif Systems	WiFi Development Tools (802.11) ESP32-C3 general-purpose development board, embeds ESP32-C3-MINI-1, 4 MB flash, with pin header Learn More	Datasheet	730 On Order View Dates	1:¥944	Min.: 1 Mult.: 1	Deta
		Mfr. Part # ESP32-C3-DevKitC-02 Mouser Part # 356-ESP32C3DEVKITC02	Espressif Systems	Development Boards & Kits - Wireless ESP32-C3 general-purpose development board, embeds ESP32-C3- WROOM-02-N4, 4 MB flash, with pin header	Datasheet	340 On Order View Dates	1:¥1,062	Min.: 1 Mult.: 1	RoHS Detai



Thanks for listening!

Questions?

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Thanks!