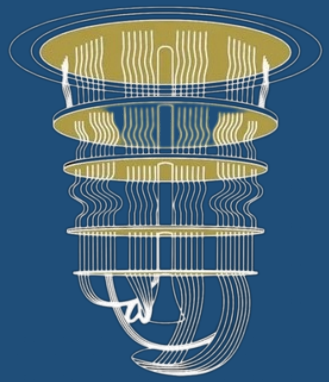
Keio University

SQAI
Center of Innovation for Sustainable Quantum AI

An FPGA-based Implementation of Quantum Computer Simulator Qulacs



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RISC-V

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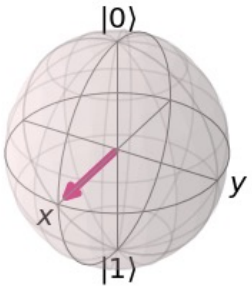
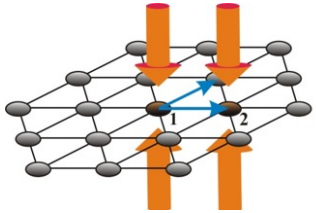
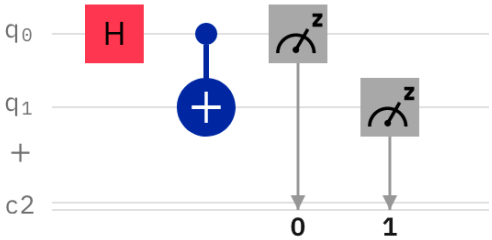
1. Quantum Simulator using State Vector



Bloch sphere



Entanglement



IBM quantum Composer

- For a qubit (quantum bit) state: a coherent superposition of the basis states
  - **Linear combination** of $|0\rangle$ and $|1\rangle$: $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$
    - $|0\rangle = (0, 1)$ $|1\rangle = (1, 0)$ $|\alpha|^2 + |\beta|^2 = 1$
    - $|\alpha|^2$ vs. $|\beta|^2$ → The probability for $|0\rangle$ and $|1\rangle$

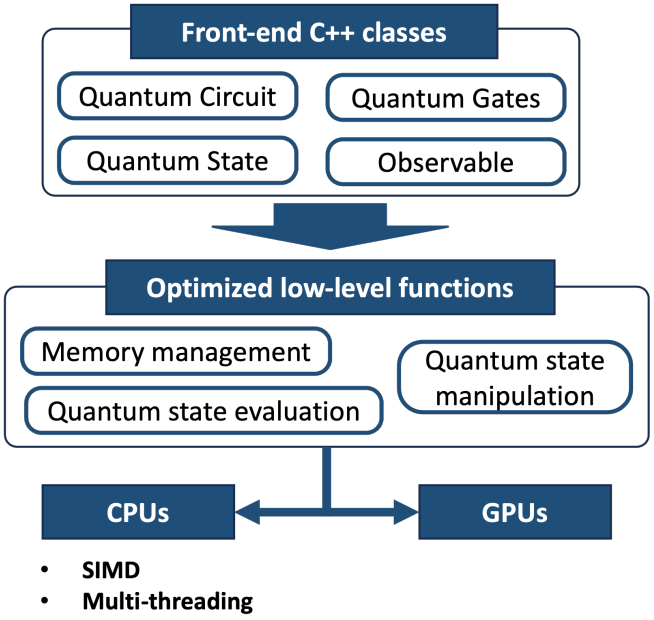
$$|\psi\rangle = \alpha \begin{bmatrix} 1 \\ 0 \end{bmatrix} + \beta \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$

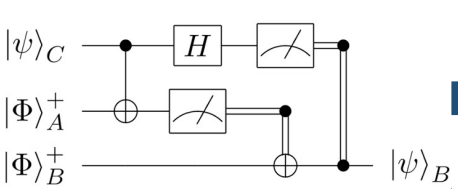
- For n qubit
  - $|\psi\rangle = a_{0\ldots00}|0\ldots00\rangle + a_{0\ldots01}|0\ldots01\rangle + \ldots + a_{1\ldots11}|1\ldots11\rangle$
  - 2^n states: Complex vectors representation
  - n qubits VS. Double precision Complex (128 bits) → Memory capacity: 2^{n+4} Bytes

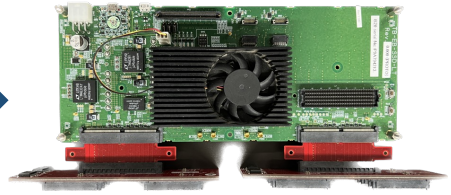
$$|\psi\rangle = a_{0\ldots00} \begin{bmatrix} 1 \\ 0 \\ \vdots \\ 0 \end{bmatrix} + a_{0\ldots01} \begin{bmatrix} 0 \\ 1 \\ \vdots \\ 0 \end{bmatrix} + \cdots + a_{1\ldots11} \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 1 \end{bmatrix}$$

2. Quantum Simulator Qulacs VS. FPGA Implementation

Qulacs [1]: A fast simulator for quantum circuit







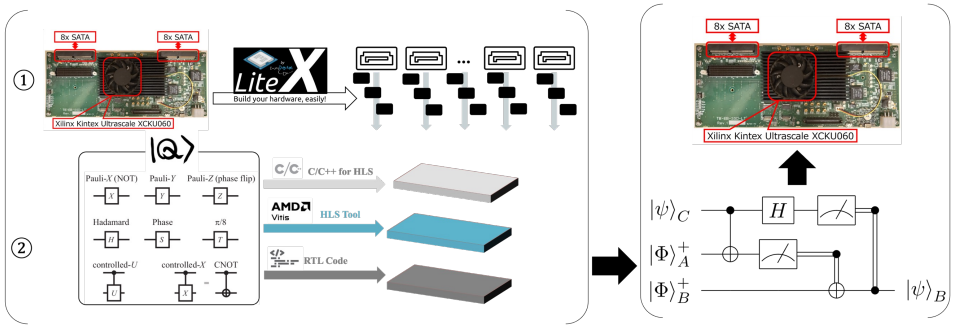
Pros & Cons of platform selection

CPUs:	Lack of locality of reference
	Virtual memory → memory requirements
GPUs:	Less requirements on computational capacity
	Costly utilization → Supercomputers / clusters
	High-speed data access using HBM2
	High-parallelism data processing
FPGAs:	Limited memory capacity → No virtual memory
	Limited performance inferior to GPUs
	Better performance in cost & energy consumption
	No additional overheads for data (de)compression

[1] Suzuki, Y. et al. (2021) 'Qulacs: a fast and versatile quantum circuit simulator for research purpose', Quantum, 5, p. 559. doi:10.22331/q-2021-10-06-559.

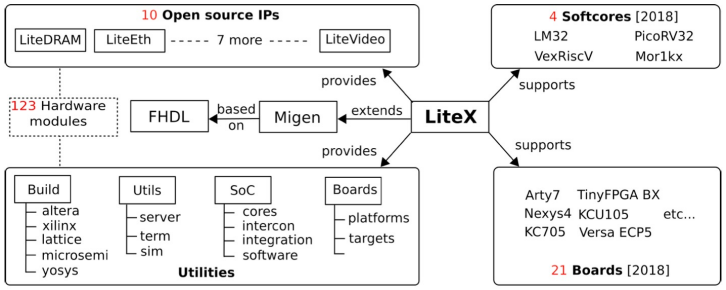
3. Qulacs Implementation on FPGA

- **2-stage Implementation**



- FPGA Trefoil Design: FPGA with **extensible memory capacities**
  - Response to enormous memory resource requirements
  - Multiple SATA-ports connection (Possible for 32 SATAs)
  - Pipelined data transfer (Higher throughput with less latency)

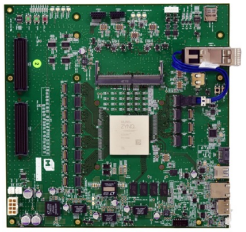
- LiteX [2] Design

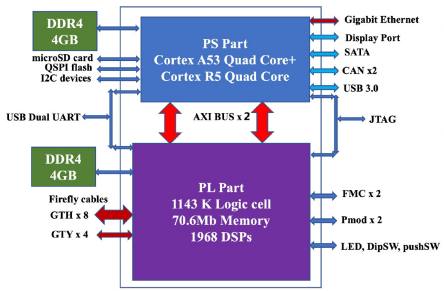


- HLS Design for Quantum Gates

Quantum Gates1	Meaning	Matrix
H (Hadamard)	Convert the qubit from clustering state to uniform superposed state	$\frac{1}{\sqrt{2}}\begin{bmatrix}1 & 1\\ 1 & -1\end{bmatrix}$
S	Rotates qubits 90 around the Z axis, counterclock	$\begin{bmatrix}1 & 0\\ 0 & e^{-\frac{\pi}{2}}\end{bmatrix}$
CNOT (Controlled Not)	Entangle & disentangle Bell states	$\begin{bmatrix}1&0&0&0\\0&1&0&0\\0&0&0&1\\0&0&1&1\end{bmatrix}$
Matrix	Arbitrary 2 quantum gates multiplication	

- FPGA platform





[2] Kermarrec, Florent, et al. "LiteX: an open-source SoC builder and library based on Migen Python DSL." *arXiv preprint arXiv:2005.02506* (2020).

4. Qulacs Optimization using HLS

- **Hadamard Gate Design**

n-qubit quantum circuit with 2^n states saved in vector state[ ]

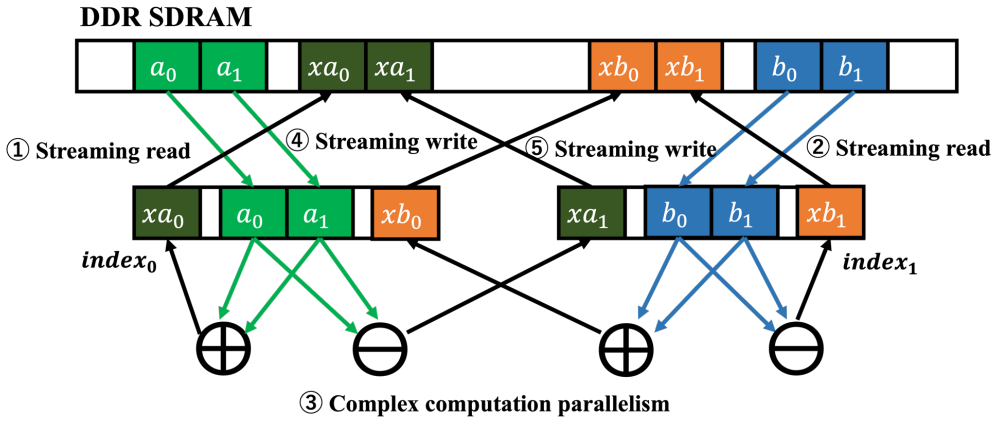
Target qubit: t

- $index_0 = b_{n-1}b_{n-2}\dots 0_t b_{t-1}b_{t-2}\dots b_0$
- $index_1 = b_{n-1}b_{n-2}\dots 1_t b_{t-1}b_{t-2}\dots b_0$

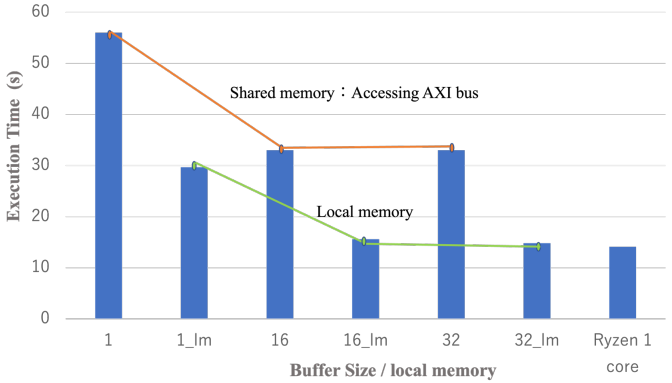
$x_0 = state[index_0]$ $y_0 = state[index_1]$ $x_1 = state[index_0 + 1]$ $y_1 = state[index_1 + 1]$

$$state[index_0] = \frac{1}{\sqrt{2}}(x_0 + x_1) \qquad state[index_1] = \frac{1}{\sqrt{2}}(y_0 + y_1)$$

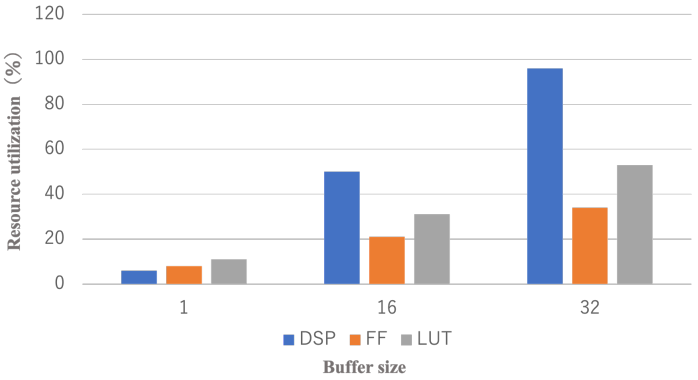
$$state[index_0 + 1] = \frac{1}{\sqrt{2}}(x_0 - x_1) \qquad state[index_1 + 1] = \frac{1}{\sqrt{2}}(y_0 - y_1)$$



- **Execution Time for H Gate (28 qubits)**



- **Resource utilization for H Gate (28 qubits)**



Extensible in qubit size with multiple FPGA cluster

Welcome to Poster Session for more details

Thank you for listening