SiFive

Leadership in the New Computing Era

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Founded by the Inventors of RISC-V

- SiFive is the RISC-V founder & brand standard
- Leading the commercialization effort since 2010
- World's largest technology Co's work with SiFive to adopt RISC-V
- Largest team & investment

Continued Investment Across Diverse Portfolio

SiFive

	Established Products in Silicon	New & Recently Announced	What's Next?
Performance 64-bit Application Processors	*Infrastructure*: P670, P650 *Consumer*: P550, P470, P450	P870-D	More performance, improved compute density Next generation consumer cores with RVA23 New features & improved PPA enabling more design points
Intelligence Scalable AI Compute	X280, X288	XMxx, X390, X380	Expansion of portfolio to cover more design points
Essential 32/64-bit Processors	E7, E6, E2 S7, S6, S2 U7, U6	Gen 4 release	Gen5 (& beyond) Expanded product space
Automotive ASIL B/D, cybersecurity	E6-A, S7-A	P870-A	Refreshed & expanded Automotive Essential products Automotive grade performance and intelligence processors

PLUS… System IP (IOMMU, WorldGuard security, RAS, AIA…) & software…. with ongoing investment

400+

design wins

Billions

Chips based on SiFive RISC-V cores, >10 billion cores

The Gold Standard

Majority of top Semi manufacturers
Major U.S. hyperscalers
Leading electric, and autonomous vehicles

Every “Magnificent 7” company has a RISC-V program

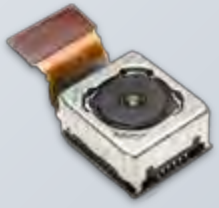
SiFive is supplying 5 of them

SiFive Products Are in the Field

A wide range of control, real-time and application processor applications

Embedded Controller for mobile SoC

Camera Sensor



Optical Image Stabilizer

SSD

FPGA Platforms

Network Switch

Surveillance Camera

WiFi/BT Module

Laptop Docking Station

Smart Watch

Shift to RISC-V for Performance and AI Acceleration

SiFive

Consumer

Edge AI Security Camera

Computational Photography

Mobile & Wearables

Smart TV

Infrastructure

Generative AI

DPU

Storage, Networking

5G

Automotive

Standalone ADAS

Central Compute

IVI

Accelerating the RISC-V Software Ecosystem

HiFive Premier P550 Board

Key points

- High performance RISC-V CPU board
- Focusing on a comprehensive out of the box experience
- More information here

What might not have been obvious from the PR

- This is effectively an embedded RISC-V PC
- Expected to be fastest performing RISC-V dev board in market

What can you expect next?

- Broader portfolio of HiFive development boards
- More news and announcements coming soon…

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SiFive Product Update

2024 - A Year of Product Portfolio Expansion

Embedded ("Essential")

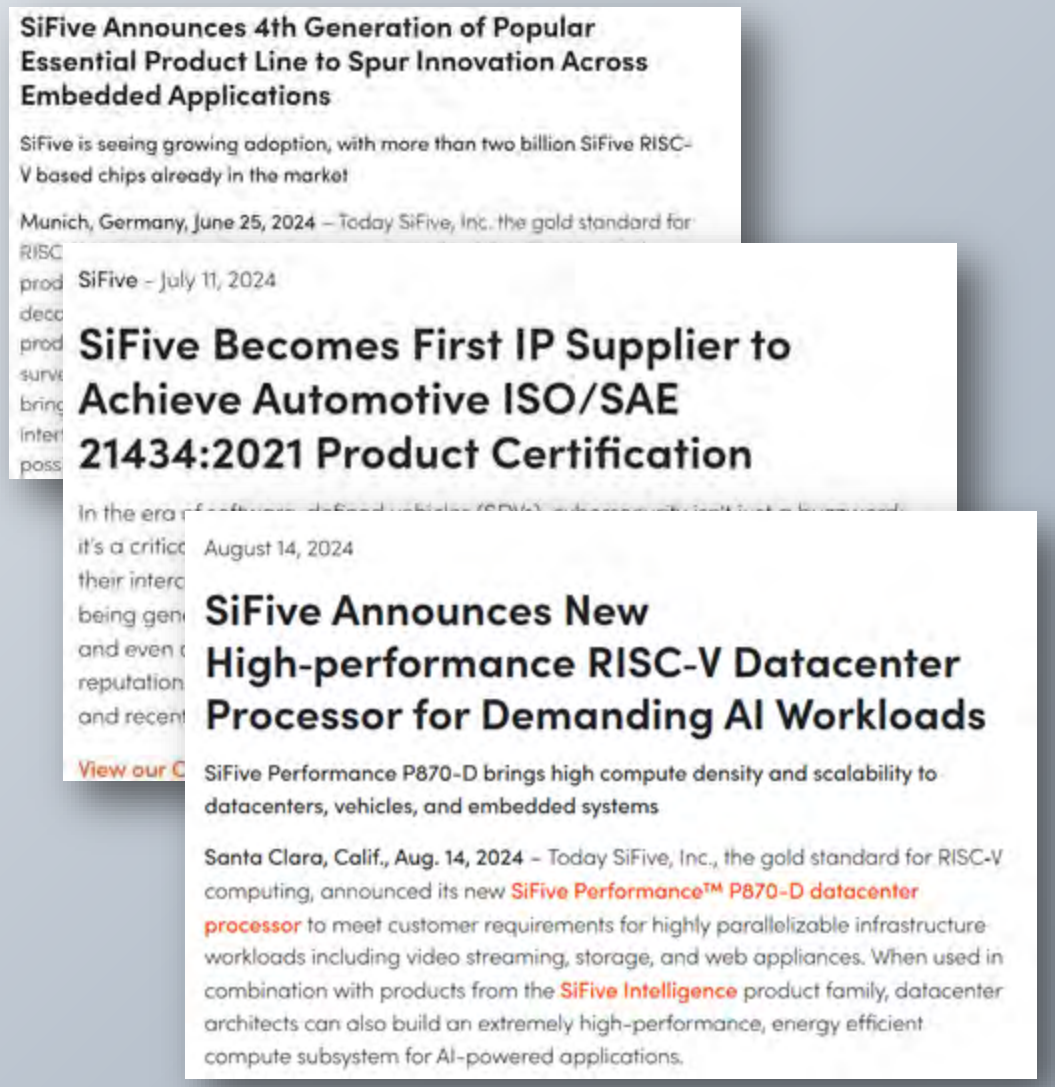
- 4th Generation of Essential Family; Improved performance and power efficiency, inclusion of industry-standard interfaces
- ISO 26262 and ISO 21434; First IP provider to achieve ISO 21434 certification

Applications Processors ("Performance")

- P550 Premier Board; Advancing RISC-V open-source software
- P870-D Solution
  - Most performant RISC-V processor available today. Bar none.
  - Emphasis on simplifying creation of scalable systems

AI Compute ("Intelligence")

- Today! **XM Processor**. Leadership processor for accelerating high performance AI workloads



SiFive Announces 4th Generation of Popular Essential Product Line to Spur Innovation Across Embedded Applications

SiFive is seeing growing adoption, with more than two billion SiFive RISC-V based chips already in the market

Munich, Germany, June 25, 2024 – Today SiFive, Inc. the gold standard for

SiFive – July 11, 2024

SiFive Becomes First IP Supplier to Achieve Automotive ISO/SAE 21434:2021 Product Certification

August 14, 2024

SiFive Announces New High-performance RISC-V Datacenter Processor for Demanding AI Workloads

SiFive Performance P870-D brings high compute density and scalability to datacenters, vehicles, and embedded systems

Santa Clara, Calif., Aug. 14, 2024 – Today SiFive, Inc., the gold standard for RISC-V computing, announced its new SiFive Performance™ P870-D datacenter processor to meet customer requirements for highly parallelizable infrastructure workloads including video streaming, storage, and web appliances. When used in combination with products from the SiFive Intelligence product family, datacenter architects can also build an extremely high-performance, energy efficient compute subsystem for AI-powered applications.

ISO 26262 & ISO 21434 Certifications

Key points

- 4 Essential products certified to ISO 26262 (functional safety) and ISO 21434 (cyber security)
- Products and processes are reviewed and audited by an independent third-party (TÜV SÜD)

What might not have been obvious from the PR

- First IP supplier of **any CPU architecture** to achieve ISO 21434

What can you expect next?

- Further expansion of Automotive grade products across all three pillars of compute

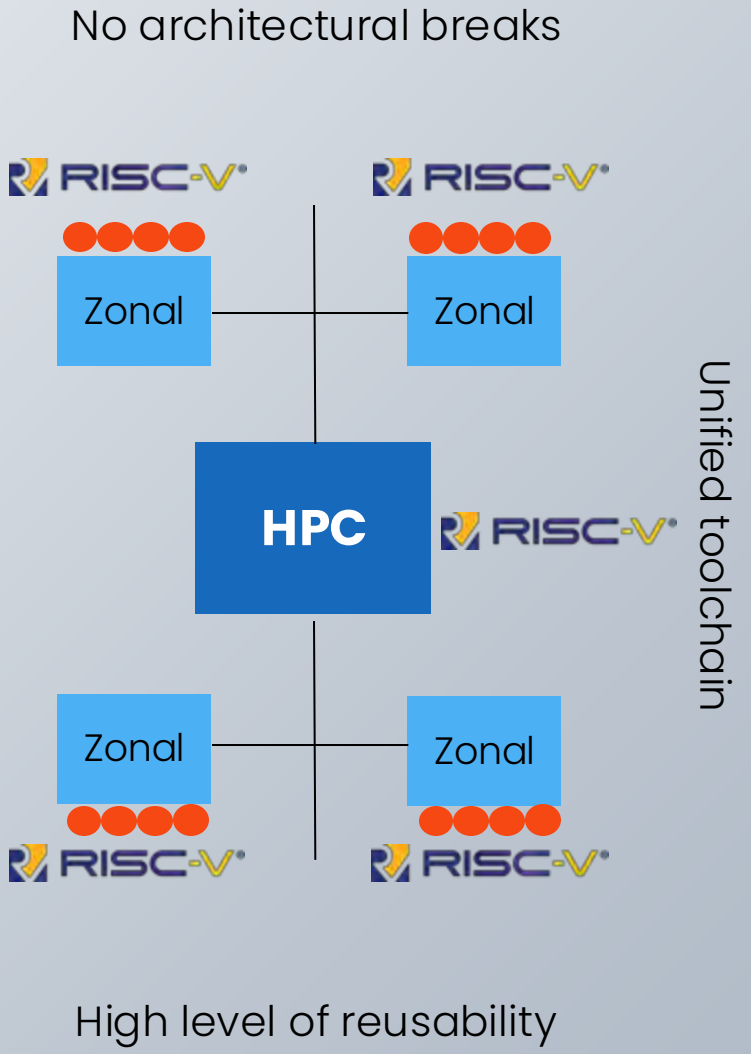
The Auto Evolution – a Better Approach

RISC-V is Open.

RISC-V is Flexible.

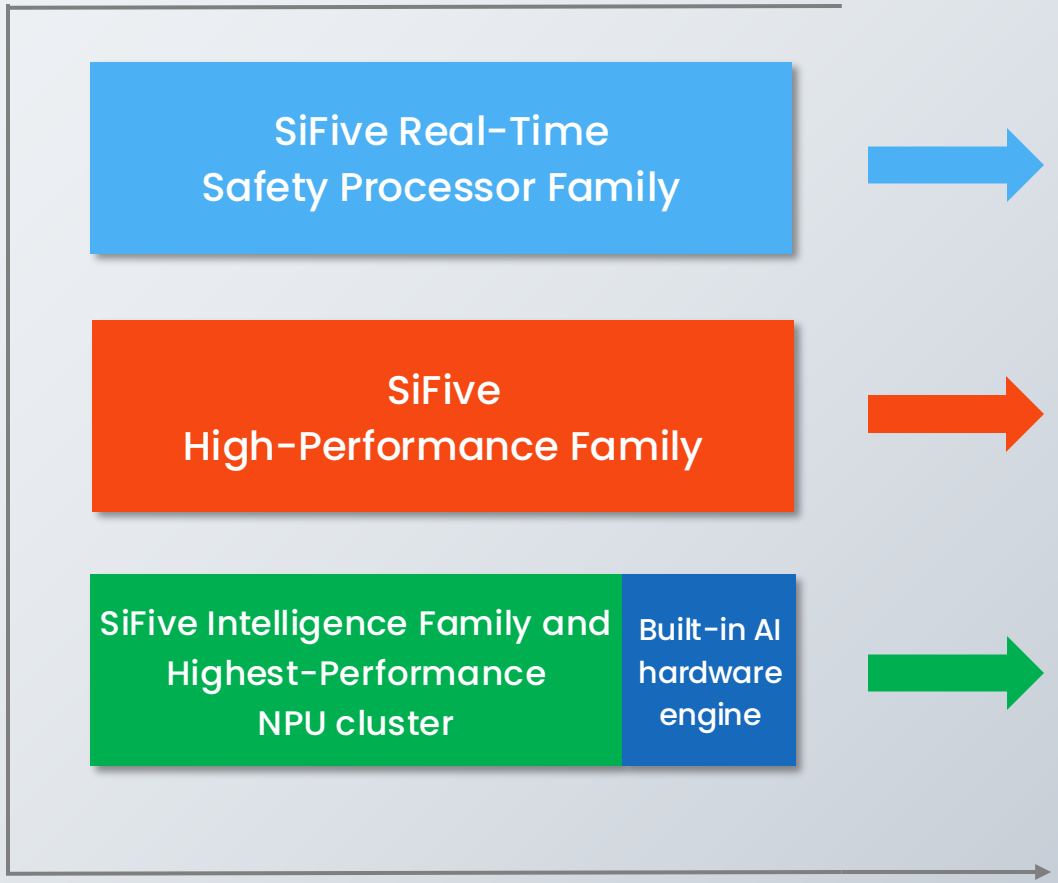
RISC-V is Standardized.

RISC-V is the best architecture for software defined vehicles.



ADAS & Zonal HW Building Blocks

Taking ADAS HW to the next level



Supporting safety automotive control functions (Essential Line, 32- and 64-bit)

High-performance CPU IP class executing general Apps and tasks (Performance Line)

Innovative parallel streams with highest-performance AI TIME engine (X390 + TIME)

Security, IOMMU, Trace, Debug, Peripherals, Cache- and Bus structures, Memory subsystem. NoC, d2d, c2c, coherency, etc

RISC-V Automotive Software Ecosystem

4th Generation Essential Processor Portfolio

Key points

- Major update to embedded products which have shipped in billions of deployed devices
- Family includes cores from 2 stage single issue to 8 stage dual issue, 32- and 64-bit options
- Up to 40% improvement in power over prior generation

What might not have been obvious from the PR

- Very wide scalability & configuration options

What can you expect next?

- A fifth generation, continued innovation & investment
- Expansion of the features, options, configurations

4th generation SiFive Essential IP portfolio

Fully refreshed portfolio with many configuration options to cover all the possibilities

	2-3 Stage Single Issue Lowest Power & Area	8 Stage Single Issue Performance Efficiency	8 Stage Dual Issue High Performance
64-bit Application Processors		**U6** Gen4	**U7** Gen4
64-bit Real-Time Embedded Processors	**S2** Gen4	**S6** Gen4	**S7** Gen4
32-bit Real-Time Embedded Processors	**E2** Gen4	**E6** Gen4	**E7** Gen4

4th generation Essential Updates

Driven by market requirements and customer feedback

Better performance	Lower Power	Latest Features	Improved Interfaces
Improved L2 Cache	Up to 40% Runtime Power Reduction	RVA22 Profile	AMBA ACE Support
Enhanced L1 Memory Performance	New Power Management Features	Hypervisor	More CLPs per Core
Better Code Density		WorldGuard Security	Improved Burst Support
		Advanced Interrupt Controller	
		Secure Debug	

AI Is a Capability, Not an Application

A capability that will be added to virtually all systems

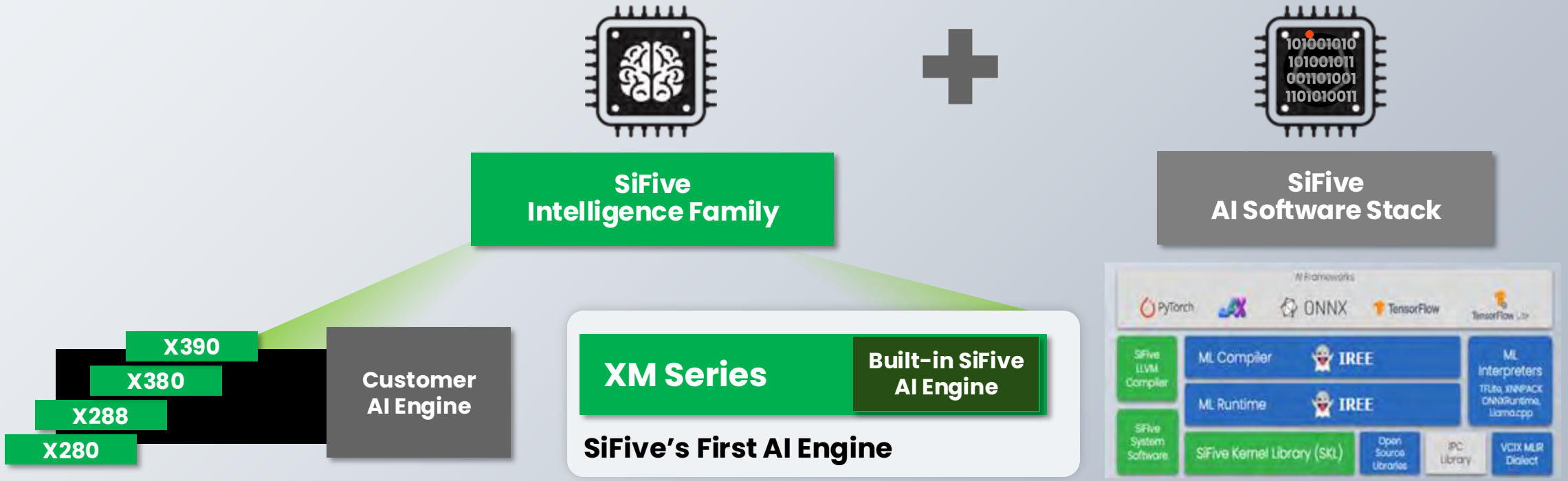
Supports a wide range of devices
From sensors to supercomputers

Addresses different perf/latency requirements
From object recognition to generative AI

Adapts to various market-specific constraints
From data center to memory-constrained systems

A flexible and scalable hardware solution is needed to maximize AI software investment

Today SiFive Expands Intelligence Product Portfolio



New XM series will complement existing X Series portfolio, giving customers more choice

SiFive Intelligence Family Recap

Features

X390
1024-bit VLEN
Single / Dual Vector ALU
VCIX (2048-bit)

X380
512-bit VLEN
Single Vector ALU
VCIX (1024-bit)

X288
512-bit VLEN
Single Vector ALU
Split-Lock with DCLS
CXL Host interface

X280
512-bit VLEN
Single Vector ALU
VCIX (1024-bit)

4x Vector computation compared to X280

4x Data bandwidth compared to X280

2021 2022 2023 Time

Flagship SiFive Based Design Wins

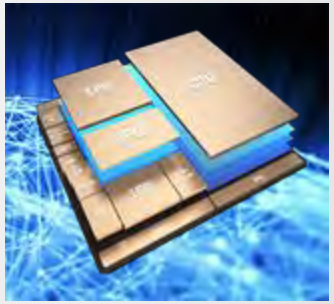
Edge → **Datacenter**

Leading Auto Customers

MICROCHIP

kinara™

SOPHGO



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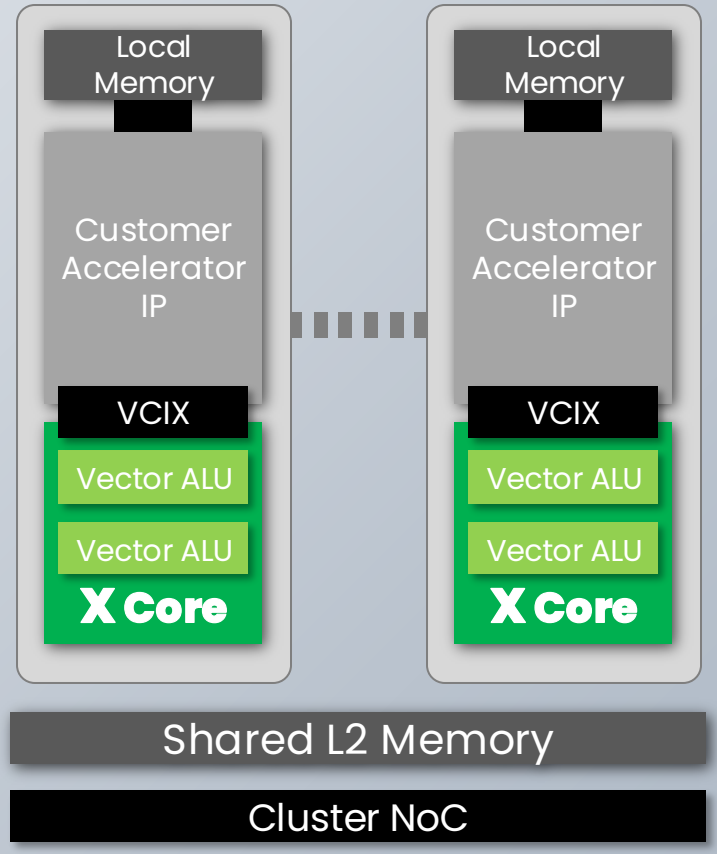
Tier 1 DC Customer

Strong momentum spanning wide range of markets and use cases

Typical Intelligence X Core Implementation Using VCIX

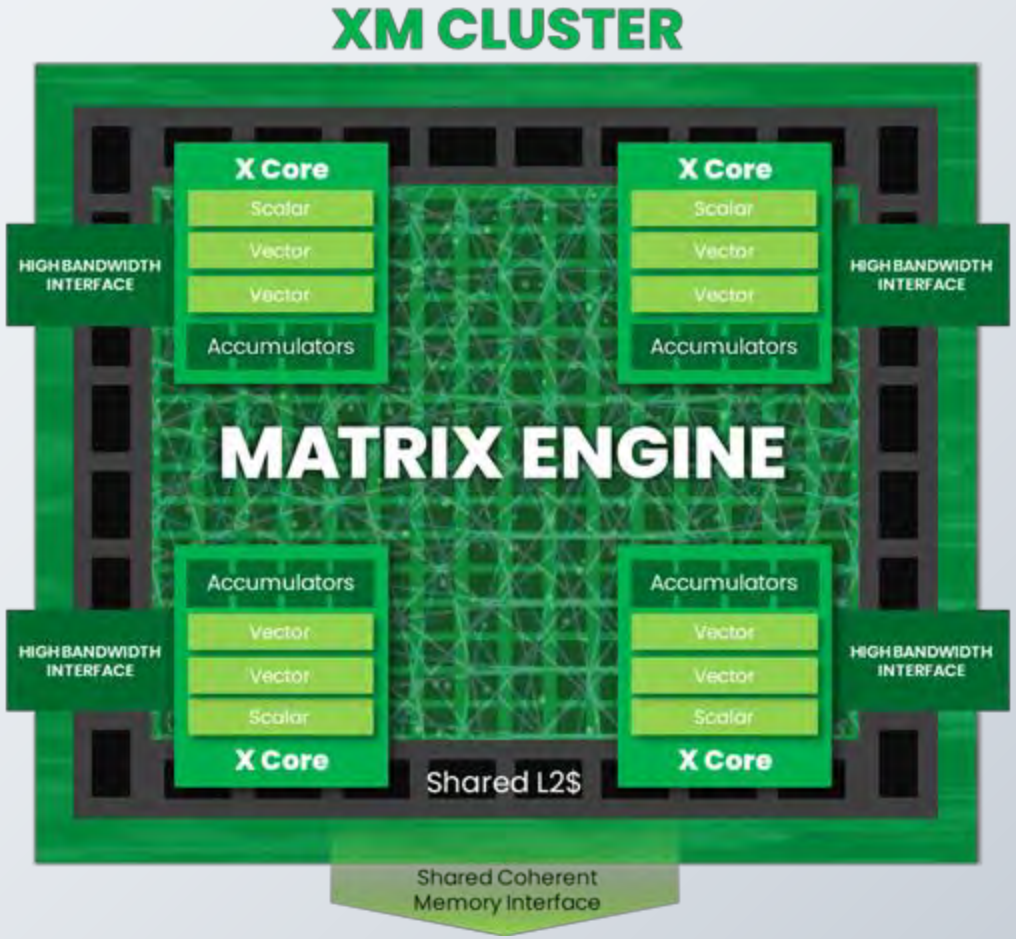
- X-Cores provide RISC-V standards, wide vectors, memory interface, and supported software stack
- Highly scalable coherent memory system to accommodate any AI workload
- Wide VCIX interface to optimize data transfer and reduce latency to customer accelerator IP
- 768GBs of total bandwidth per core
- Provides a rapid way for customers to attach high-bandwidth custom accelerators into a standard RISC-V system



Intelligence Cores with VCIX turn customer accelerators into a scalable RISC-V systems

SiFive XM – Scalable AI Compute Clusters

XM available now for select customers in early evaluation phase



SiFive Matrix Engine

Fat outer-product design
Tightly integrated with 4 X-Cores
Deep fusion with vector units

4 X-Cores per Cluster

Each with dual vector units
Executes all other layers e.g. activation functions
Configurable capacity and bandwidth L2 Cache
New exponential acceleration instructions (up to 64 per cycle per core)

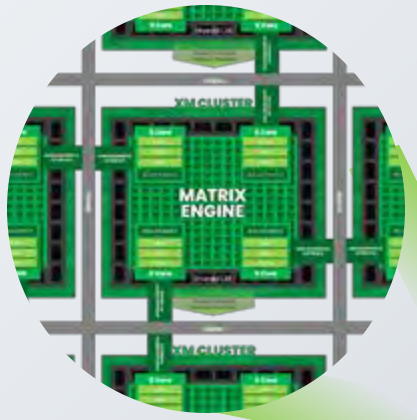
New Matrix Instructions

Fetched by scalar unit
Source data comes from vector registers (INT8, BF16, FP16, FP32, FP64)
Destination to each matrix accumulator (INT32, FP32, FP64)

1 Cluster = 16 TOPS (INT8), 8 TFLOPS (BF16) per GHz
2TB/s Sustained Bandwidth per XM Cluster

Integration of scalar/vector/matrix engines enables extremely memory bandwidth-efficient compute

Extremely Scalable AI Perf



4,096
512
64
8
TFLOPS @ BF16

64 TFLOPS @ 1GHz

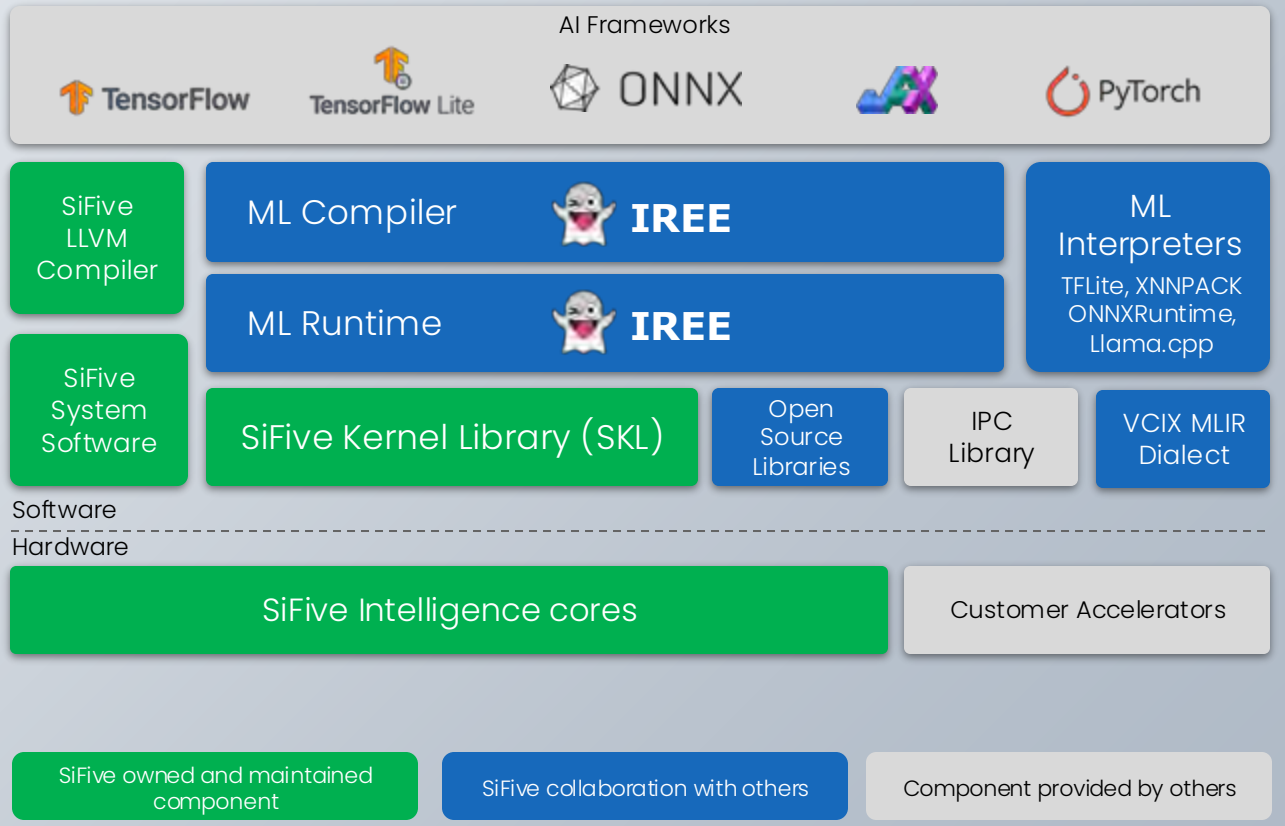
8 TFLOPS @ 1GHz

1
8
XM Clusters
64
512

Massive scalability allowing customers to build up to industry leading levels of performance

Software Strategy for Intelligence Processor Family

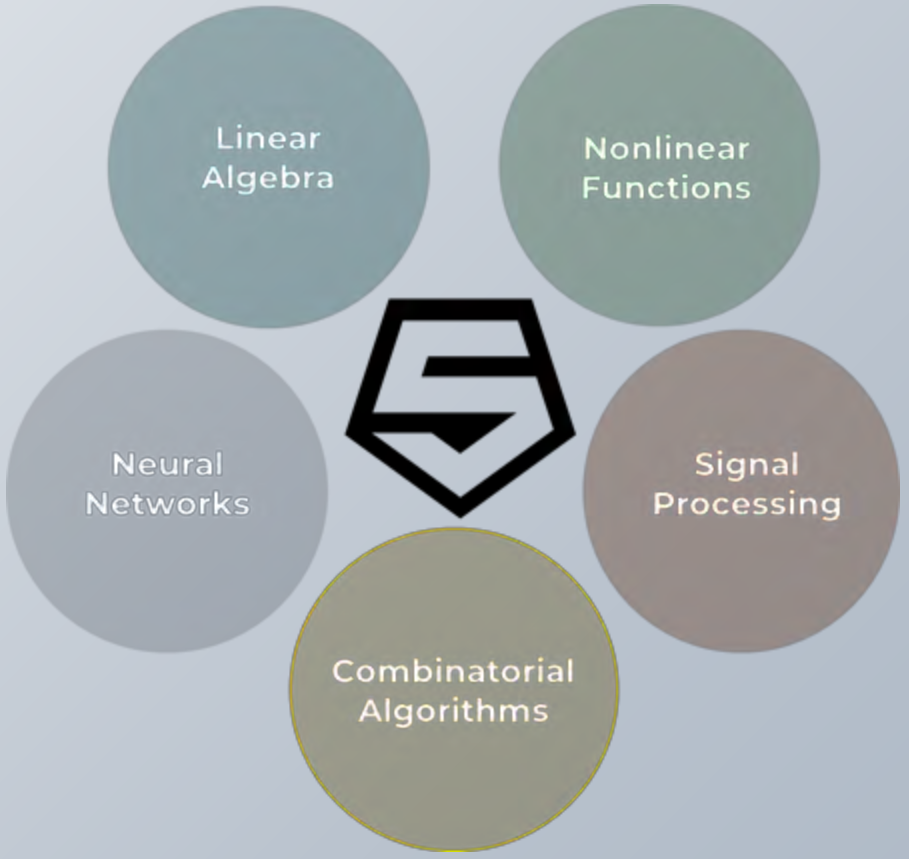
- SiFive will collaborate across the ecosystem to support creation and evolution of comprehensive solutions
- SiFive is focusing engineering efforts on optimizations for its processor cores within common frameworks
- 3+ years investment in software effort to date
- Creating a proven software reference as starting point



Enabling a collaborative full AI software framework

SiFive Kernel Libraries (SKL)

- Organized into five key areas
- Delivers performance acceleration
- Libraries expose standard APIs where applicable



SiFive will open source SKL to provide a proven foundation for customer development and to help align software efforts across the RISC-V ecosystem

Why SiFive?

Real-time processing / Embedded

Application processing / Performance

AI processing/ Intelligence

We invented RISC-V: Nobody knows it better

Complete IP portfolio: >$500M R&D investment

Proven quality: billions of cores shipped, ISO certifications

Customization expertise: workflow geared to enable customer optimized solutions

Trusted advisor: good partners value your interests as much as theirs

Empowering innovators

www.sifive.com