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A Multi-purpose RISC-V Framework

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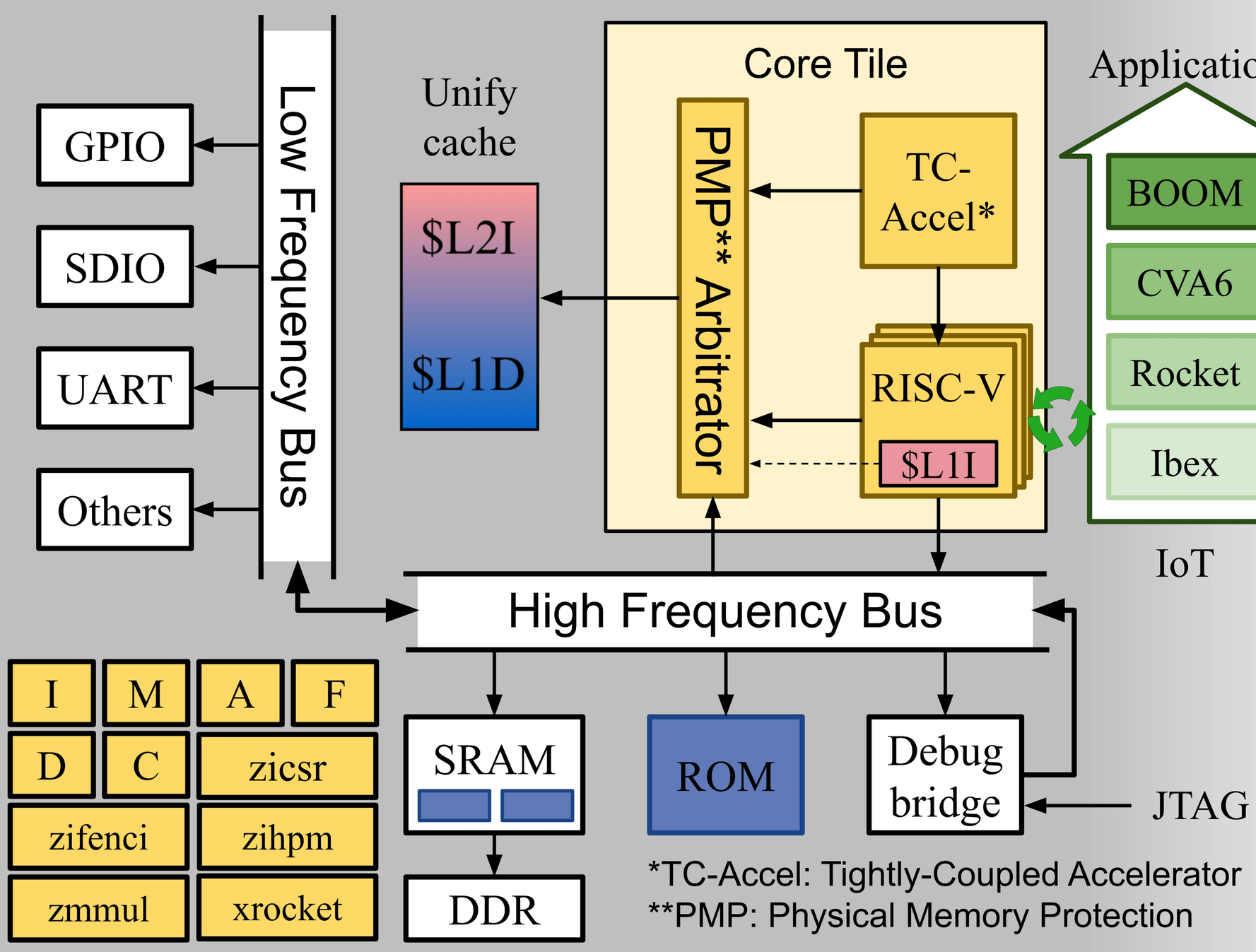
I. INTRODUCTION

This poster presents our motivated RISC-V framework. The open-source RISC-V Instruction Set Architecture (ISA) is increasingly gaining popularity and acceptance, both within the industry and academic communities. The modularity of the RISC-V ISA allows the processors to adapt to a wide range of requirements, from Internet of Things (IoT) devices to application-class processors. In addition, openness facilitates the accessibility of diverse open-source and commercial implementations. These elements could encompass several areas such as security, artificial intelligence, low-power design, and multi-core. Because the RISC-V system designs are subject to distinct requirements, our primary motivation for this work is the provision of an efficient RISC-V framework that offers flexibility to accommodate varying requirements, ranging from "IoT-class" to "application class" capabilities. The foundation of our RISC-V framework is the widely recognized Chipyard framework. This framework enables us to provide a high-level description of the RISC-V system using Scala, a powerful functional programming language. Using Chipyard as a foundation, we enhance the existing configuration and incorporate additional modules to expand the scope of the RISC-V framework. We focus on the interaction between the necessary functionality for small IoT devices, the execution of application-class tasks (such as virtual memory, caches, and several modes of privileged operation), the modularity of integrated components and the energy consumption. The ultimate objective of this effort is to provide an abstract-to-tapeout framework that can be readily managed by RISC-V researchers.

II. The RISC-V framework



The RISC-V Framework

- Reconfigurable from IoT to Application-class.
- Support multi-core.
- Customizable peripherals.
- Support tightly-coupled accelerator.
- Support debugging/ programming through JTAG (OpenOCD, GDB).

Bus sytem

- Hierarchical bus system.
- Based on TileLink.
- Deadlock-free.
- Burst + Atomic access.
- Convertible with AXI-4.

Memory system

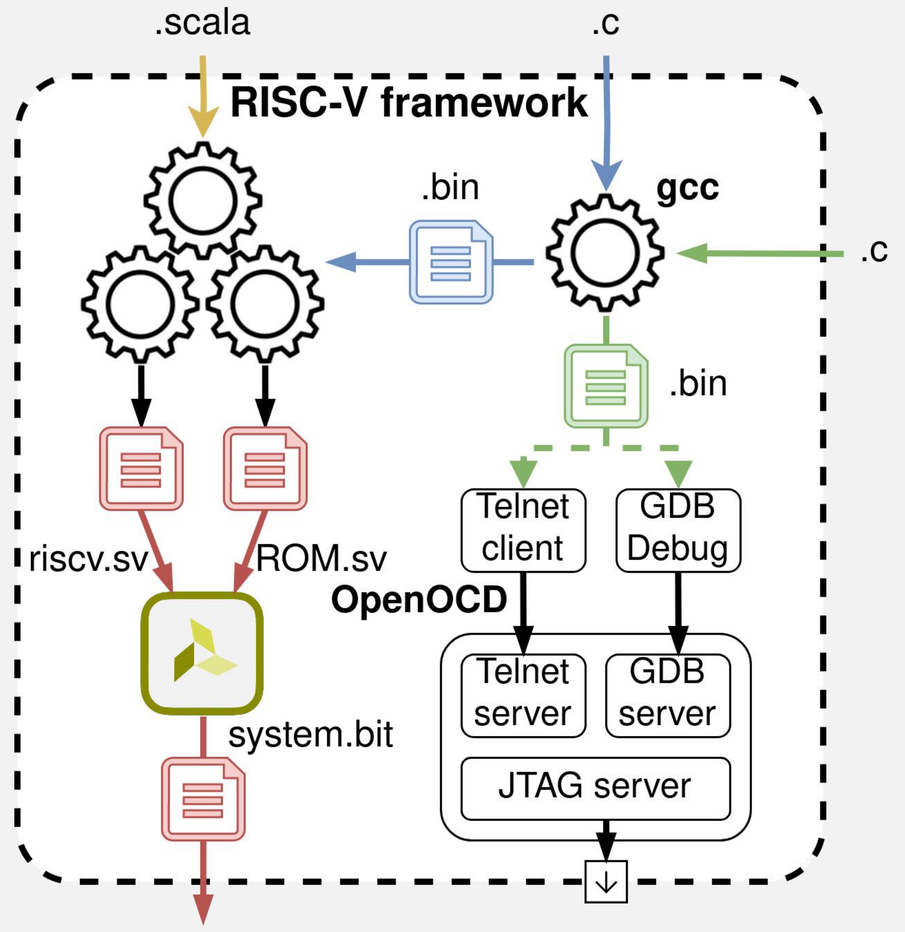
- ROM stores BootROM.
- Two-level instruction cache ($L1I, $L2I).
- Unify cache:
  - L2 Instruction cache.
  - L1 Data cache.
  - Programmable.
  - Direct access.
- Scratchpad SRAM cache for DDR.

III. IMPLEMENTATION & RESULTS

- **Platform** : Arty A7-100T (XC7A100TCSG324-1)
- **RISC-V Core** : Rocket - RV32imac
- **Cache** : 4-KB (I-Cache) 8-KB (Unify D-Cache)

Config	LUTs	Registers	BRAMs	DSP	Freq (MHz)
Tiny	10,198	5,241	6	4	119
DDR	18,718	12,940	6	4	107
DDR + SRAM	22,234	7,068	141	4	104

IV. WORKS FLOW



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