

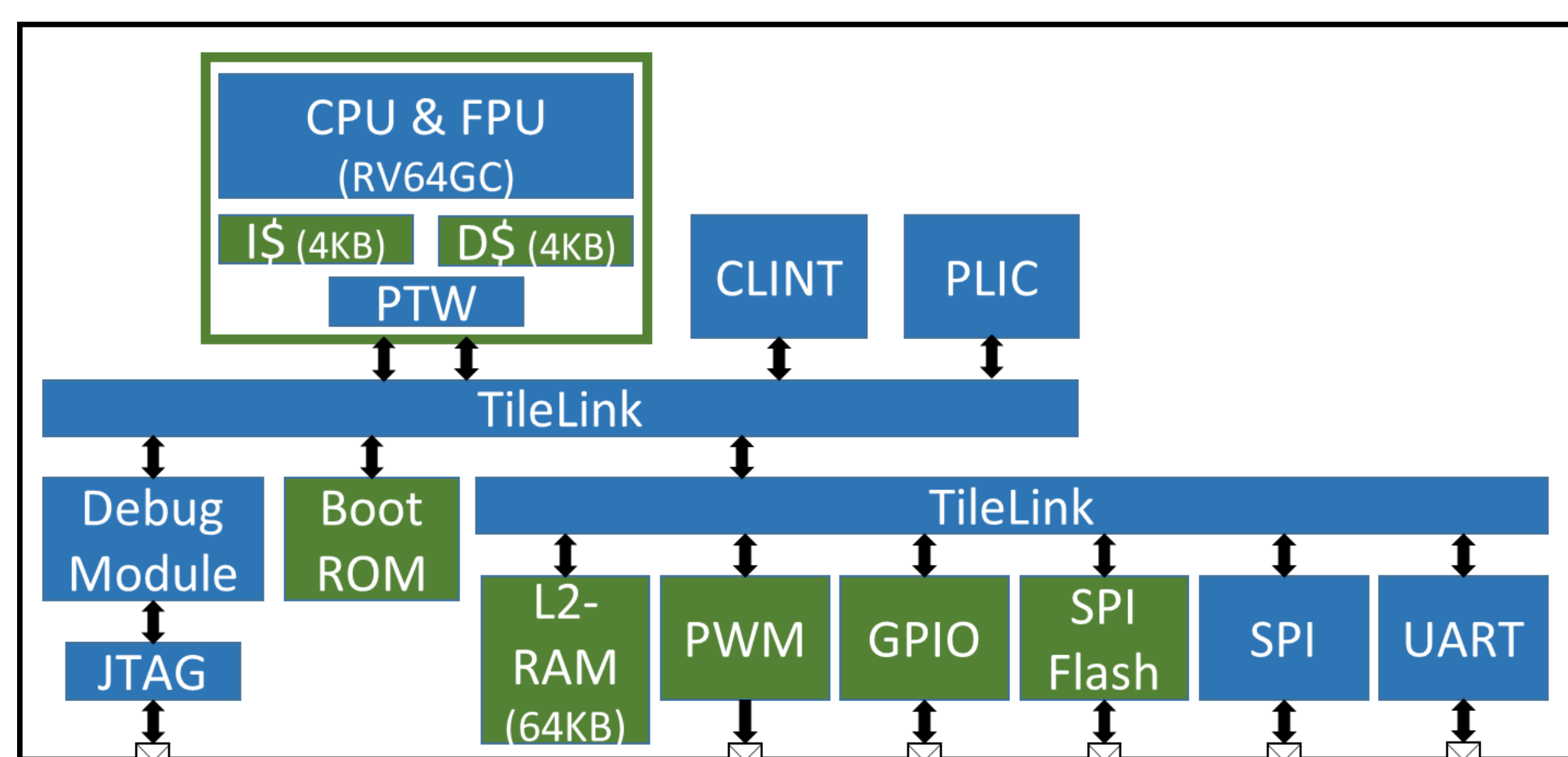
Live Demonstration: Rocket-core on ROHM-180nm and VexRiscv-core on SOTB-65nm

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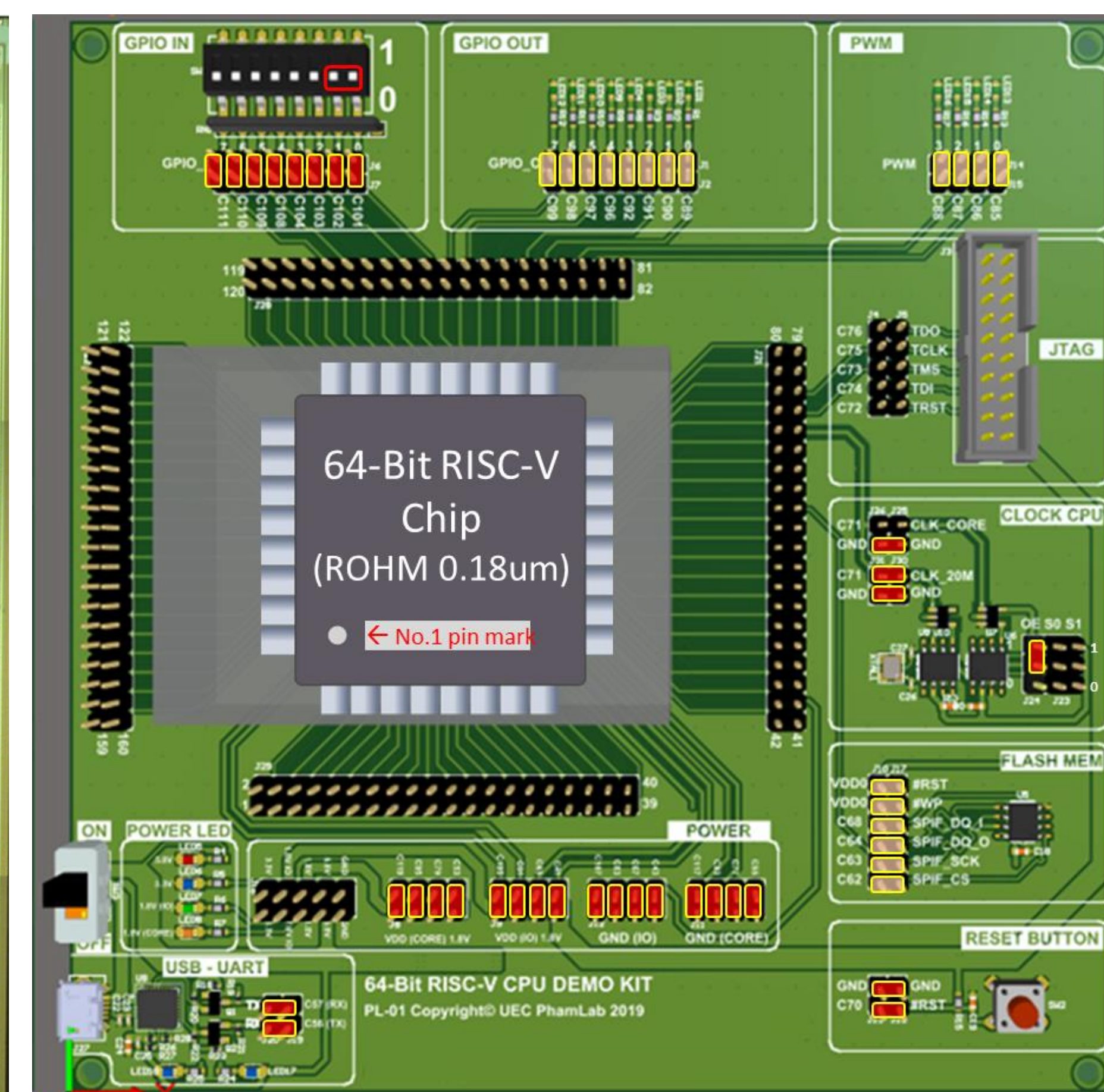
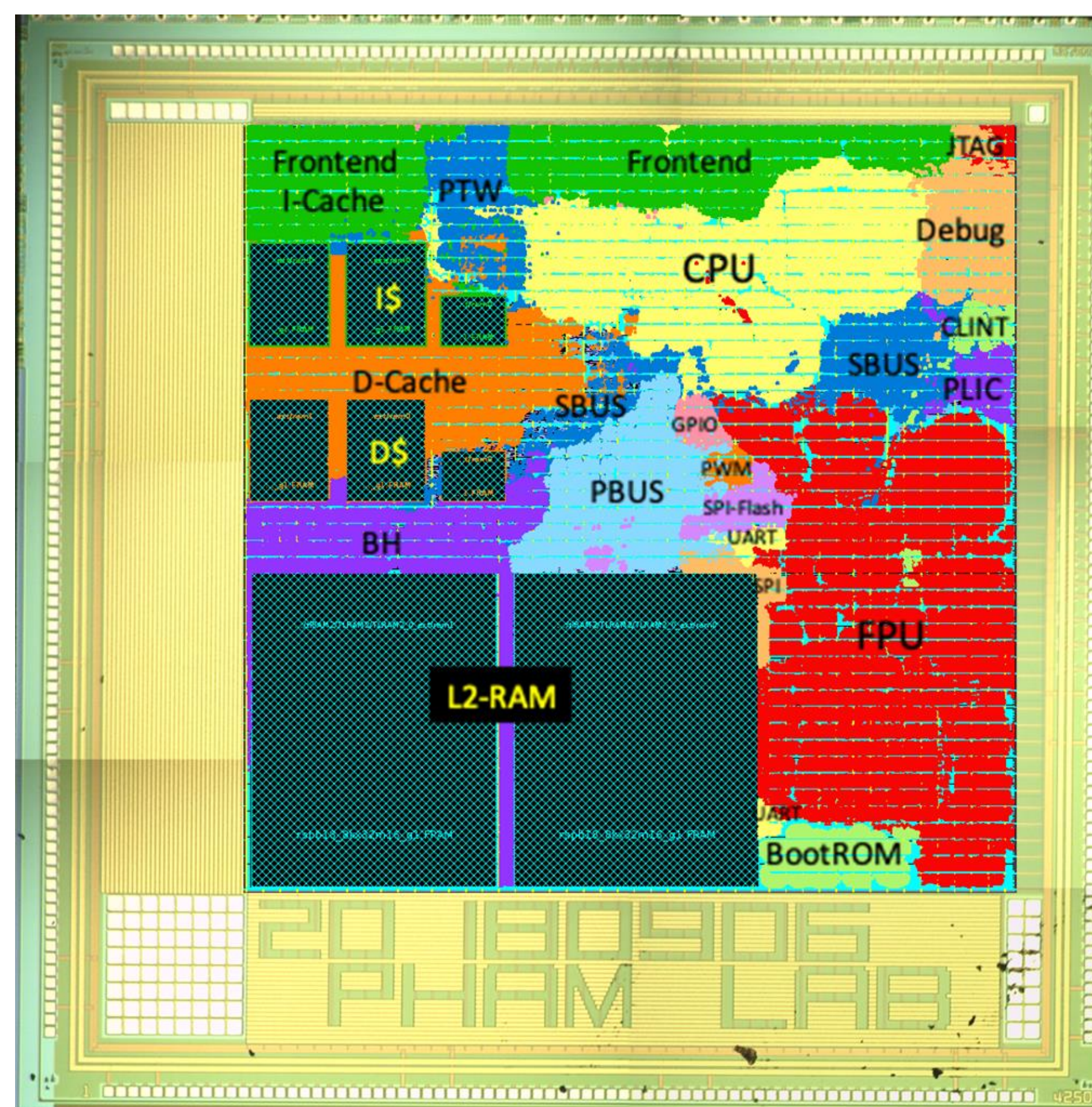
ABSTRACT

This demonstration shows two working chips, one ROHM-180nm chip with Rocket core and one SOTB-65nm chip with VexRiscv core. The Rocket and VexRiscv chips were taped out in September 2018 and August 2019, respectively. The ROHM-180nm Rocket chip is also the first RISC-V chip taped out in Japan. These two chips were among the first RISC-V chips in our laboratory when we started studying RISC-V. The purpose of the two chips is to test and try different Very Large-Scale Integrated circuit (VLSI) implementation strategies.

I. ROCKET CHIP

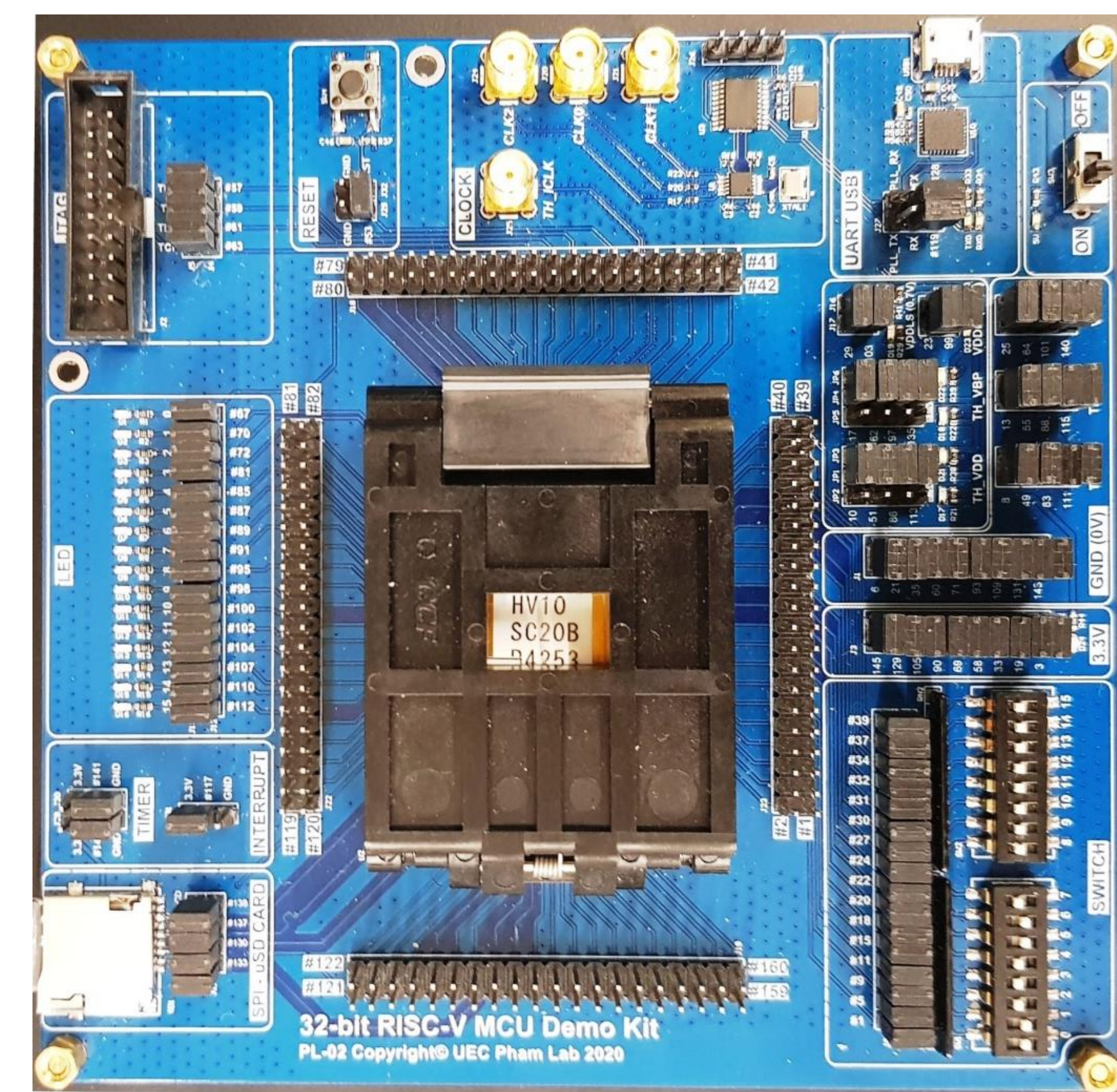
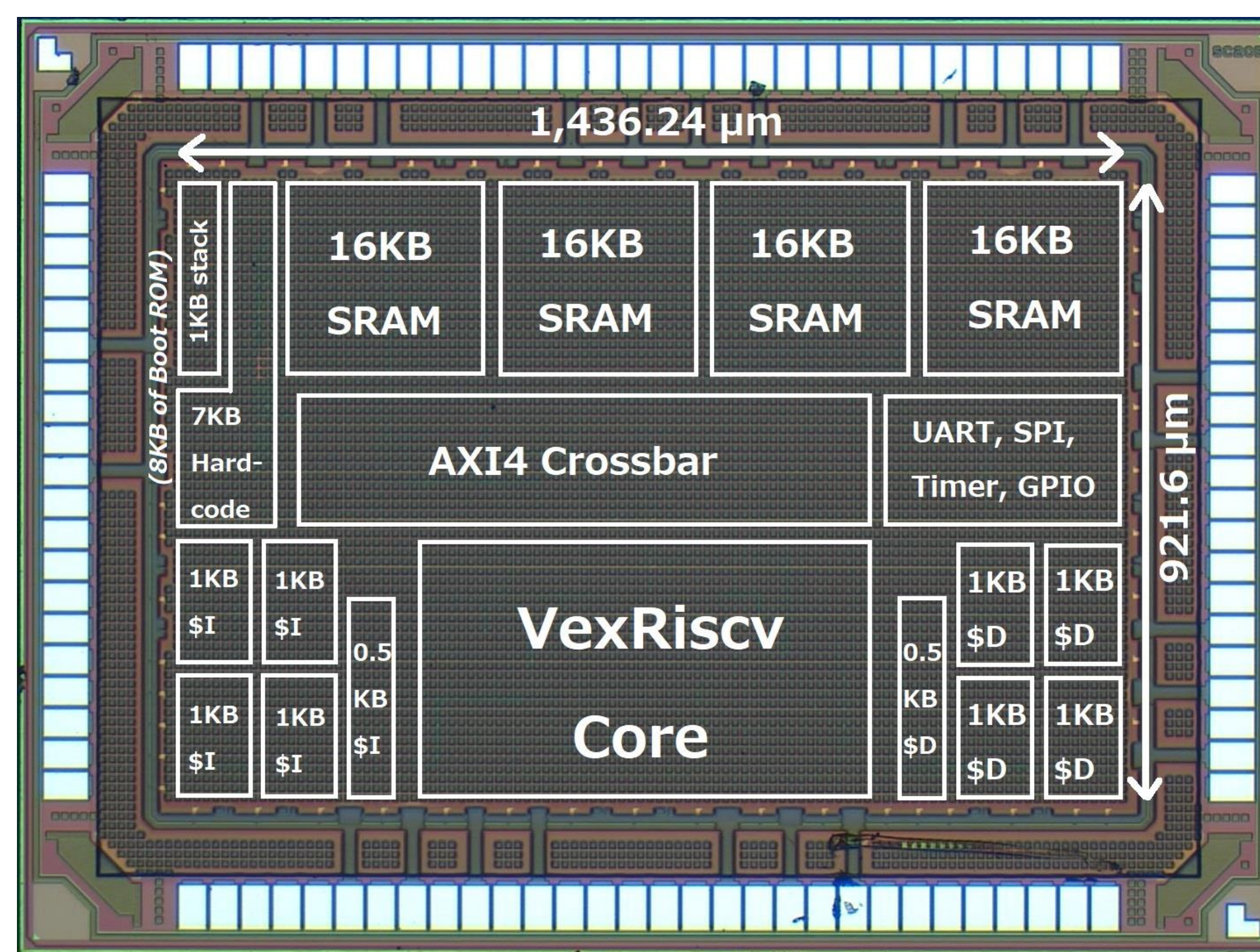
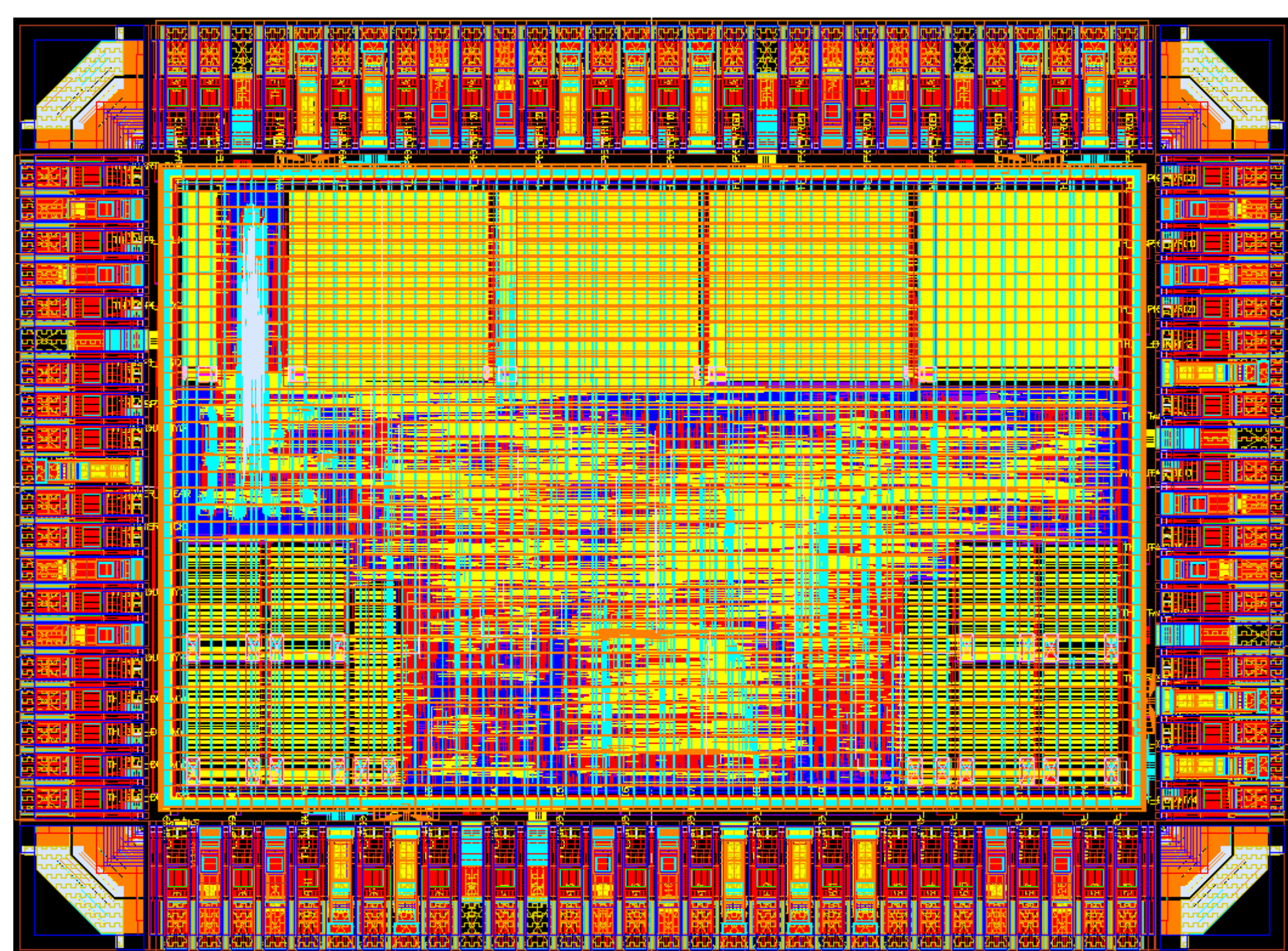


- Based on SiFive Freedom GitHub (Freedom U540-C000)
- Process: ROHM-180nm fab. on September 2018
- Single-core Rocket with RV64GC
- Have MMU with L1 and L2 caches: 4KB instruction cache, 4KB data cache, and 64KB L2 cache
- Core area of $3.75 \times 3.75\text{-mm}^2$ with $\sim 302\text{k}$ gate-count



- Maximum operating frequency $\sim 80\text{MHz}$

II. VEXRISCV CHIP



- Based on SpinalHDL/Vexriscv GitHub (Briey SoC)
- Process: SOTB-65nm fab. on August 2019
- Single-core VexRiscv with RV32IM
- Chip core benchmark: 1.27 DMIPS/MHz and 2.4 Coremark/MHz
- Core area of $1.44 \times 0.92\text{-mm}^2$ with $\sim 349\text{k}$ gate-count

- Peak performance of 156-MHz operating frequency @ 1.2-V V_{DD} and +1.6-V V_{BB} (power density of $270\mu\text{W}/\text{MHz}$)
- Best power density of $33.4\mu\text{W}/\text{MHz}$ @ 0.5-V V_{DD} and +0.8-V V_{BB} (operating frequency of 15-MHz)

REFERENCES

- [1] SiFive Freedom: <https://github.com/sifive/freedom>
- [2] VexRiscv: <https://github.com/SpinalHDL/VexRiscv>
- [3] T.-T. Hoang, *et al*: Low-power High-performance 32-bit RISC-V Microcontroller on 65-nm Silicon-On-Thin-BOX (SOTB), *ELEX*, 2020.

ACKNOWLEDGEMENT

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