Linux Capable RISC-V SoC with OpenXC7 for Educational Purposes

Yimin Gu[1, 2], Xu He[2], Xingyan Chen[2], Shicheng Zheng[2], and Jianliang Lu[2]

1. The University of Tokyo, 2. The University of Science and Technology of China

Contact: guyimin@mail.ustc.edu.cn

RISC-V softcores are already commodities, but... As a student, can you understand the code?

・Due to the complex design, written in another language (Chisel, SpinalHDL, etc), most capable cores are not suitable for beginners. Meanwhile, most smaller cores doesn't have the RV32IMA_Zicsr instructions/interrupts/peripheral interfaces.

・The author, as a student, spent two years writing a Linux capable core, Quasi SoC, in easy-to-read pure Verilog. A rich set of peripherals makes it run on nearly every board.

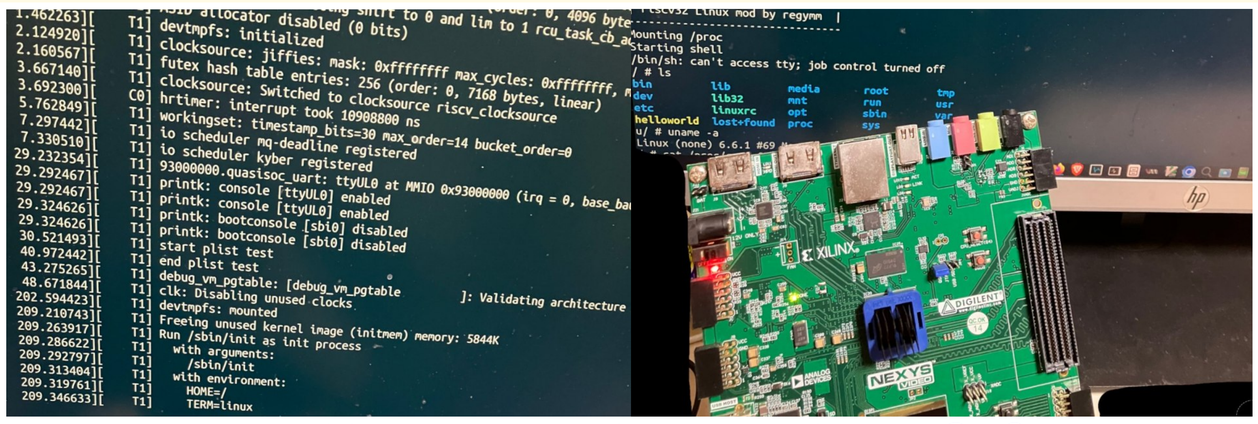
・**32-bit No-MMU Linux**, a good medium-level challenge for students, is supported for the first time, and now upstreamed.

・*The idea is: if I can do this, you also can!*

Simulation quickstart

Huge motivation for beginners

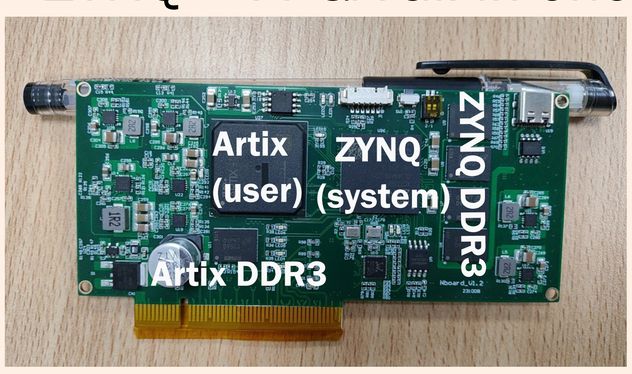
All toolchain dockerized



https://github.com/regymm/quasiSoC

User space	riscv-tests, coremark, video out w/ newlib, raw binary	busybox, ymedit w/ uclibc, bFLT	buildroot userspace w/ glibc, ELF
Operating System	Baremetal	NOMMU Linux	MMU Linux
CPU/peripherals	∂CPU (RV32IMA Zicsr, multicycle 100 MHz, aclint, cache, MMU) QuasiSoC (DDR3, SDRAM, PSRAM, UART, 1842300 baud serialboot, SDCard, HDMI, LCD, VT100 terminal, PS2, W5500, etc)		
Hardware platform	Nexys 4 DDR (Artix 7 100t) -- USTC's course Nexys Video (Artix 7 200t, DDR3) -- current dev platform FPGAOL (Artix 7 35t, Online platform)		

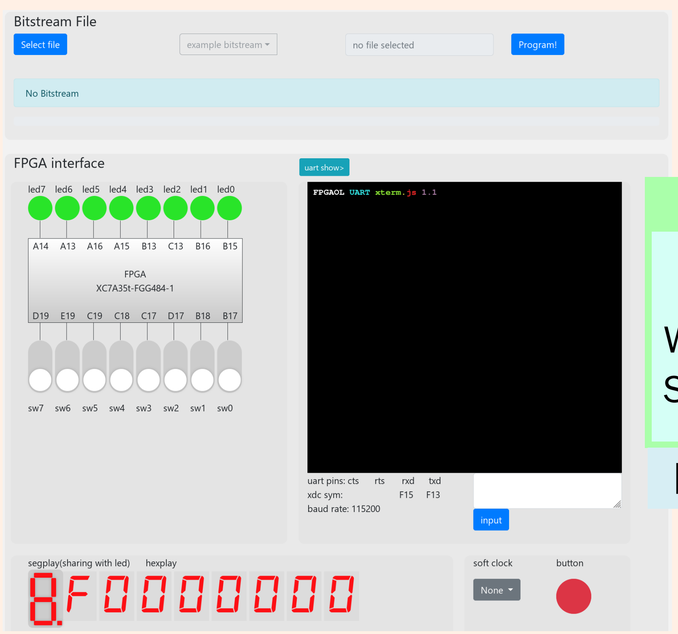
FPGA-as-a-Service: Educational Web platform ZYNQ + FPGA all-in-one solution



FPGAs are fast devices, to sample the customized I/Os, another FPGA is required.

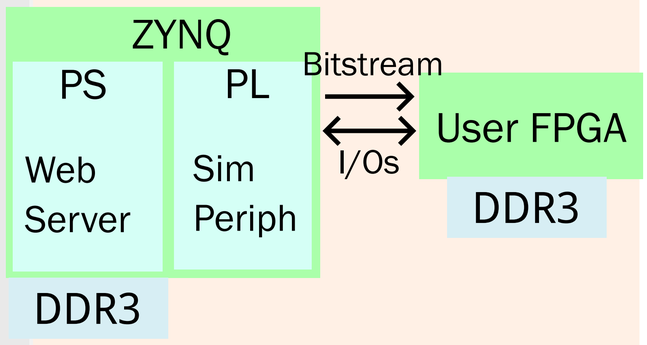
Simulated peripherals brings a flexible amount of LEDs, 7-seg displays, and serial ports.

User's FPGAs can access large storage (128MB to GB level) with a BRAM-like interface, whose content can be uploaded from webpage.



Webpage to interact with real FPGAs

30 nodes are enough to be time-shared by 300 students, even at peak hours.



Plan: make this portable, and everyone having a board can serve it online

Questions in Digital Circuits and Computer Organization and Design courses

Example:

Digital Circuits (ハードウェア構成法, B2 S1) and Computer Organization and Design (コンピュータアーキテクチャ, B2 S2) courses at USTC, using the Nexys 4 DDR

Complains from students:

・Setting up environment is hard!

・Compiling a small design is slow!

・Different from Makefile-based software flow!

My observations:

・In both courses, NO ONE uses DDR! Let alone SD Card!

==> Having large memory/persistent storage is hard

==> No way to understand memory hierarchy

・Synthesis RISC-V code into BRAM is common!

==> No way to load code into softcore

・Debugging is primitive (By LEDs/7-seg display)

==> No way to check memory content if things went wrong

・Only run very small software test code (to fit in BRAM...)

From teachers:

・Hardware is expensive, and breaks over the years

・One board per student is not efficient to manage

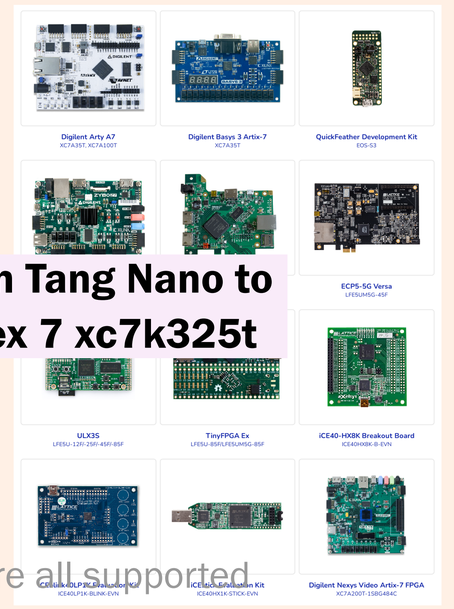
FPGA **OK**
128 KB

256 MB

16 GB

IceStorm, PrjTrellis, and OpenXC7: FOSS FPGA toolchain is no longer a dream

	Project Icestorm	Project Trellis	Project X-Ray	QuickLogic Database
Basic Tiles:	✓	✓	✓	✓
- Logic	✓	✓	✓	✓
- Block RAM	✓	✓	✓	✓
Advanced Tiles:	✓	✓	✓	
- DSP	✓	✓	×	
- Hard Blocks	✓	✓	×	
- Clock Tiles	✓	✓	✓	
- IO Tiles	✓	✓	✓	✓
Routing:	✓	✓	✓	✓
- Logic	✓	✓	✓	✓
- Clock	✓	✓	✓	✓



From Gowin Tang Nano to Xilinx Kintex 7 xc7k325t

f4pga.com

Now DSP, ZYNQ7, MMCM, PLL, IOSDERDES are all supported

- Yosys / NextPnR flow
- When first using OpenXC7, I feel there's **no IP cores!** DDR3?? AXI interconnect?? PCIe???
- Realizing Vivado "free to use" IP cores are NOT free software, but vendor-locking traps!

These are still modern devices: 7-Series lifetime extended to 2035

All-free-software toolchains and IP cores is the coming trend!

Conclusion and Future Expectations

A 32-bit MMU/No-MMU Linux-capable softcore with rich peripherals is implemented by pure Verilog, and supported by OpenXC7, the FOSS FPGA toolchain.

FPGA-as-a-Service online platforms, with the power of emerging FOSS FPGA toolchains, can potentially be a new solution to hardware education.