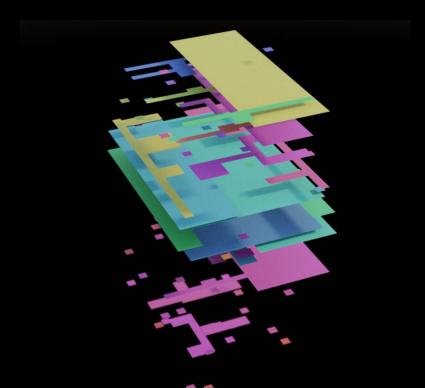
Open Source ASIC tooling



@matthewvenn bit.ly/riscv-japan-2022

ChipFlow





Helping product companies make their own chips

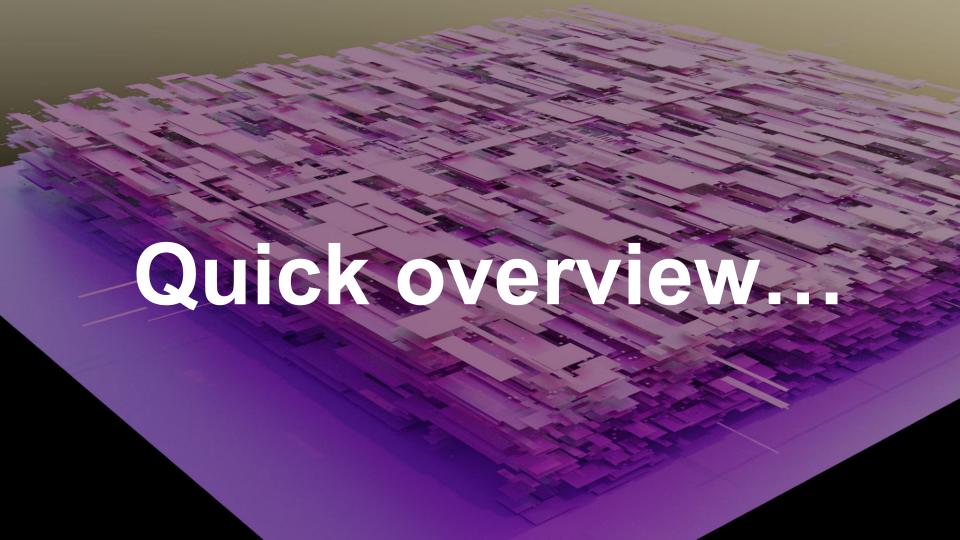
Learn to design your own ASIC and get it fabricated!

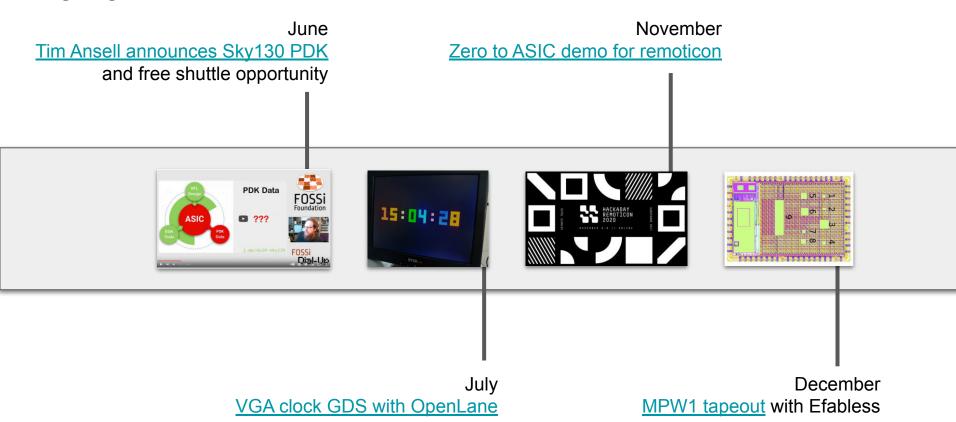
The home for Yosys and related Open Source EDA projects

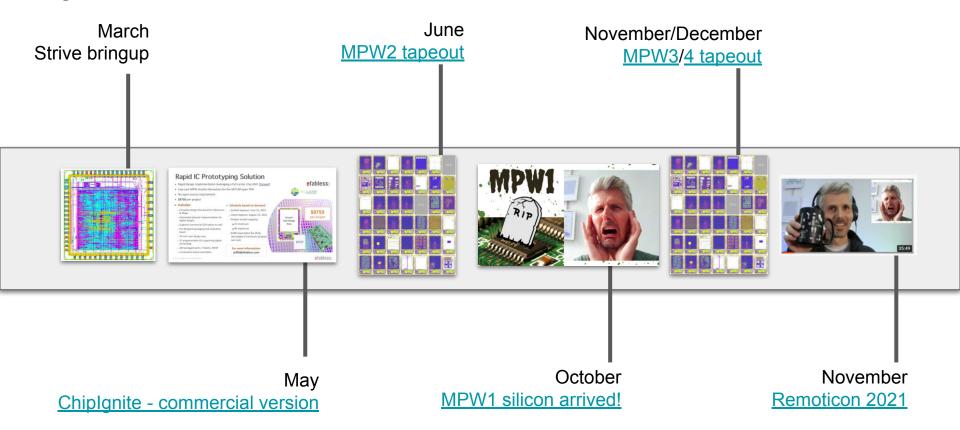
https://www.chipflow.io/

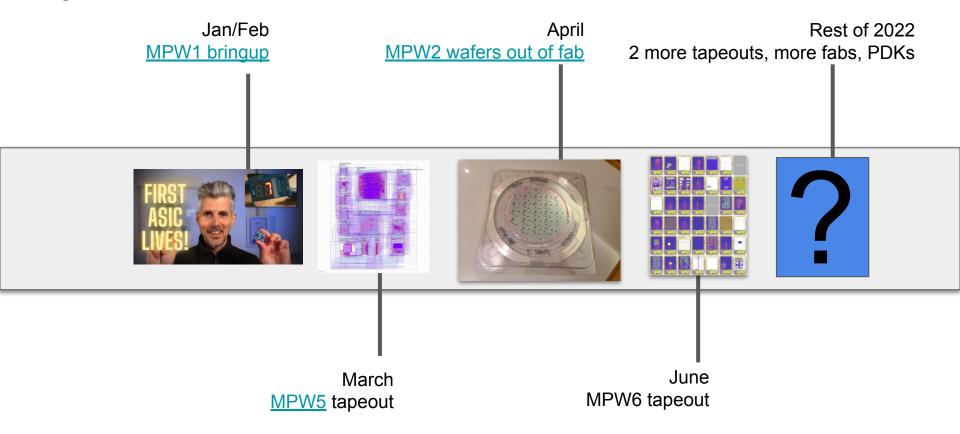
https://zerotoasiccourse.com/

https://www.yosyshq.com/



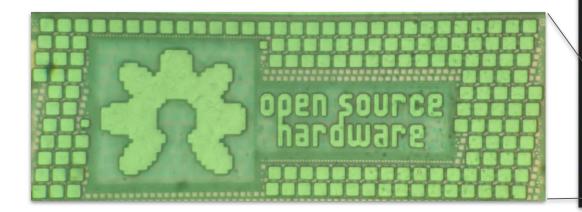


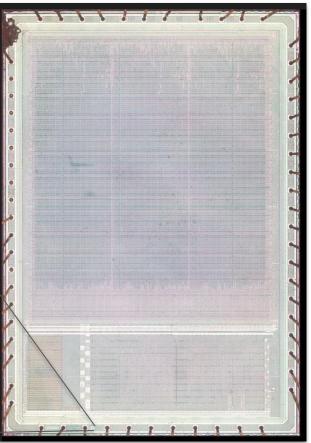


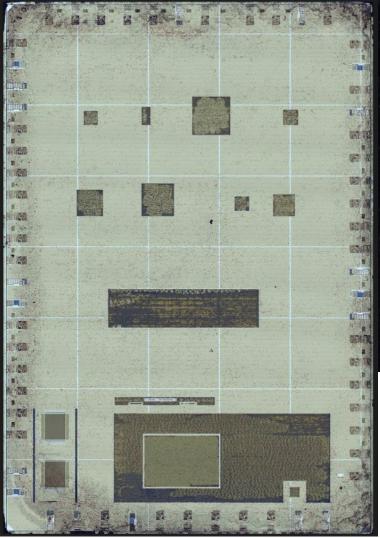


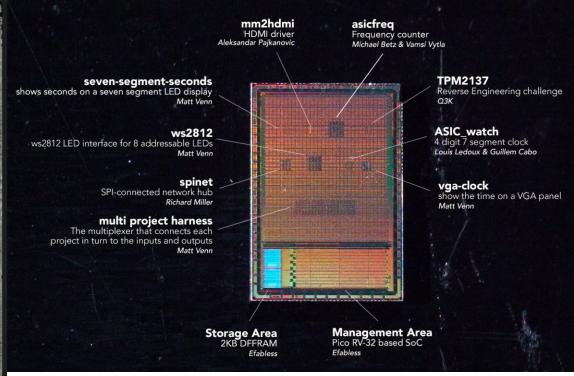
MPW1

- Die imaged by <u>John McMaster</u>
- Zoomable image
- OpenTapeOut talk

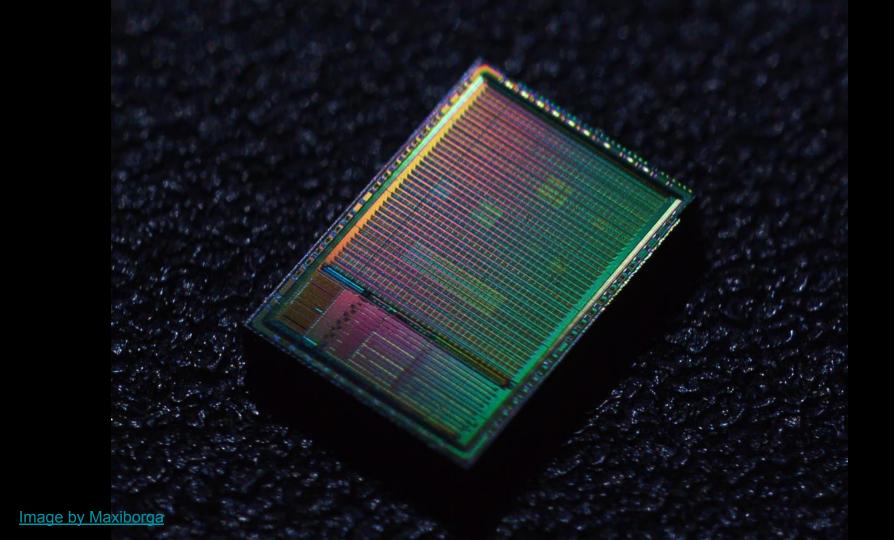








Photos by <u>Maxiborga</u>
Die images by <u>https://www.texplained.com/</u>
Lots more info <u>https://bit.ly/mpw1-samples</u>







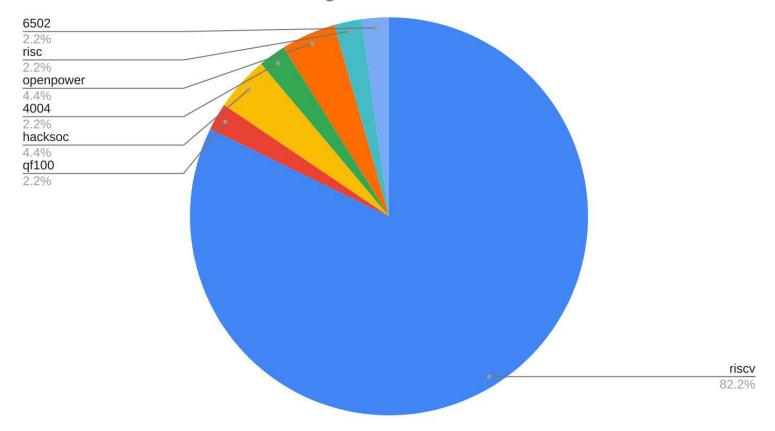
https://zerotoasiccourse.com/post/mpw1-is-alive/

RISCV on the shuttles

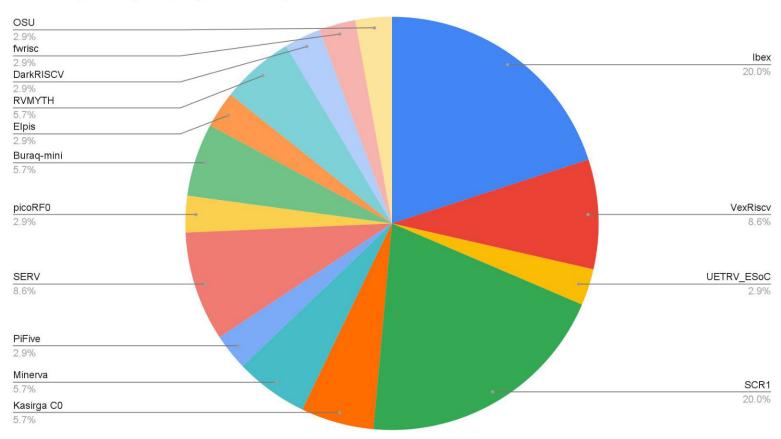
- One 'free' RISCV CPU on each chip: 40 * 5 = 200
 - o MPW1 40 PicoRV32
 - MPW2 to 5 160 VexRISC
- Of the 200 applications, 45 were SoC or CPUs
- 37 of which were RISCV variants
- In total 237 RISCV CPUs across all shuttles so far



45 CPUs were submitted to Google MPW shuttles 1 to 5



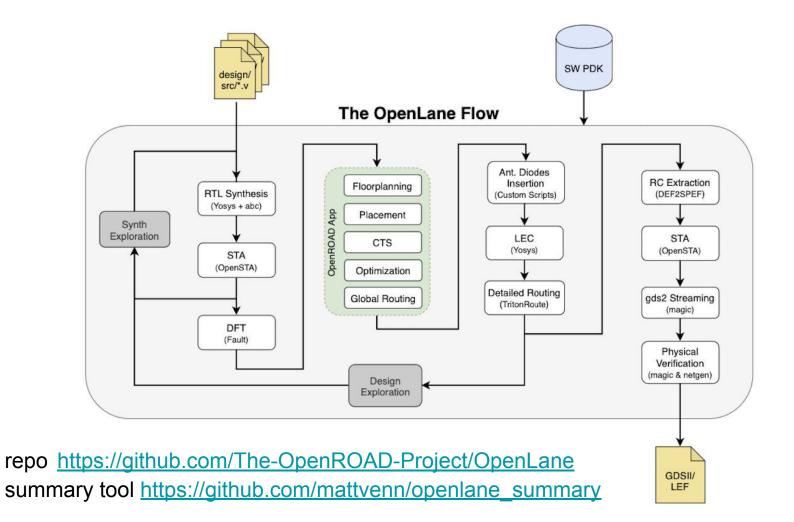
RISCV by base (excluding PicoRV32)



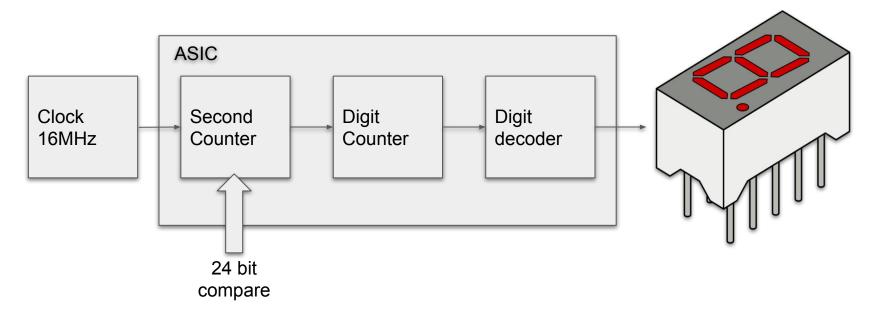
How to get your CPU onto silicon - demo



https://www.youtube.com/watch?v=MNuoYz MM-c

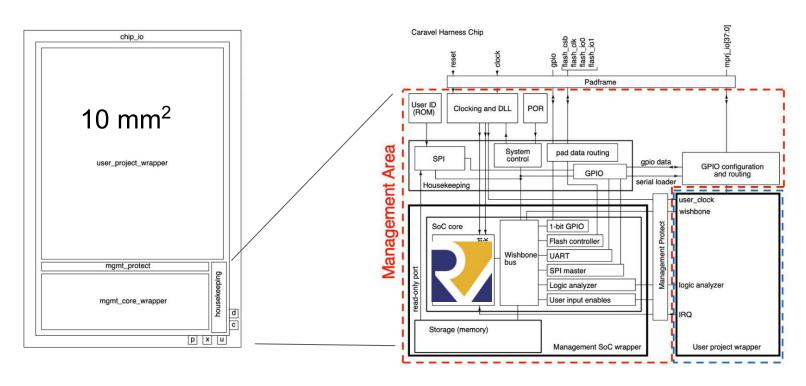


Demo design - 7 segment seconds



- repo https://github.com/mattvenn/seven_segment_seconds
- blog post on the working ASIC https://www.zerotoasiccourse.com/post/mpw1-bringup/

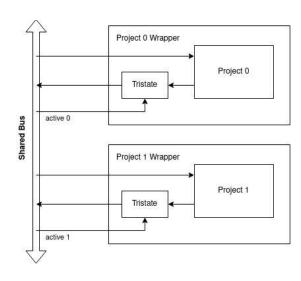
Making a submission to **Efabless**

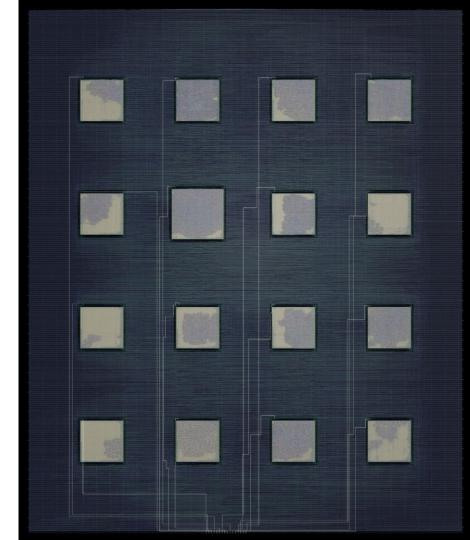


https://caravel-harness.readthedocs.io/en/latest/

Multi Project Tools

- https://github.com/mattvenn/multi_project_tools
- Project outputs isolated with tristate buffers
- Projects are activated by firmware
- Each project has around 300 x 300 um
- Used to submit 70 designs by 35 people across
 5 shuttle runs





ASIC tools in the cloud

- CMOS simulation
- OpenLane

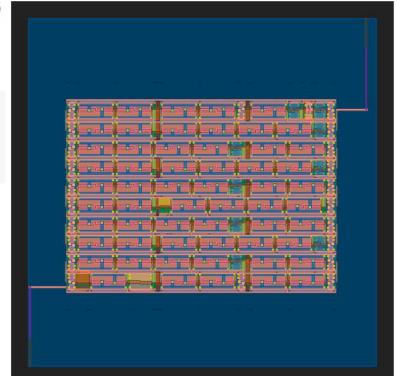
mport matplotlib.pyplot as plt

Follow <u>Proppy on twitter</u>



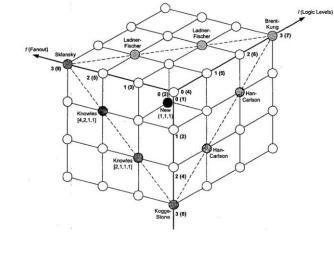
```
import pathlib
import gdstk
import IPython.display

gdss = sorted(pathlib.Path('/content/runs').glob('*/results/final/g
library = gdstk.read_gds(gdss[-1])
top_cells = library.top_level()
top_cells[0].write_svg('inverter.svg')
IPython.display.SVG('inverter.svg')
```



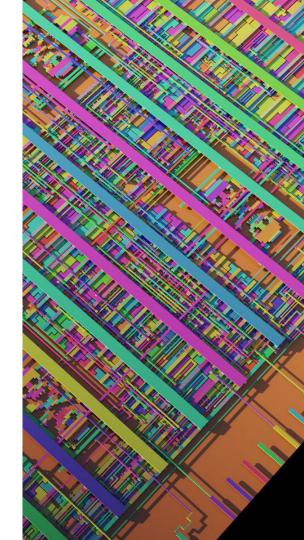
Optimising hardware adders

- When a RISC-V processor boots into Linux, <u>65%</u>
 to 72% of instructions use addition
- Teo's work allows us to create specific adders targeting a specific PPA
- We are <u>instrumenting the adders</u> and taping out on MPW6
- Follow <u>Teo on twitter</u>



Community growth

- 3k Skywater slack members on 120 channels
- Join https://join.skywater.tools/
- 450 stars on OpenLane github repo
- 2k stars on Skywater PDK repo
- 450 public projects with design/GDS on <u>Efabless website for MPW 1 to 5</u>



Get involved!

- Documentation
- Contribute to EDA software
- Next tapeout is MPW6 in June, 7 & 8 later this year

Connect with me!

- Slides https://bit.ly/riscv-japan-2022
- Newsletter
 https://www.zerotoasiccourse.com/newsletter/
- Twitter <u>@matthewvenn</u>
- Linked.in https://www.linkedin.com/in/matt-venn/

