



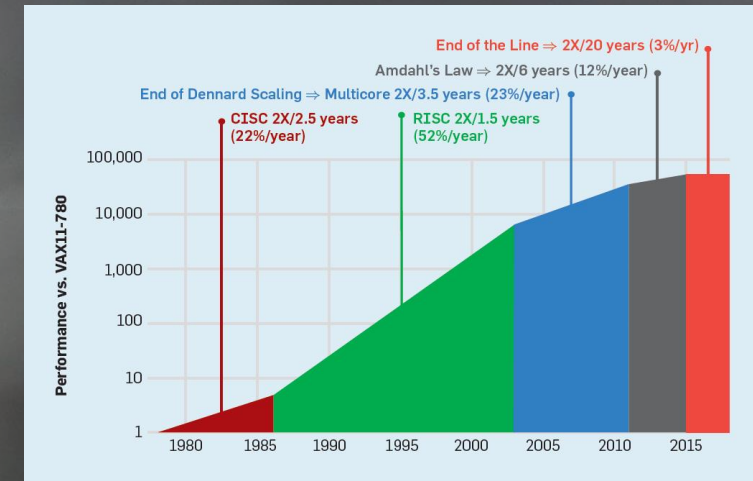
RISC-V: The Time Is Now

Yunsup Lee, SiFive Chief Technology Officer

Transformative Market Opportunity

Compute Requirements Exceed Moore's Law

- AI expanding from Data Center to the Edge
- Growth in Embedded Endpoints
- Shift Away From General Purpose Platforms
 - Highly Optimized Products
 - Domain Specific Architecture
 - Workload Focused Platforms
 - Configurable Core
 - Scalable Product Lines

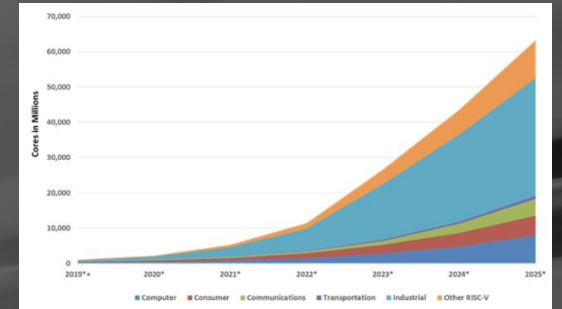


Growth of computer performance using integer programs, A New Golden Age for Computer Architecture ¹

The Time is Right for Freedom of Innovation & Choice

Inflection Point: RISC-V Momentum & Adoption

- Open Standard ISA available for all
- Engineered for practical Use Cases
- Attractive to large Community of Contributors
- Modern, “clean slate” design delivers scalability and superior performance, power and area efficiency
- Reduces the cost of software through community leverage and broad reuse
- RISC-V openness and lack of proprietary lock-in encourages long-term adoption



“Based on the already sizeable adoption of RISC-V, we forecast that the market will consume a total of **62.4 billion RISC-V cores by 2025**”

- Semico Research ²

Bloomberg

“After revolutionizing software, the open-source movement is threatening to do same to the chip industry. ... In just a few years, RISC-V has grown from a college teaching tool into an **open-source standard being explored by industry giants** including Google, Samsung Electronics Co., Alibaba Group Holding Ltd., Qualcomm Inc. and Nvidia Corp.”

- Ian King, Bloomberg ³

RISC-V Community Globally Established & Growing

84 Chip
SoC, IP, FPGA

6 I/O
Memory, Network,
Storage

15 Services
Fab, Design Services

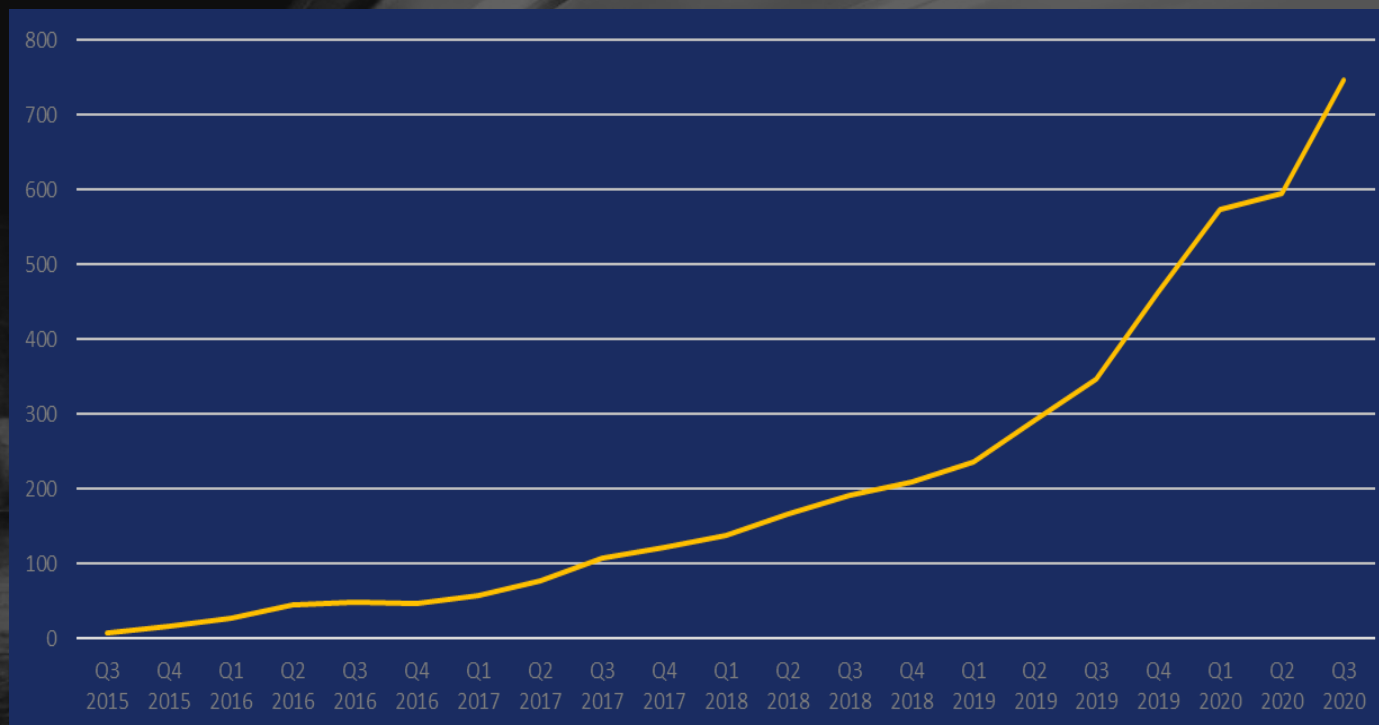
27 Software
Dev Tools, Firmware, OS

4 Systems
ODM, OEM

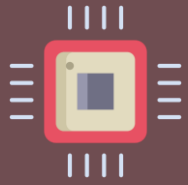
31 Industry
Cloud, Mobile, HPC, ML,
Automotive

49 Research
Universities, Labs, other
Alliances

450+ Individuals
RISC-V Developers &
Advocates



More Than 750 RISC-V Foundation Members in 50 Countries



FPGA Soft Core



Wearables



Photonics Embedded Controller

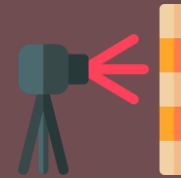
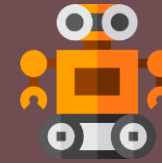


Image Signal Processor EC



Display Adapter



Warehouse Robotics



Satellites



Security Subsystem



FPGA Hardened Core



Fast Storage



Internet of Things



Boot Controller



Augmented Reality

More Than 200 Design Wins with 80 Companies including 6 of the Top 10 Tech Companies



Smart Cities



Voice Recognition



Audio Processor



Wi-Fi & BLE



Data Plane Embedded Controllers



Industrial Robotics



Human Interface Devices



Networking Embedded Controller

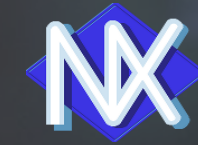


Edge AI Controller



Educational Technology

Embedded RTOS & Tools For RISC-V



Open Source

Commercial



Linux & Apps for RISC-V

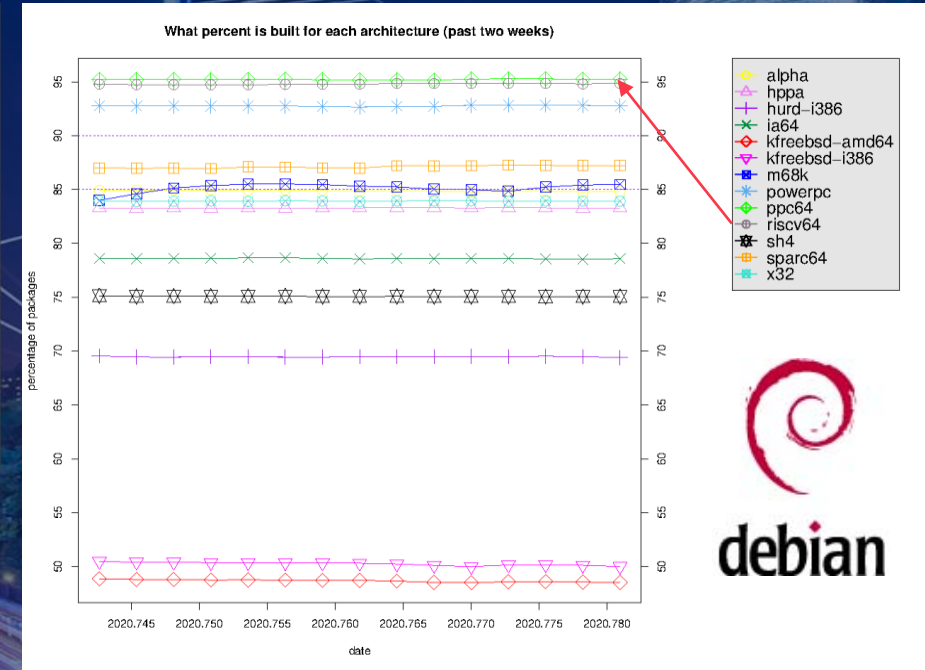




Debian on RISC-V

Debian builds ~95% of packages on RISC-V

- Milestone in becoming 'normal' architecture
- Docker, Kubernetes demonstrated on Debian using SiFive HiFive Unleashed



Graph produced October 13th, 2020 - <https://buildd.debian.org/stats/>

Yes, we can!

carlosedp/echo-riscv

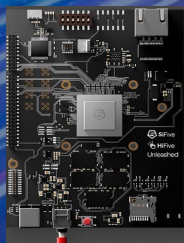
```
Linux qemu-riscv 5.3.0-rc4-g6c2a8bd-dirty #6 SMP Fri Nov 22 18:00:43 -02 2019 riscv64 GNU/Linux
root@carlosedp/echo-riscv:~# docker build -t carlosedp/echo-riscv .
[+] Building 4.26s (5/5) FINISHED
--> [internal] load dockerignore
--> -- transferring context: 38
--> [internal] load build definition from Dockerfile
--> -- transferring Dockerfile: 37B
--> [internal] load build context
--> -- transferring context: 39B
--> CACHED [5/5] COPY echo-riscv /echo-riscv
--> exporting to image
--> -- exporting layers
--> -- writing image sha256:73107a1f5118086f308158877ba8130fba14a8780745aa261d51fca46081f2
--> -- naming to docker.io/carlosedp/echo-riscv
root@carlosedp/echo-riscv:~# docker run --name hello -d -p 8085:8085 carlosedp/echo-riscv
bf363a272b79a71731c8664e8524982a16708c3110bf47713baf11aa48999
root@carlosedp/echo-riscv:~# curl localhost:8085
Hello, I'm running Echo inside a container on linux/riscv64
```

#RISCVSUMMIT | tmt.knected.com/risc-v-summit/

Orchestration Works on Risc-V too!

Cloud Native Computing Foundation, Kubernetes, K3S, Prometheus, OpenFaaS

#RISCVSUMMIT | tmt.knected.com/risc-v-summit/



Carlos Eduardo de Paula (Sr. Cloud Architect, Red Hat)
 RISC-V Ambassador
 "The RISC-V Journey Thru Containers to the Cloud" (RISC-V Summit 2019)



fedora^f Fedora on RISC-V

2018

- Western Digital Fedora desktop tutorial

2019

- ABOpen RISC-V Machine working with SiFive, MicroChip, Fedora, Debian, and Western Digital using Unleashed + FPGA expansion board

2020

- EFI Boot on HiFive Unleashed & QEMU

AB Open > News > Community > Western Digital Releases Fedora Desktop on RISC-V Tutorial

Western Digital Releases Fedora Desktop on RISC-V Tutorial



```
Hit any key to stop autoboot: 0
EFI stub: Booting Linux Kernel...
EFI stub: ERROR: Could not determine UEFI Secure Boot status.
EFI stub: Using DTB from configuration table
EFI stub: Exiting boot services and installing virtual address map...
[.]
[.] 0.000000] efi: EFI v2.80 by Das U-Boot
[.]
[.] 0.156407] Remapping and enabling EFI services.
[.] 0.168771] smp: Bringing up secondary CPUs ...
[.]
[.] 3.602015] systemd[1]: Detected architecture riscv64.

Welcome to Fedora 32 (Rawhide)!
```

Welcome to the Fedora/RISC-V disk image
<https://fedoraproject.org/wiki/Architectures/RISC-V>



Tommy Thorn @iamtommythorn · Oct 1

It gives me such great joy to install #rustlang via rustup in QEMU VM running #Fedora #riscv and pull over my projects and Everything Just Works(TM). Thanks to all.



1



8



14



Tommy Thorn @iamtommythorn · Oct 9

Update: Rust 1.47 was released and can be installed directly from rustup.rs with no fuss. 🌞



1



8



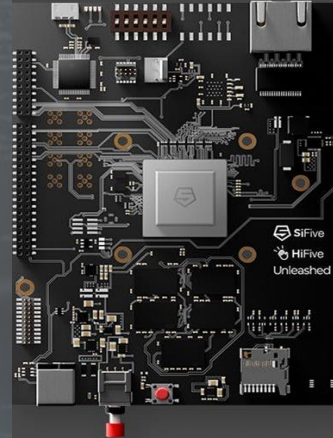
14





SiFive HiFive Developer Systems

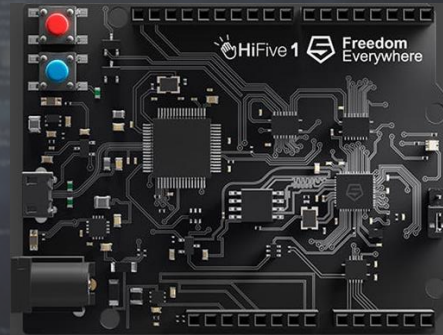
Application &
Linux
Development



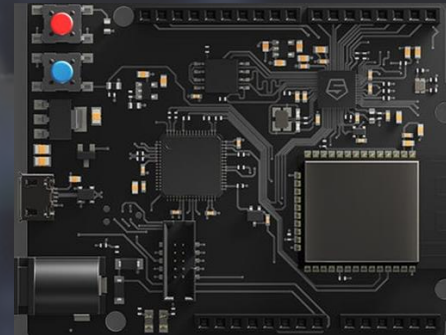
HiFive Unleashed



Embedded
Development



HiFive1



HiFive1 Rev B

Enabled First
Wave of
Ecosystem
Development

RISCV[®] Software

Project	RISC-V Status	Recommended source release
GCC	Upstreamed as of 7.1	Upstream or https://github.com/sifive/freedom-tools
LLVM	Upstreamed as of 9.0	https://github.com/llvm/llvm-project
GDB	Upstreamed as of 8.3	https://github.com/riscv/riscv-gnu-toolchain
binutils	Upstreamed as of 2.28	Upstream
newlib	Upstreamed as of 2.5	Upstream
glibc	Upstreamed as of 2.27	Upstream
Linux Kernel	Upstreamed as of 4.15	Upstream or https://github.com/sifive/riscv-linux
QEMU	Upstreamed as of 2.12	Upstream



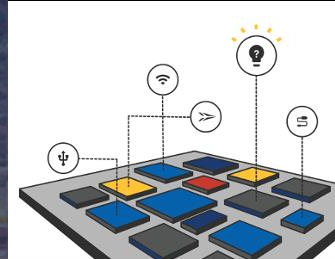


SiFive Software Products

Freedom Studio

Eclipse C/C++ Development Environment

- SiFive RISC-V Cross Compiler
- SiFive OpenOCD Debugger
- SEGGER J-Link Debugger
- SiFive QEMU Emulator
- SiFive Freedom E SDK Software



Freedom Tools

RISC-V Development Tools

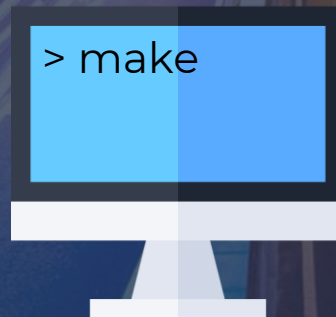
- GNU Newlib Toolchain
- OpenOCD
- QEMU
- SDK Utilities
- Trace Decoder
- XC3SPROG



Freedom E SDK

Bare Metal Software Development

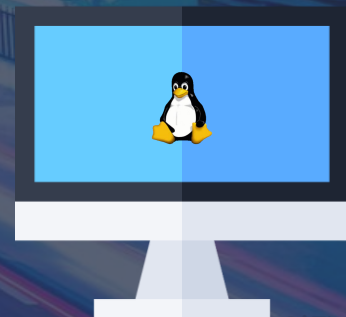
- Example Programs
- Industry Standard Benchmarks
- Board Support
- Metal Library



Freedom U SDK

Linux Software Development

- Yocto/OpenEmbedded
- Bootloaders
- Board Support
- Device Tree Binary
- Linux Kernel Images
- Disk Images





5G Base Station

- OpenRAN
- Vectors
- Server OS



Intelligent Edge

- On-Device Decision
- Low Power
- ML Frameworks



Storage

- Data & On-Device Compute
- Performance
- Control & Compute



Automotive

- ADAS & Driver Aids
- Functional Safety
- Real-Time OS

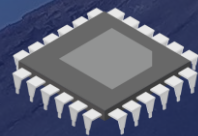
RISC-V®

Capture the Core of Leading Compute Platforms



Mobile

- Gaming & Experience
- Best Perf/W
- Mobile OS



Embedded

- Power & Area
- Security
- Developer Tools



Networking

- Data Bandwidth
- Throughput
- DPDK S/W



High Performance Compute

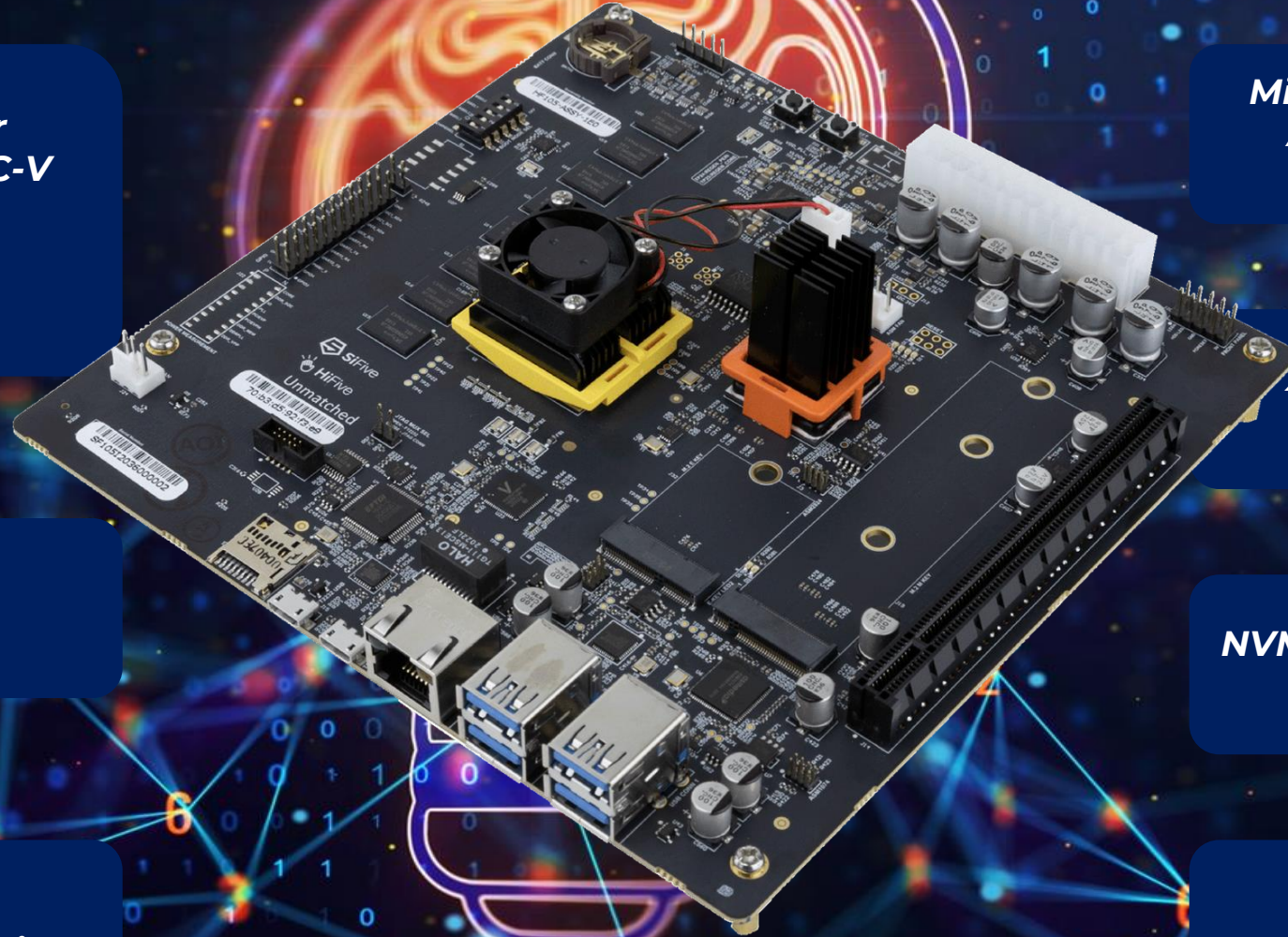
- Data & Analysis
- Scalable Throughput
- Virtualization



SiFive HiFive Unmatched

SiFive FU740 Processor
SiFive 7-Series 64-bit RISC-V
Core Complex
4x U74-MC & 1 S7 Core
2MB L2 Cache

Mini-ITX PC Form Factor with
ATX 24-pin Power Supply
Connector



X16 PCIe® Expansion Slot
(PCIe Gen 3 x8)

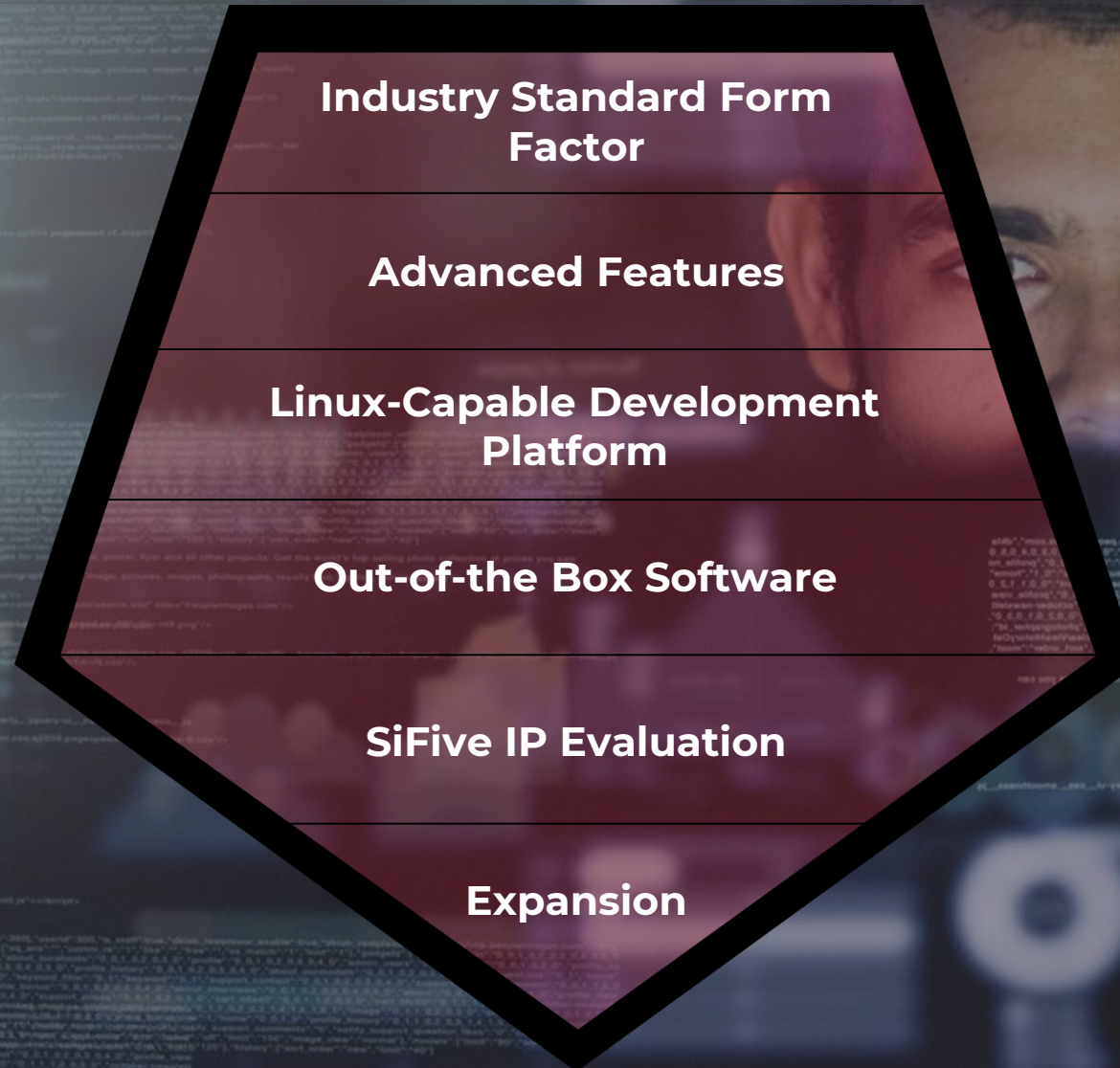
8GB DDR4 Memory
32 MB SPI FLASH

NVME M.2 2280 (PCIe® Gen 3 x4)
MicroSD Card Slot

4x USB 3.2 Gen 1 Ports
MicroUSB Console Connection

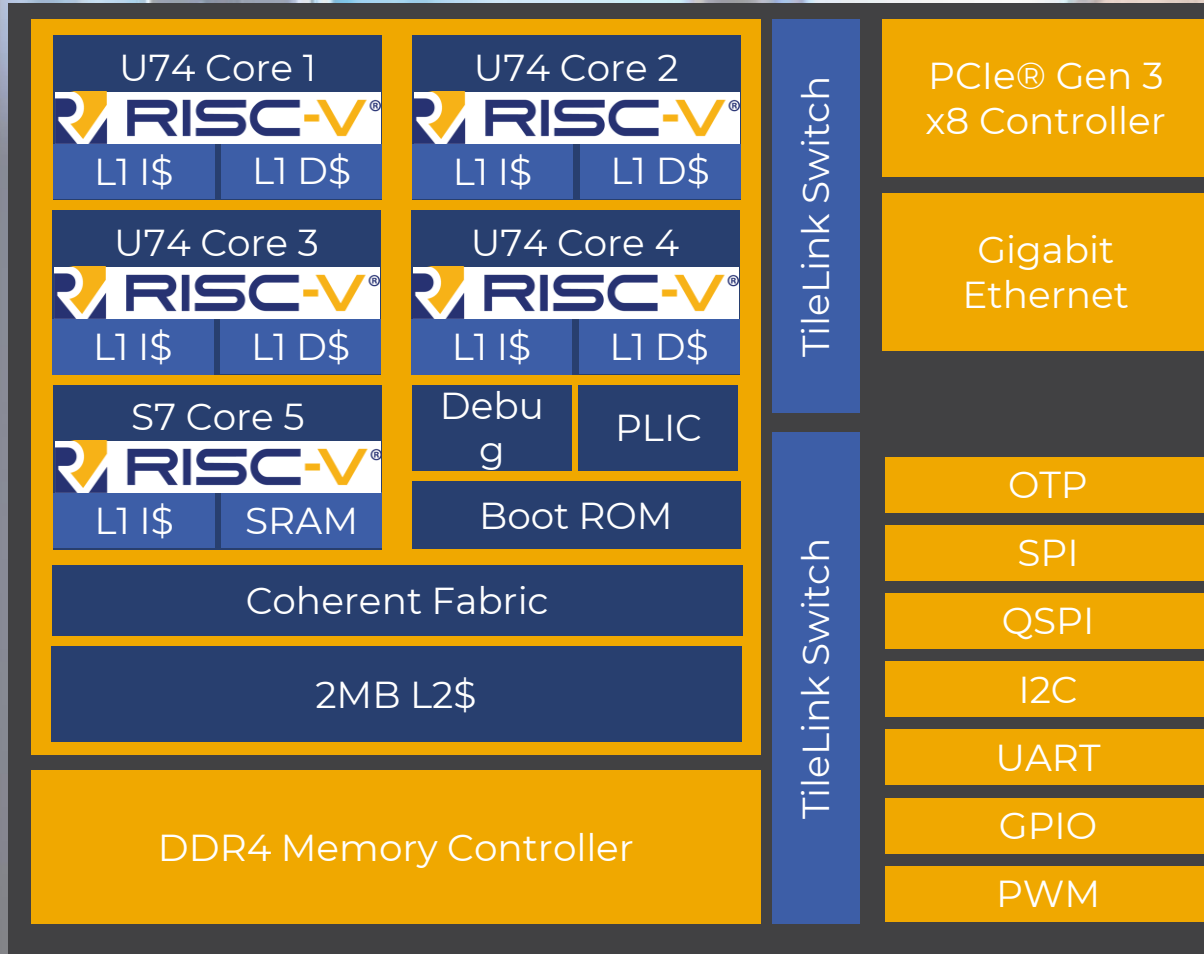
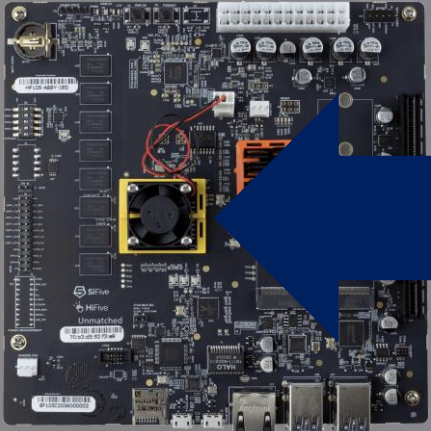
Gigabit Ethernet
M.2 Key E Wi-Fi/Bluetooth

What Do Developers Want?





SiFive FU740 SoC



SiFive 7-Series Multi-Core Application Processor

- 64-Bit 8-Stage Dual-Issue, Superscalar RISC-V Core

Application Core Complex

- 4x SiFive U74 Cores
- RV64GC (RV64IMAFDC)
- 32KB I\$ Per Core
- 32KB D\$ Per Core

Single Embedded S7 Core

- RV64IMAC
- 16KB I\$
- 8KB DTIM

2MB Coherent Banked L2\$

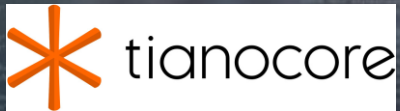
Integrated PCIe® Gen 3, DDR4, & I/O

Key RISC-V Open-Source Projects

UEFI

EDK2 Upstreamed
September 2020

GitHub:
[/riscv/riscv-uefi-edk2-docs](#)



V8

Google Javascript Engine
TurboFan Compiler
The Ignition Engine
WebAssembly Compile

RV64IMAFD Support

GitHub:
[/v8-riscv/v8/wiki/Project-Roadmap](#)
[v8-riscv/v8/wiki/Work-groups](#)



Java

Initial porting work done on
OMR/OpenJ9/OpenJDK

GitHub:
[/AdoptOpenJDK/openjdk-build](#)

Binaries:
<https://ci.adoptopenjdk.net/job/jdk11-linux-riscv-openj9-build/>



AOSP

Looking for Partners!
Porting begun by ISCAS –
PLCT Lab

GitHub:
[/aosp-riscv/](#)
[/guoyinchen/riscv-aosp-soong/tree/riscv_android-10.0.0](#)




Build The RISC-V Ecosystem Together

Free & Open Architecture
Commercial Innovation
Community Contribution

 RISC-V®

 SiFive


GitHub



Thank You



SIFIVE.COM

FOOTNOTES

1. A New Golden Age for Computer Architecture, By John L. Hennessy, David A. Patterson, Communications of the ACM, February 2019, Vol. 62 No. 2, Pages 48-60
<https://cacm.acm.org/magazines/2019/2/234352-a-new-golden-age-for-computer-architecture/fulltext>
2. Semico Forecasts Strong Growth for RISC-V, <https://riscv.org/announcements/2019/11/9679/>
3. Intel and Softbank Beware. Open Source Is Coming to the Chip Business, <https://www.bloomberg.com/news/articles/2020-01-22/open-source-transformed-software-the-chip-industry-is-next>

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