

PolarFire SoC how we got here.



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



SMART | CONNECTED | SECURE

Tim Morin

11/5/2020

Agenda

- **Introducing PolarFire SoC**
- **The Icicle Kit**
- **Development Tools**
- **MI-V Ecosystem**

Introducing PolarFire SoC

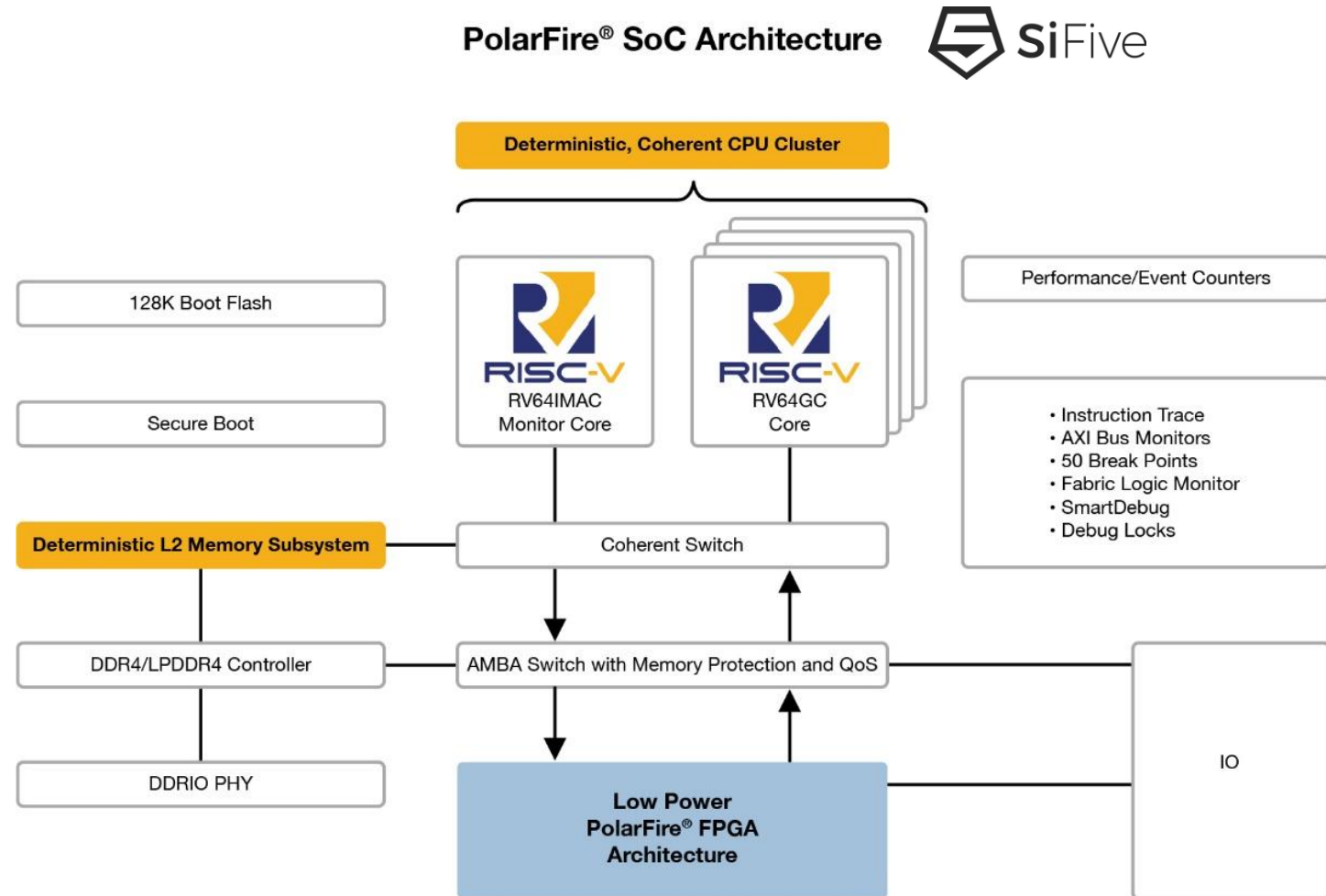
PolarFire SoC - RISC-V Enabled Innovation Platform

Highly Differentiated

- Low power, high performance SoC
 - Thermal efficiency
 - Solutions ~50% power of competition
- Unique AMP mode for mixed real-time and Linux operation
- Defense grade security with Spectre/Meltdown immunity
- Exceptional reliability (SEU Configuration Immune)
- Smallest form factors

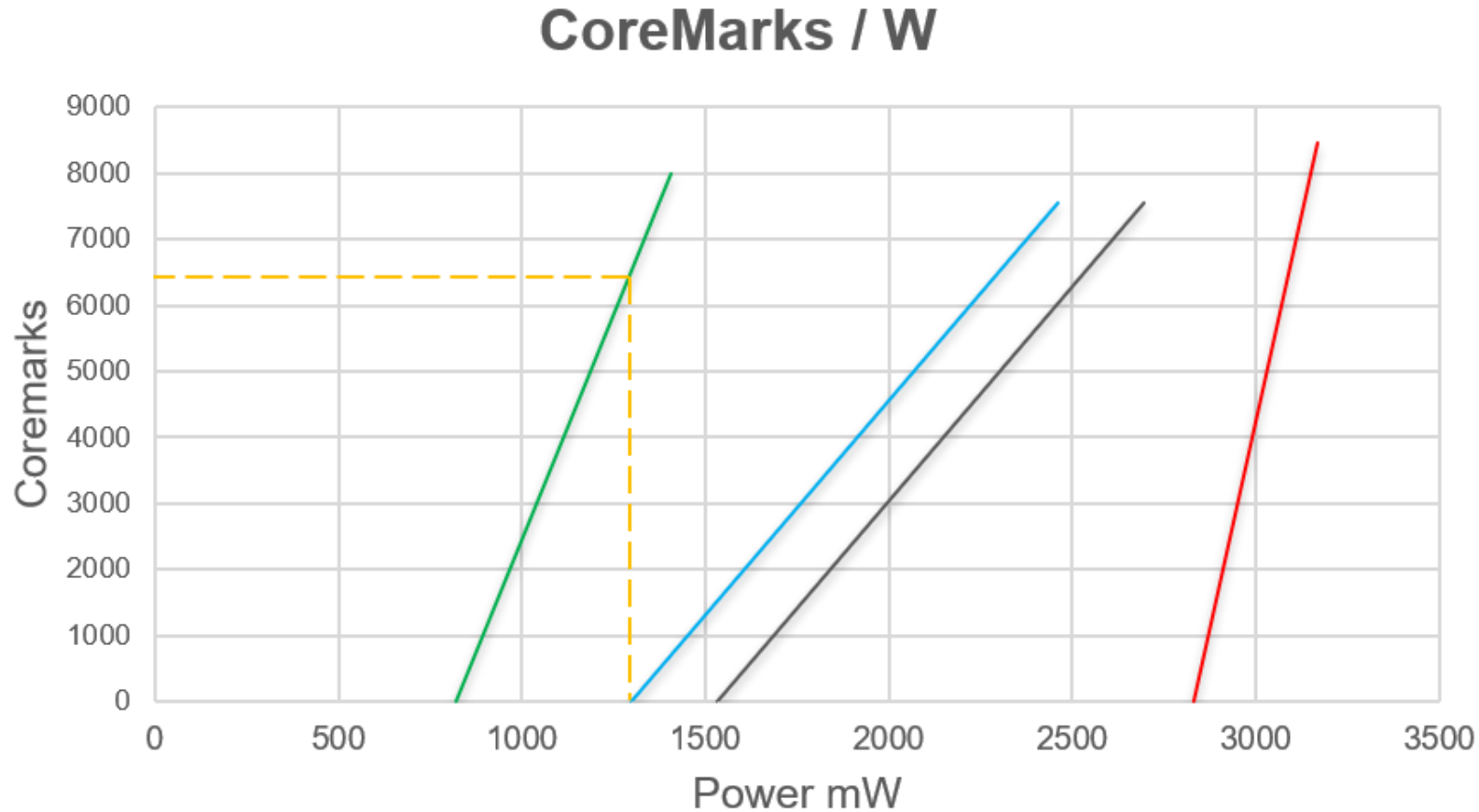
Freedom to Innovate in

- Linux and Real-Time
- Thermal and Power Constrained Systems
- Securely Connected IoT Systems
- Mixed Criticality Systems



Open. Lowest Power. Programmable RISC-V Solutions.

Market Leading Power efficiency



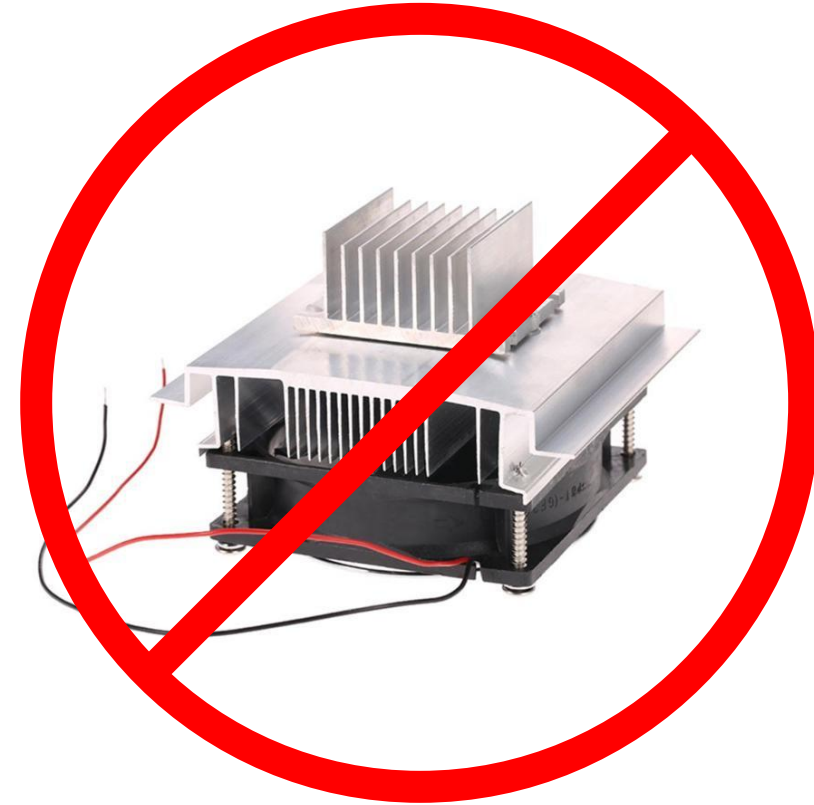
SoC FPGAs

— MPFS095T

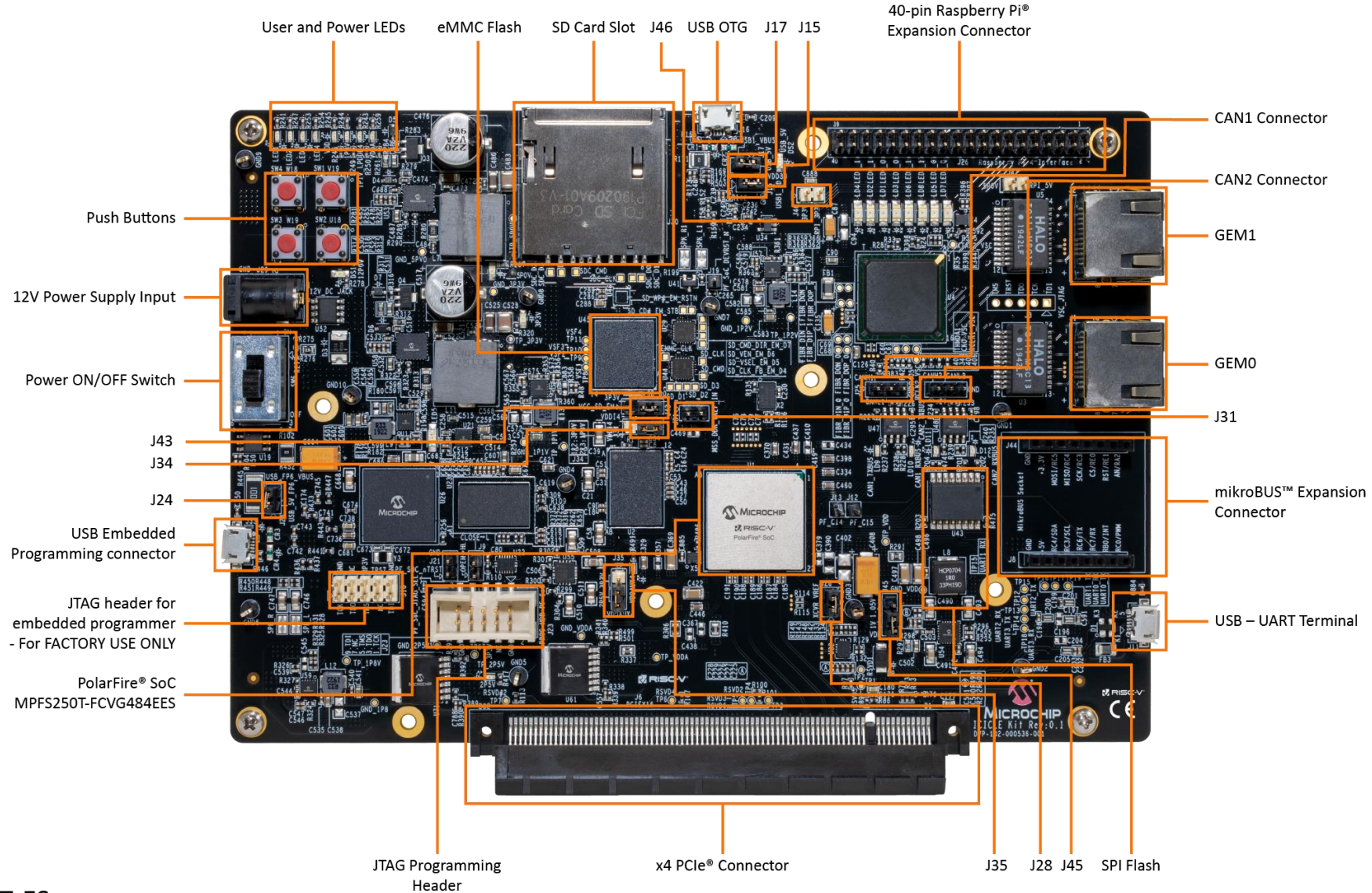
— 2xCortex A9

— 2xCortex A9

— 2xCortex A53



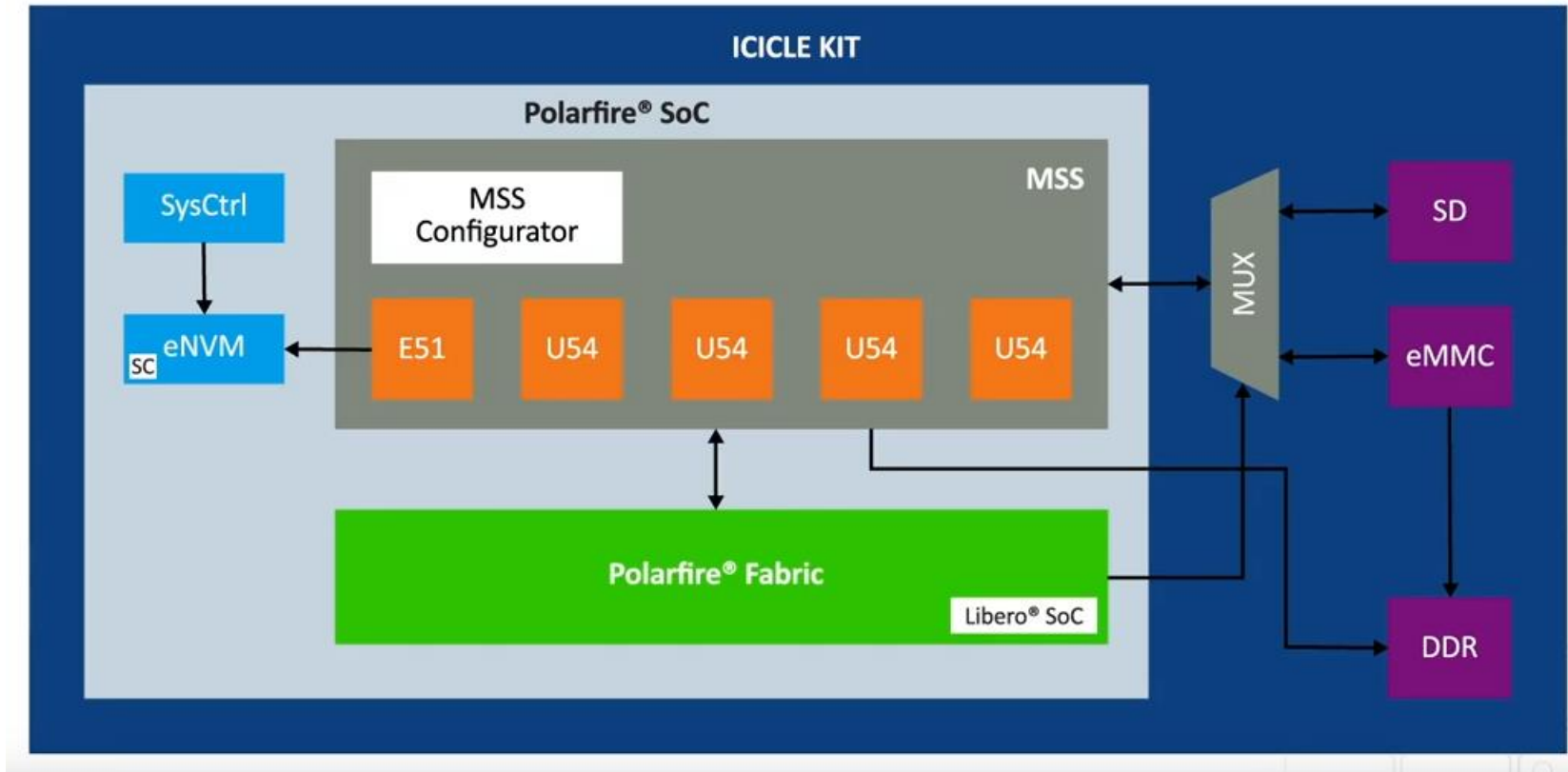
PolarFire SoC Icicle Kit



MPFS-ICICLE-KIT-ES
MSRP \$489 – Shipping

The Boot Process

- eNVM contains Start up code - called Hart Software Services



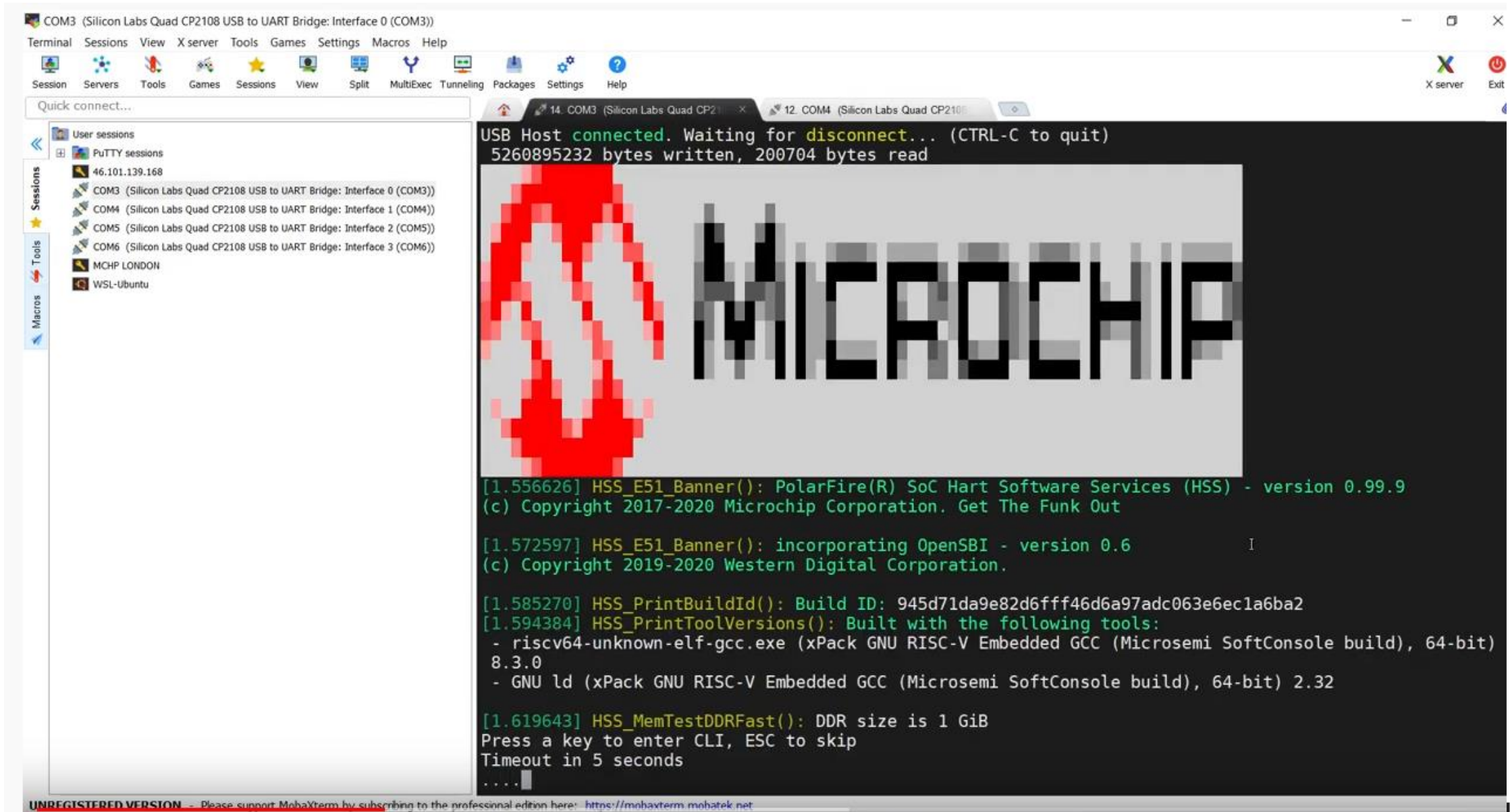
Cable Connections

- Com port 0 : Hart Software Services messages
- Com port 1 : Linux Boot messages



115.2 k baud
No flow control
No parity

Com Port 0 = Hart Software Services Boot up



The screenshot shows a MobaXterm terminal window with the title "COM3 (Silicon Labs Quad CP2108 USB to UART Bridge: Interface 0 (COM3))". The terminal output displays the following information:

```
USB Host connected. Waiting for disconnect... (CTRL-C to quit)
5260895232 bytes written, 200704 bytes read

[1.556626] HSS_E51_Banner(): PolarFire(R) SoC Hart Software Services (HSS) - version 0.99.9
(c) Copyright 2017-2020 Microchip Corporation. Get The Funk Out

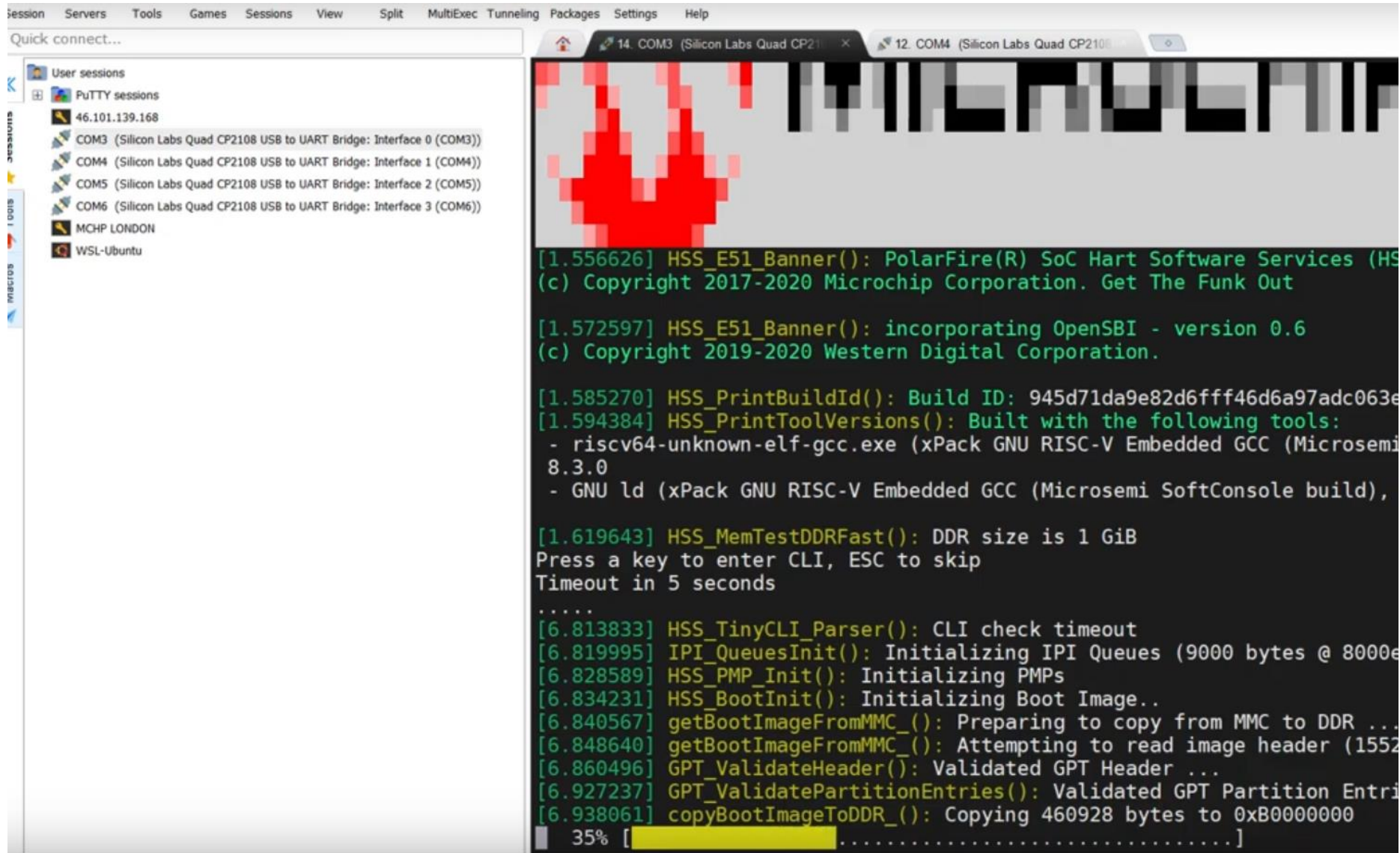
[1.572597] HSS_E51_Banner(): incorporating OpenSBI - version 0.6
(c) Copyright 2019-2020 Western Digital Corporation.

[1.585270] HSS_PrintBuildId(): Build ID: 945d71da9e82d6fff46d6a97adc063e6ec1a6ba2
[1.594384] HSS_PrintToolVersions(): Built with the following tools:
- riscv64-unknown-elf-gcc.exe (xPack GNU RISC-V Embedded GCC (Microsemi SoftConsole build), 64-bit)
8.3.0
- GNU ld (xPack GNU RISC-V Embedded GCC (Microsemi SoftConsole build), 64-bit) 2.32

[1.619643] HSS_MemTestDDRFast(): DDR size is 1 GiB
Press a key to enter CLI, ESC to skip
Timeout in 5 seconds
....
```

The output includes a red Microchip logo, the HSS version (0.99.9), OpenSBI version (0.6), build ID (945d71da9e82d6fff46d6a97adc063e6ec1a6ba2), tool versions (GCC 8.3.0 and GNU ld 2.32), and DDR size (1 GiB). The terminal also shows a "UNREGISTERED VERSION" notice at the bottom.

Copy U-boot from eMMC to DDR



```
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
User sessions
  PUTTY sessions
    46.101.139.168
    COM3 (Silicon Labs Quad CP2108 USB to UART Bridge: Interface 0 (COM3))
    COM4 (Silicon Labs Quad CP2108 USB to UART Bridge: Interface 1 (COM4))
    COM5 (Silicon Labs Quad CP2108 USB to UART Bridge: Interface 2 (COM5))
    COM6 (Silicon Labs Quad CP2108 USB to UART Bridge: Interface 3 (COM6))
  MCHP LONDON
  WSL-Ubuntu

[1.556626] HSS_E51_Banner(): PolarFire(R) SoC Hart Software Services (HSS)
(c) Copyright 2017-2020 Microchip Corporation. Get The Funk Out

[1.572597] HSS_E51_Banner(): incorporating OpenSBI - version 0.6
(c) Copyright 2019-2020 Western Digital Corporation.

[1.585270] HSS_PrintBuildId(): Build ID: 945d71da9e82d6fff46d6a97adc063e
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8.3.0
- GNU ld (xPack GNU RISC-V Embedded GCC (Microsemi SoftConsole build),

[1.619643] HSS_MemTestDDRFast(): DDR size is 1 GiB
Press a key to enter CLI, ESC to skip
Timeout in 5 seconds
.....
[6.813833] HSS_TinyCLI_Parser(): CLI check timeout
[6.819995] IPI_QueueInit(): Initializing IPI Queues (9000 bytes @ 8000e
[6.828589] HSS_PMP_Init(): Initializing PMPs
[6.834231] HSS_BootInit(): Initializing Boot Image..
[6.840567] getBootImageFromMMC_(): Preparing to copy from MMC to DDR ...
[6.848640] getBootImageFromMMC_(): Attempting to read image header (1552
[6.860496] GPT_ValidateHeader(): Validated GPT Header ...
[6.927237] GPT_ValidatePartitionEntries(): Validated GPT Partition Entr
[6.938061] copyBootImageToDDR_(): Copying 460928 bytes to 0xB0000000
35% [.....]
```

U boot running

```
14. COM3 (Silicon Labs Quad CP2108 USB to UART Bridge: Interface 0 (COM3))
[11.120667] HSS_Boot_PMPSetupHandler(): Hart1 setup complete
HSS_OpenSBI_Setup(): MTVEC switching from 20220230 to 20220100

U-Boot 2020.01 (Sep 30 2020 - 21:35:05 +0000)

DRAM: 1 GiB
error setting mac-address property
MMC: sdhc@20008000: 0
In: serial@20100000
Out: serial@20100000
Err: serial@20100000
Net:
Warning: ethernet@20112000 using MAC address from ROM
eth0: ethernet@20112000
Hit any key to stop autoboot: 0
switch to partitions #0, OK
mmc0(part 0) is current device
```

Un compressing Linux Kernel

```
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
Out: serial@20100000
Err: serial@20100000
Net:
Warning: ethernet@20112000 using MAC address from ROM
eth0: ethernet@20112000
Hit any key to stop autoboot: 0
switch to partitions #0, OK
mmc0(part 0) is current device
Scanning mmc 0:1...
Found U-Boot script /boot.scr.uimg
1096 bytes read in 12 ms (88.9 KiB/s)
## Executing script at 88100000
3586352 bytes read in 313 ms (10.9 MiB/s)
## Copying 'fdt@microchip_icle-kit-es-a000-microchip.dtb' subimage from FIT image at 88300000
sha256+ Loading part 253 ... OK
## Loading kernel from FIT Image at 88300000 ...
Using 'conf@microchip_icle-kit-es-a000-microchip.dtb' configuration
Trying 'kernel@1' kernel subimage
Description: Linux kernel
Type: Kernel Image
Compression: gzip compressed
Data Start: 0x883000fc
Data Size: 3574554 Bytes = 3.4 MiB
Architecture: RISC-V
OS: Linux
Load Address: 0x80200000
Entry Point: 0x80200000
Hash algo: sha256
Hash value: e63bddd6526c3fff234ad855b9fb73d44f2506e3c268b8340b8970589160a6d0
Verifying Hash Integrity ... sha256+ OK
## Flattened Device Tree blob at 88000000
Booting using the fdt blob at 0x88000000
Uncompressing Kernel Image
```

UNREGISTERED VERSION - Please support MahaYterm by subscribing to the professional edition here: <https://mohayterm.mohatek.net>

Linux booted


```
Quick connect...
[ OK ] Started System Logging Service.
[ OK ] Starting Login Service...
[ OK ] Started IPv6 Packet Filtering Framework.
[ OK ] Started IPv4 Packet Filtering Framework.
[ OK ] Reached target Network (Pre).
[ OK ] Starting Network Service...
[ OK ] Started Network Service.
[ OK ] Starting Network Name Resolution...
[ OK ] Started Login Service.
[ OK ] Started Network Name Resolution.
[ OK ] Reached target Network.
[ OK ] Reached target Host and Network Name Lookups.
[ OK ] Started Collectd.
[ OK ] Started NFS status monitor for NFSv2/3 locking..
[ OK ] Started Respond to IPv6 Node Information Queries.
[ OK ] Started Network Router Discovery Daemon.
[ OK ] Starting Permit User Sessions...
[ OK ] Started Load/Save Random Seed.
[ OK ] Started Permit User Sessions.
[ OK ] Started Getty on tty1.
[ OK ] Started Serial Getty on ttyS0.
[ OK ] Reached target Login Prompts.
[ OK ] Reached target Multi-User System.
[ OK ] Starting Update UTMP about System Runlevel Changes...
[ OK ] Started Update UTMP about System Runlevel Changes.


OpenEmbedded nodistro.0 icicle-kit-es ttyS0


icicle-kit-es login: root
root@icicle-kit-es:~# uname -a
Linux icicle-kit-es 5.6.16 #1 SMP Wed Sep 30 20:28:26 UTC 2020 riscv64 riscv64 riscv64 GNU/Linux
root@icicle-kit-es:~#
```


PolarFire Soc GitHub

Pinned repositories

 [polarfire-soc-bare-metal-library](#)
Bare metal embedded software drivers and examples for PolarFire SoC
● C ☆ 10 🍴 3

 [meta-polarfire-soc-yocto-bsp](#)
PolarFire SoC yocto Board Support Package
● BitBake ☆ 6 🍴 8

 [polarfire-soc-buildroot-sdk](#)
PolarFire SoC Buildroot Software Development Kit
● Makefile ☆ 8 🍴 2

 [polarfire-soc-documentation](#)
PolarFire SoC Documentation
☆ 7 🍴 1

🔍 Find a repository... Type: All ▾ Language: All ▾

polarfire-soc-bare-metal-library
Bare metal embedded software drivers and examples for PolarFire SoC
● C 🍴 3 ☆ 10 ⓘ 0 🛠️ 1 Updated 29 minutes ago



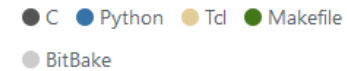
hart-software-services
PolarFire SoC hart software services
● C 🍴 8 ☆ 6 ⓘ 1 🛠️ 0 Updated 36 minutes ago



polarfire-soc-linux-examples
● JavaScript 🍴 0 ☆ 1 ⓘ 0 🛠️ 0 Updated 1 hour ago



Top languages



People >

This organization has no public members. You must be a member to see who's a part of this organization.

PolarFire SoC on the RISC-V exchange

- New website to bring everything together

RISC-V Exchange

The RISC-V Exchange provides a window into work that people are doing in hardware and software. This section of our website will grow as hardware and software projects are added.

- **Available Boards** – see below
- **Available Cores & SoCs**
- **Available Software**
- **Available Books**

RISC-V Exchange: Available

Site Feedback

Discussion about this site, its organization, how it works, and how we can improve it.

PolarFire SoC Icicle Kit

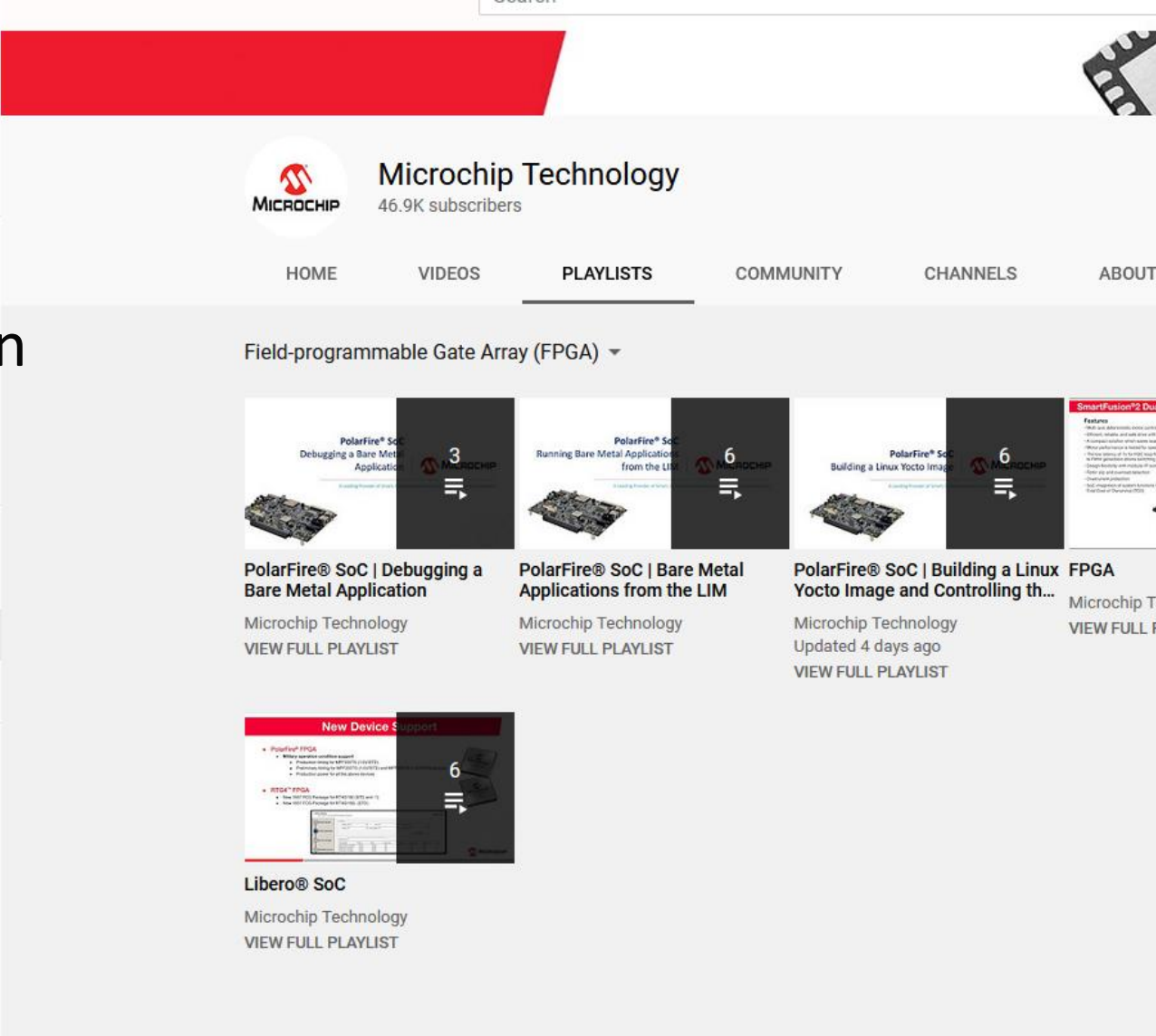


This is the place to discuss the PolarFire SoC icicle Kit. This category will be moderated by Microchip Engineers to help you on your way. Thanks for showing up and sharing with us.

- Yocto Project
- Buildroot Project
- PolarFire SoC Bare Metal Projects
- Restoring to Factory Defaults
- Hart Software Services
- General

PolarFire SoC on YouTube

- Playlists of 3-5 minute how-to videos
 - 6 playlists by end of November
 - Debugging a bare metal application
 - Out of the box
 - Using the LIM
 - Using DDR
 - Adding a peripheral to the fabric
 - Build Linux using Yocto
 - Adding a peripheral to the fabric



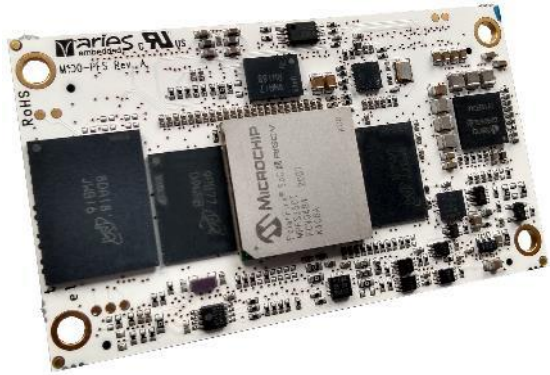
The screenshot shows the YouTube channel page for Microchip Technology, which has 46.9K subscribers. The navigation menu includes HOME, VIDEOS, PLAYLISTS (selected), COMMUNITY, CHANNELS, and ABOUT. The main content area is titled "Field-programmable Gate Array (FPGA)" and displays several playlists:

- PolarFire® SoC | Debugging a Bare Metal Application** (3 videos)
- PolarFire® SoC | Bare Metal Applications from the LIM** (6 videos)
- PolarFire® SoC | Building a Linux Yocto Image and Controlling th...** (6 videos)
- FPGA** (Microchip Technology)
- Libero® SoC** (Microchip Technology)

Each playlist card includes a thumbnail image, the title, the channel name "Microchip Technology", and a "VIEW FULL PLAYLIST" link. The "Building a Linux Yocto Image" playlist is noted as being updated 4 days ago.

System On Modules

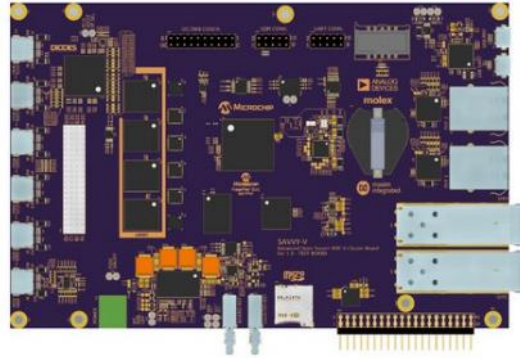
Coming Soon



**Aries
Embedded**

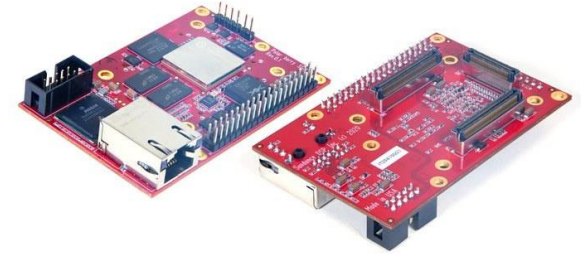


Trenz



<https://www.crowdsupply.com/ali-uzel/savvy-v>

Part of
Microchip
Get Launched



Sundance DSP
<https://www.crowdsupply.com/sundance-dsp/polarberry>



Digitalcore

Mi-V Ecosystem Partners



Where to buy the Icycle Kit?

- **CrowdSupply**
 - <https://www.crowdsupply.com/microchip/polarfire-soc-icycle-kit>
- **Mouser**
 - <https://www.mouser.com/new/microchip/microchip-polarfire-soc-icycle-kit/>
- **Digi-key**
 - <https://www.digikey.com/en/product-highlight/m/microchip-technology/mpfs-icycle-kit-es--polarfire-soc-fpga-icycle-kit>
- **Arrow**
 - <https://www.arrow.com/en/products/mpfs-icycle-kit-es/microsemi>
- **Avnet**
 - <https://www.avnet.com/wps/portal/silica/products/new-products/npi/2020/microchip-polarfire-soc/>

PolarFire SoC – Best in Class!

- **PolarFire FPGA Award Winning Features**

- 30-50% Lower power
- Defense grade security
- Exceptional reliability
- Smallest, lowest power, secure form factors – 11x11, 16x16, 19x19

- **Plus Microprocessor Subsystem**

- Linux and real time in a deterministic, coherent CPU cluster
- 30-50% Lower power
- Defense grade secure boot
- Spectre/Meltdown immune
- SECDED on all memories



Important Links

- **PolarFire SoC:** www.microsemi.com/polarfiresoc
- **Solutions:** www.microsemi.com/polarfiresoc#getting-started
- **Icicle Kit:** www.microsemi.com/icicle
- **Software:**
 - **MSS Configurator:** <https://www.microsemi.com/product-directory/soc-design-tools/5587-pfsoc-mss-configurator-tool>
 - **Libero SoC:** www.microsemi.com/liberosoc
 - **SoftConsole:** www.microsemi.com/softconsole
- **Marketing Contact:** polarfiresoc@microchip.com
- **Tech support:** <https://soc.microsemi.com/Portal/Default.aspx>
- **Tech Videos:** https://www.youtube.com/c/MicrochipTech/playlists?view=50&sort=dd&shelf_id=4

Thank You!

PolarFire SoC Family

1st device

	Features	MPFS025T	MPFS095T	MPFS160T	MPFS250T	MPFS460T
FPGA Fabric	K Logic Elements (4LUT + DFF)	23	93	161	254	461
	Math Blocks (18x18 MACC)	68	292	498	784	1420
	LSRAM Blocks (20k bit)	84	308	520	812	1460
	uSRAM Blocks (64x12)	204	876	1494	2352	4260
	Total RAM Mbits	1.8	6.7	11.3	17.6	31.6
	uPROM Kbits	194	387	415	470	553
	User DLL's/PLL's	8 each	8 each	8 each	8 each	8 each
High Speed IO	250 Mbps to 12.5 Gbps SERDES Lanes	4	4	8	16	20
	PCIe Gen2 End Points/Root Ports	2	2	2	2	2
Total FPGA IO	HSIO+GPIO	108	276	312	372	468
Total MSS IO	MSS IO	136	136	136	136	136
MSS DDR DB	MSS DDR Data Bus	16	32	32	32	32
Packaging Commerical & Industrial RoHS	Type/Size/Pitch	MSS IO / HSIO / GPIO / XCVRs				
	FCSG325 (11x11, 11x14.5*, 0.5 mm)	102 / 32 / 48 / 2	102 / 32 / 48 / 2			
	FCSG536 (16x16, 0.5 mm)		136 / 60 / 108 / 4	136 / 60 / 108 / 4	136 / 60 / 108 / 4	
	FCVG484 (19x19, 0.8 mm)	136 / 60 / 48 / 4	136 / 60 / 84 / 4	136 / 60 / 84 / 4	136 / 60 / 84 / 4	
	FCVG784 (23x23, 0.8 mm)		136 / 144 / 132 / 4	136 / 144 / 168 / 8	136 / 144 / 180 / 8	
	FCG1152 (35x35, 1.0 mm)				136 / 144 / 228 / 16	136 / 180 / 288 / 20

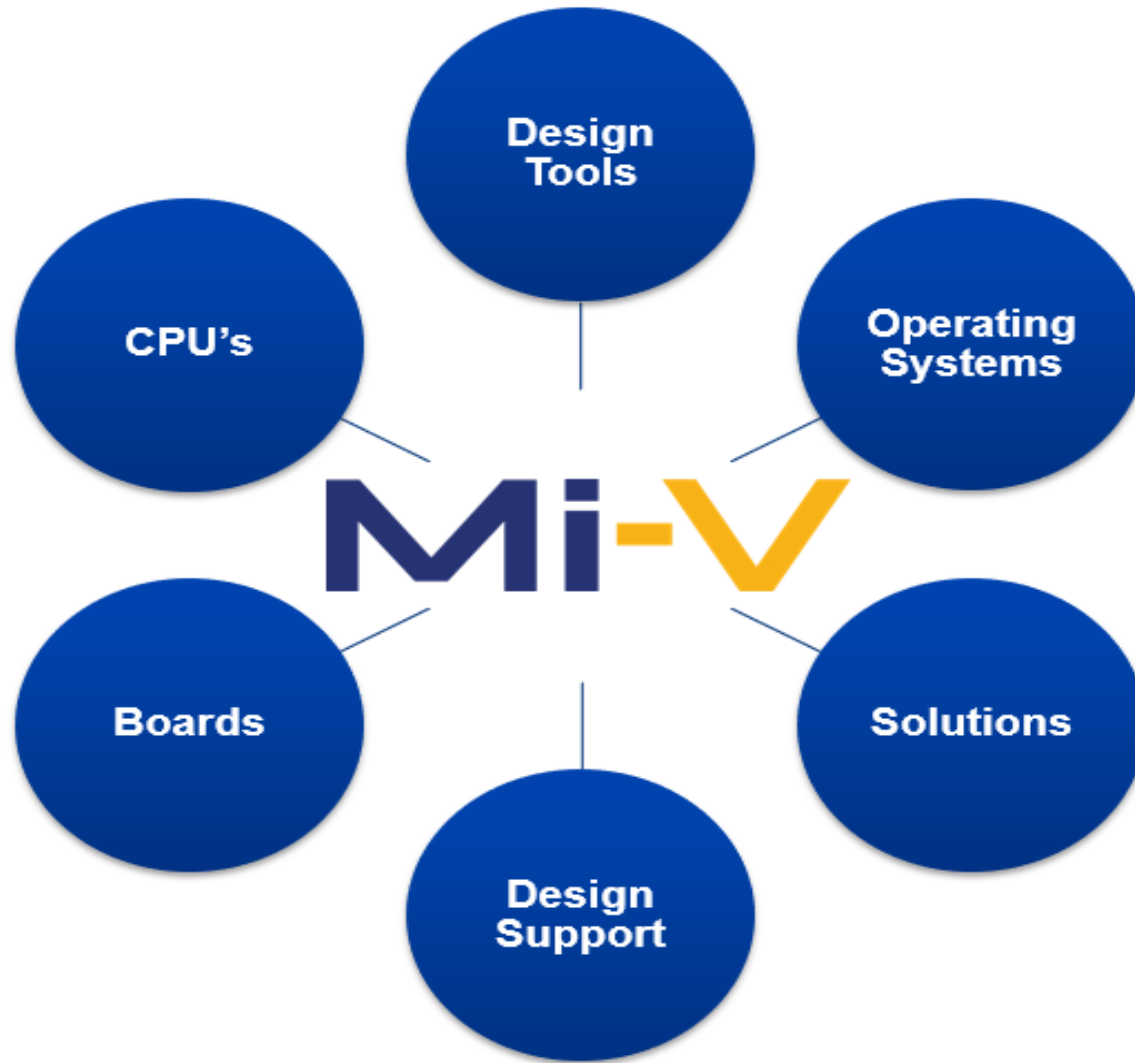
Extended Commercial (0°C-100°C) and Industrial (-40°C-100°C) Temperature Support for all Die Package Combinations - RoHS only

Additional Temp Grade: Military (-55°C-125°C) - Leaded packages only



Microchip's Mi-V Ecosystem

A Leading Provider of RISC-V Based Solutions



Microchip's Comprehensive Ecosystem to Support RISC-V Development

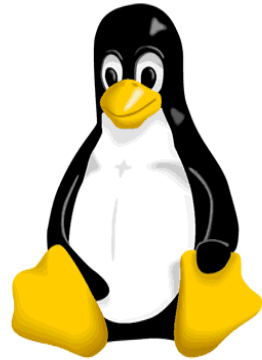
Mi-V Development Tools



C/C++ support
ADA support on demand

AdaCore

Mi-V Operating System Support



Linux

yocto
PROJECT



Covers 99% of the embedded rich OS market

Mi-V Commercial Real Time Operating Systems

Mentor[®]

A Siemens Business

BSP Available



BSP Available



Azure RTOS ThreadX

Micrium[®]
Embedded Software

Covers >90% of the market

Mi-V Open Source 64-bit RTOS

amazon



Security. Performance. Proof.

Mi-V Middleware Solutions



DOME™: Device Ownership
Management and Enrollment™



MultiZone Security for RISC-V



HEX-Five™

