Contributions

Open-Source IC & tapeouts

- → 1st *Open* Silicon Results

NIST Nanofabrication Accelerator

- → 1st *Open* Nanotechnology Platform
- → Cryogenic CMOS

Low-Power IC Design

- → ***Rapid*** Prototyping for Wearables

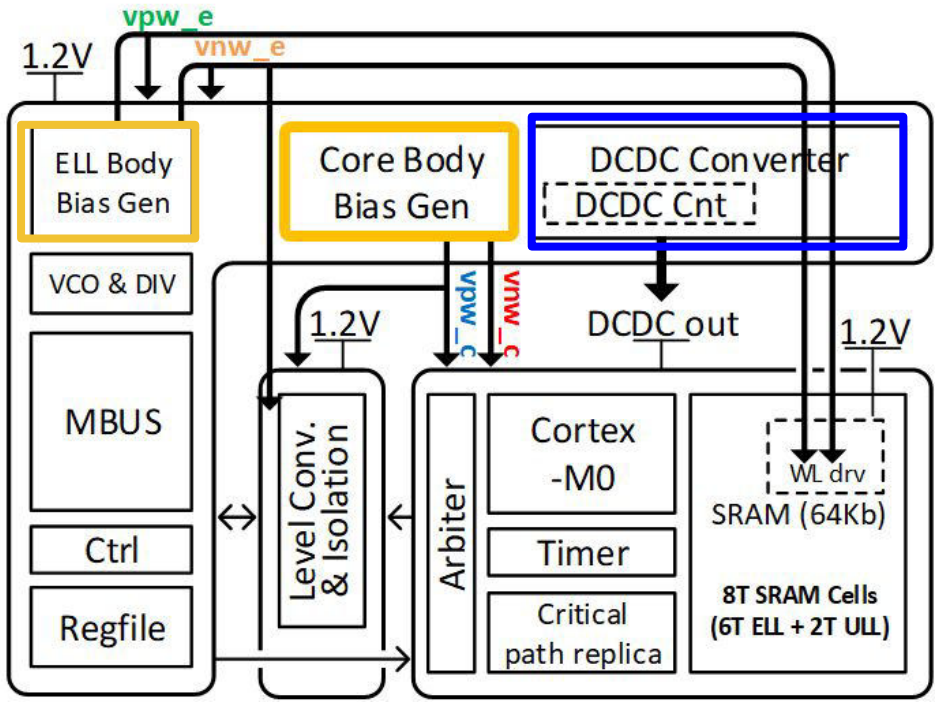
Hardware Security

- → 1st *Open* Root of Trust SoC

Low-Power SoC for Wearables

Previous Work

- Taped out in 55-nm DDC (Fujitsu) and published in ISSCC 2019 and JSSC 2020
- Power Domains
  - 1.2v
    - DC-DC converter
    - Charge Pumps
    - Clock generator
    - Controller
- DC-DC Output
  - Cortex-M0 Processor
  - 8KB SRAM

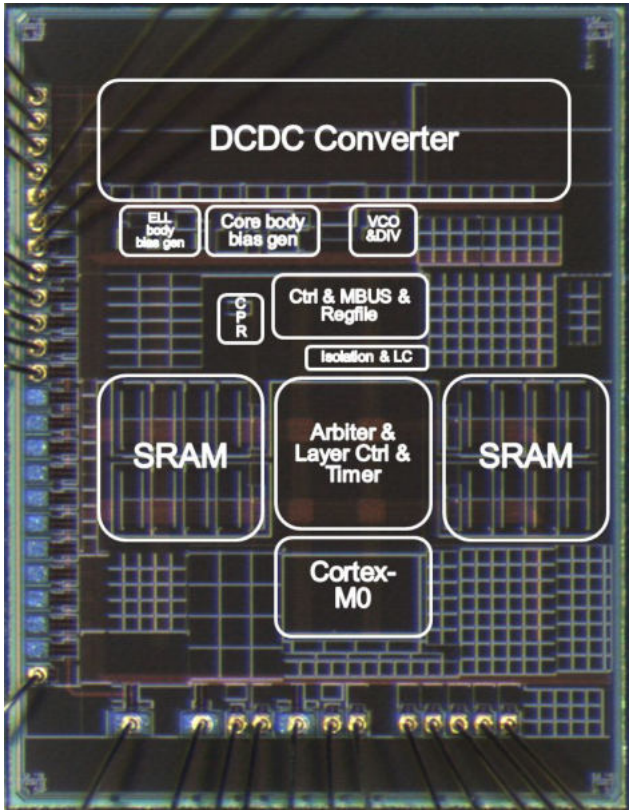


A 6.4 pJ/Cycle Self-Tuning Cortex-M0 IoT Processor Based on Leakage-Ratio Measurement for Energy-Optimal Operation Across Wide-Range PVT Variation

Low-Power SoC for Wearables

Previous Work

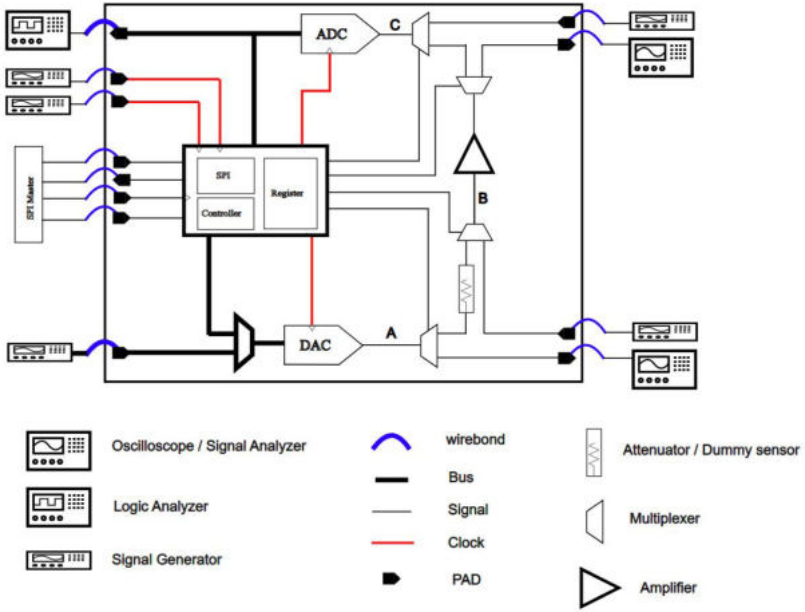
Technology	55nm DDC process
Die Size	1500μm x 1970μm
CPU	ARM Cortex M0
On-chip Memory	8KB SRAM
Supply Voltage	1.2V
Power Management Scheme	On-chip Closed-loop MEP-tracking
CPU & Memory Operating Voltage	0.48V ~ 0.75V
Clock Frequency	100kHz ~ 6MHz
Power	7.95μW @ TT, 25˚C ,1MHz
Minimum Energy Per Operation	6.4pJ/cycle @ 0.55V, 500kHz



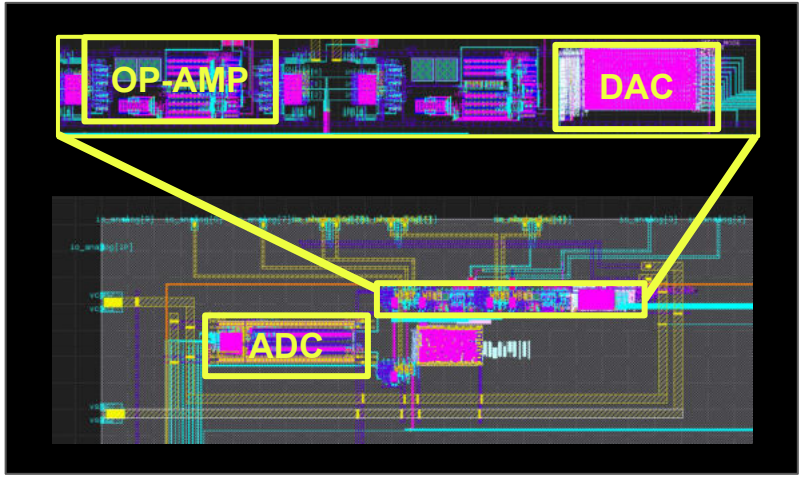
A 6.4 pJ/Cycle Self-Tuning Cortex-M0 IoT Processor Based on Leakage-Ratio Measurement for Energy-Optimal Operation Across Wide-Range PVT Variation

Low-Power SoC for Wearables

Rapid Prototyping - AFE



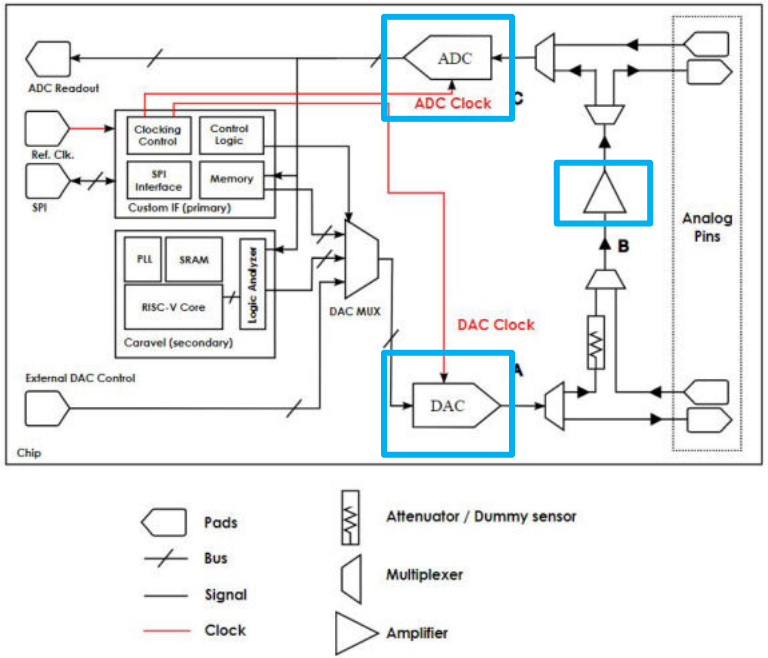
Sensor Test Harness in Skywater 130
Lab on a Chip Concept



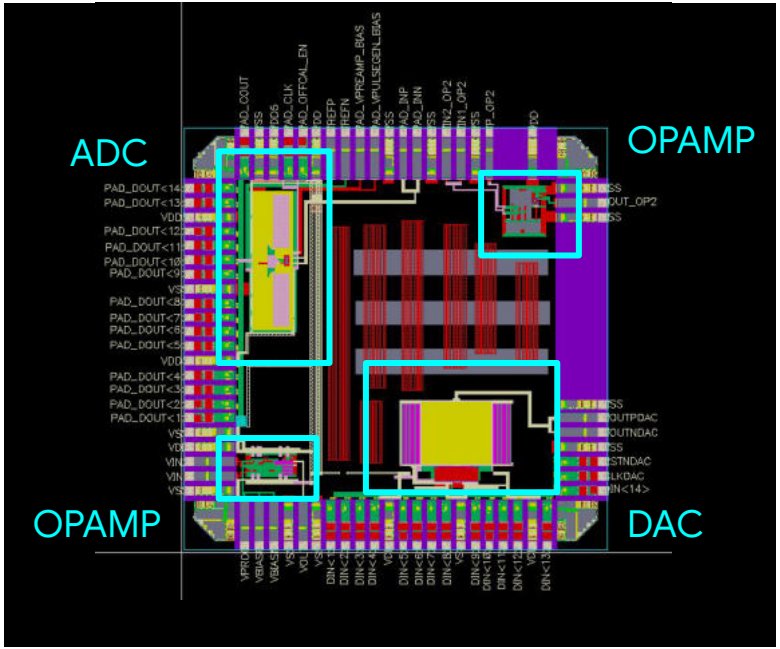
Test Harness for Rapid Prototyping

Low-Power SoC for Wearables

Rapid Prototyping - AFE



Test Harness in GF180



GF180 (Feb 2023)

On-Going Projects & Contributions

Open-Source IC & tapeouts

- ➔ 1st *Open* Silicon Results

NIST Nanofabrication Accelerator

- ➔ 1st *Open* Nanotechnology Platform
- ➔ Cryogenic CMOS

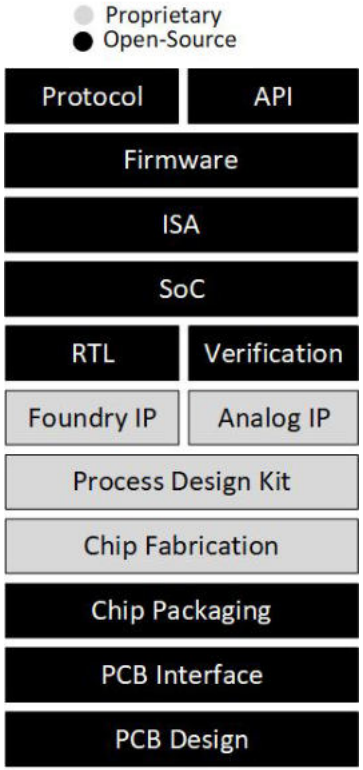
Low-Power IC Design

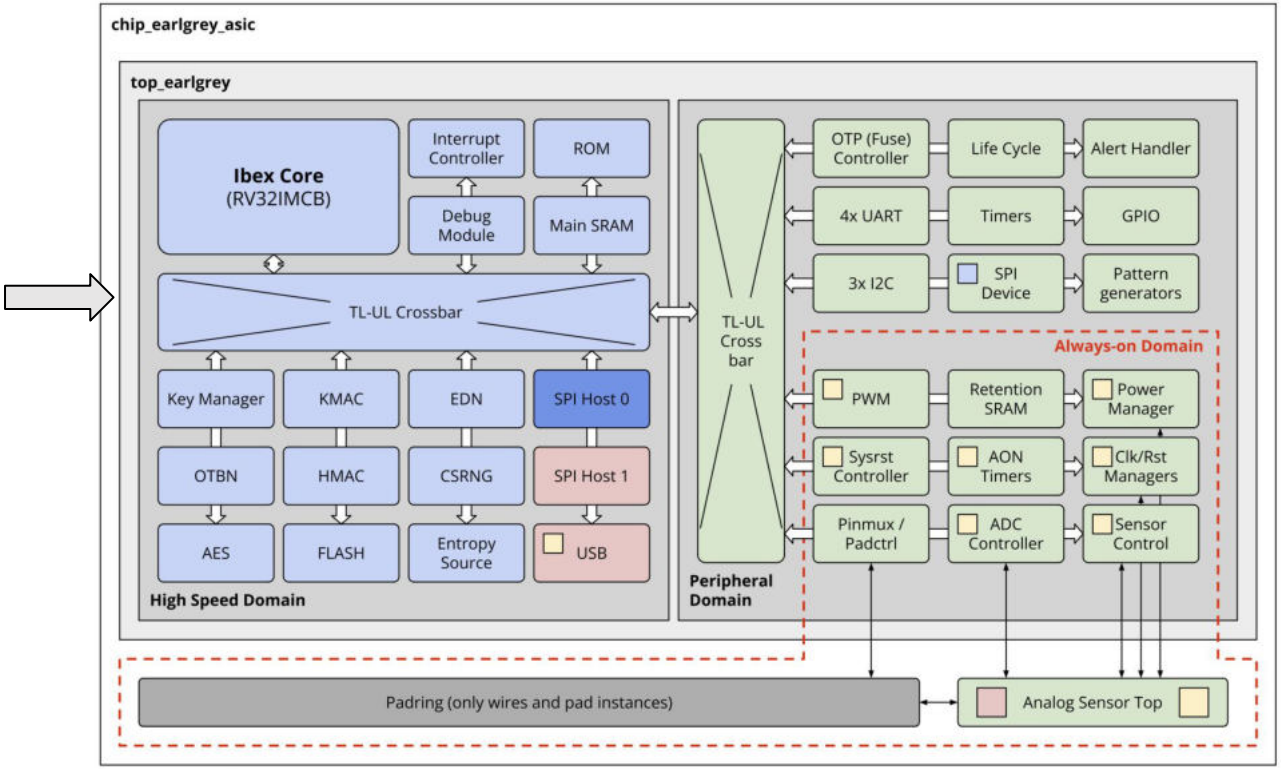
- ➔ *Rapid* Prototyping for Wearables

Hardware Security

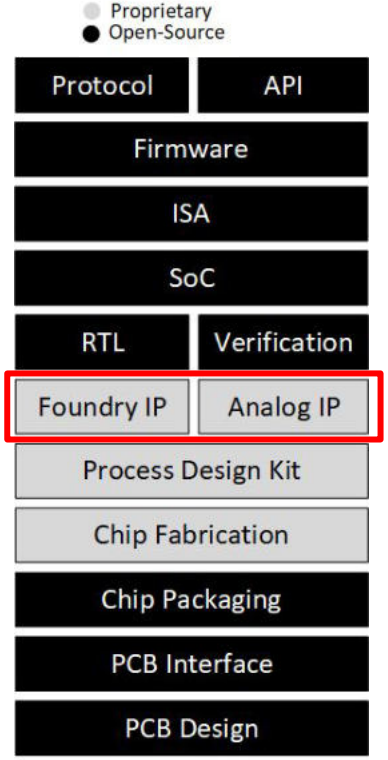
- ➔ 1st *Open* Root of Trust SoC

Open-Source Opentitan RoT

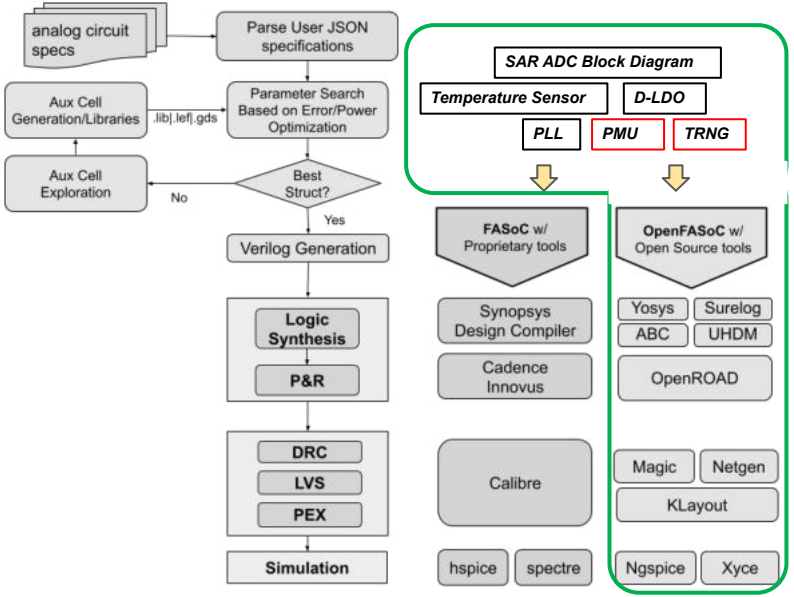




Open-Source Opentitan RoT
With *OpenFASOC* Generated Blocks



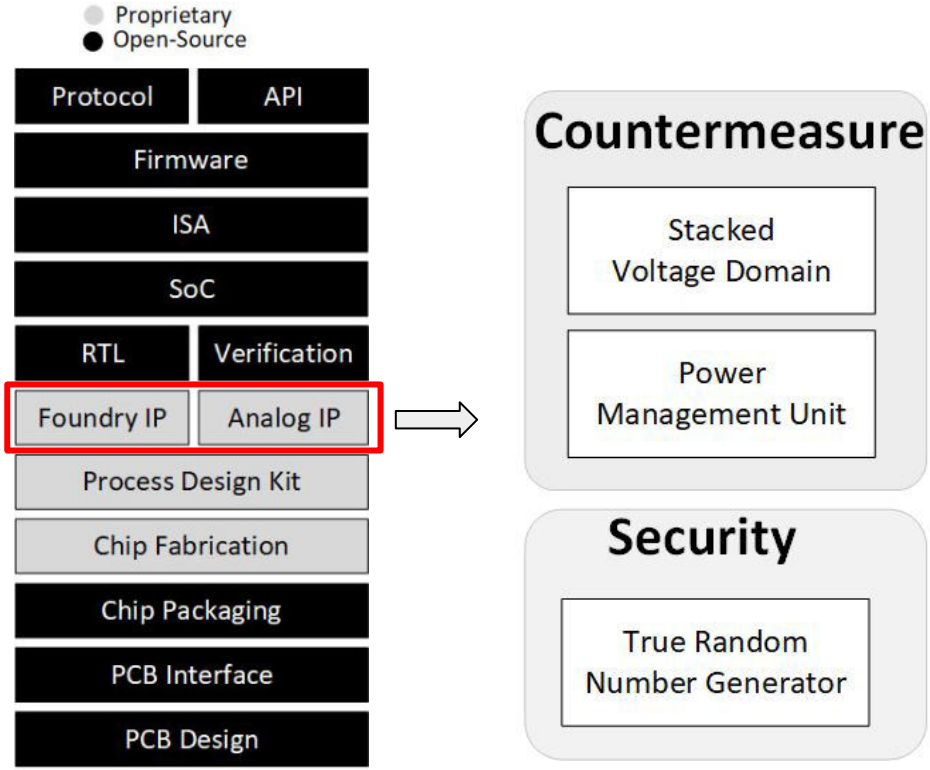
Source: https://docs.opentitan.org



OpenFASoC!

Automated **portable** analog

Proposed Techniques



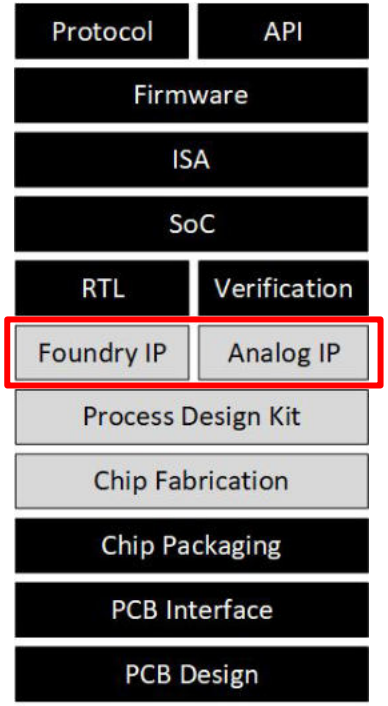
Source: https://docs.opentitan.org

- Power Side-Channel Attack Resistant Cryptographic AES SoC in Stacked Voltage Domain
- Secure Programmable PMU with noise injection
- ReRAM-based TRNG

Cryptographic AES SoC

Stacked Voltage Domain

Proprietary
Open-Source



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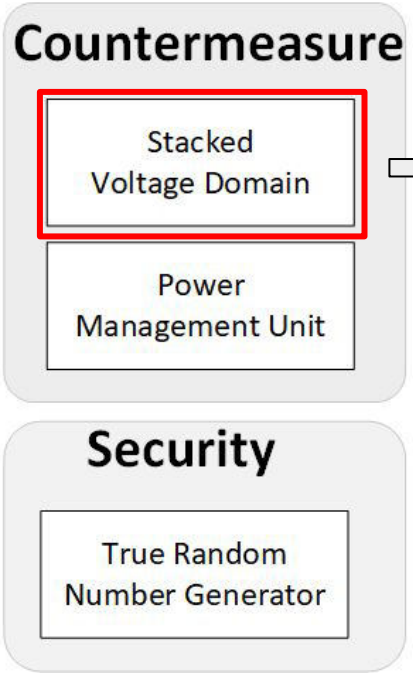
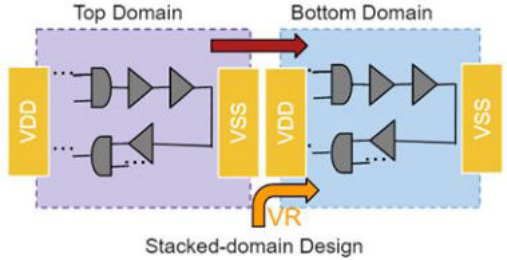
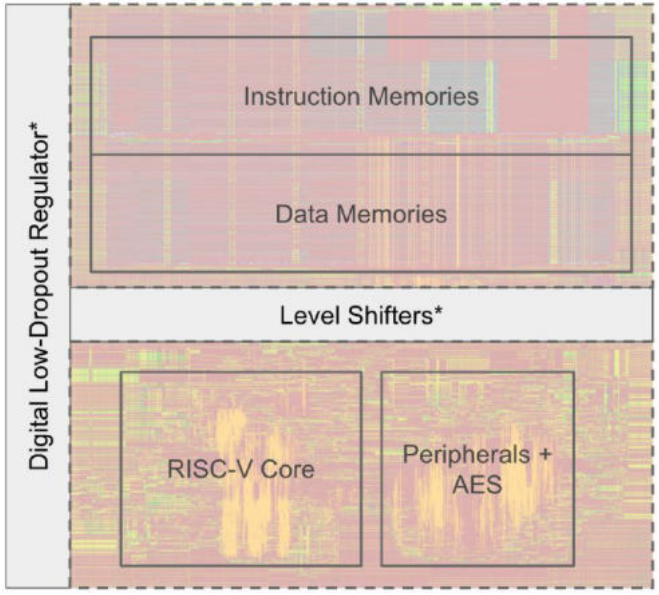
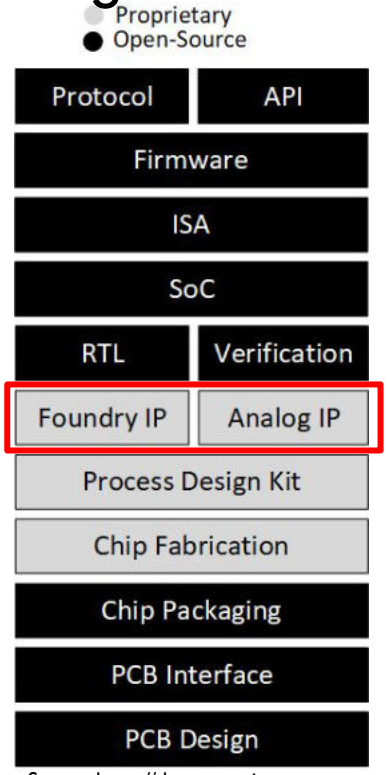






Open-Source Opentitan RoT

Voltage Stacked SoC



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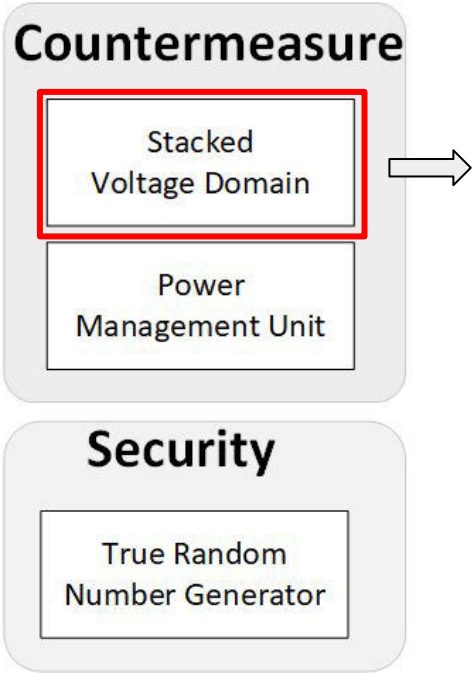
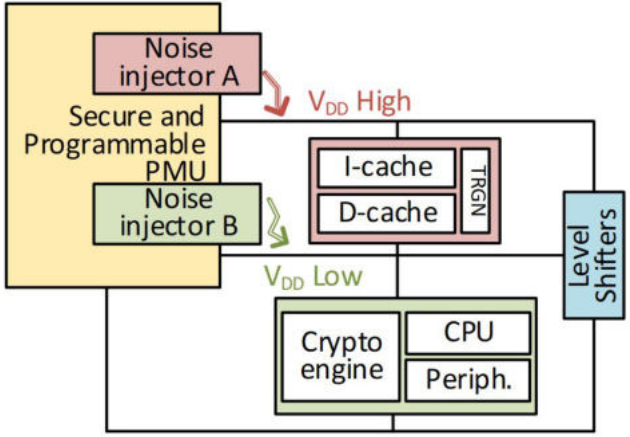




- 1st version of the PMU
- SoC includes:
  - Crypto engine
  - IBEX Core

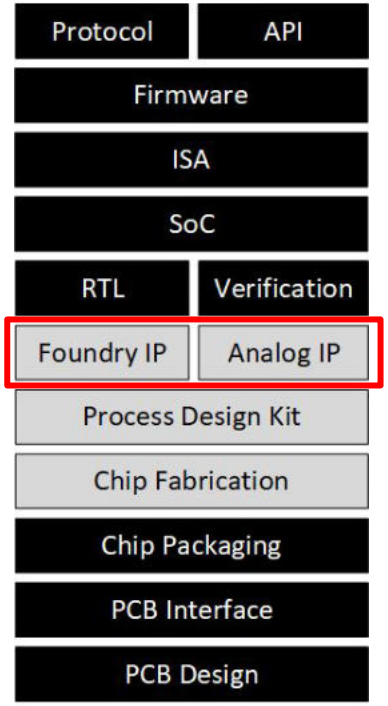
Goals:

- Perform DPA and check the efficiency of the power obfuscation techniques
- New open-source PPA (silicon results)

Open-Source Opentitan RoT

Secure Programmable PMU with Noise Injection

Proprietary
Open-Source



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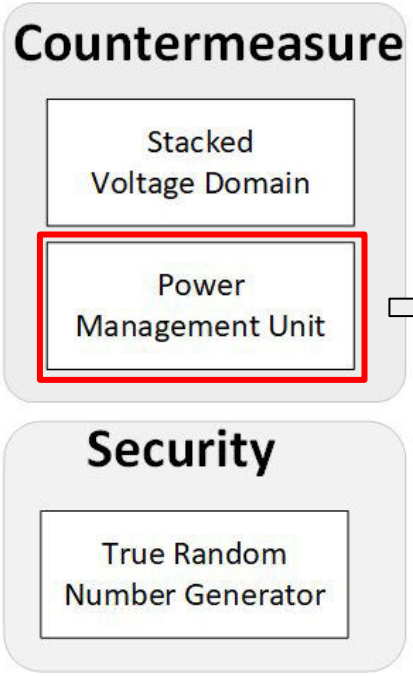
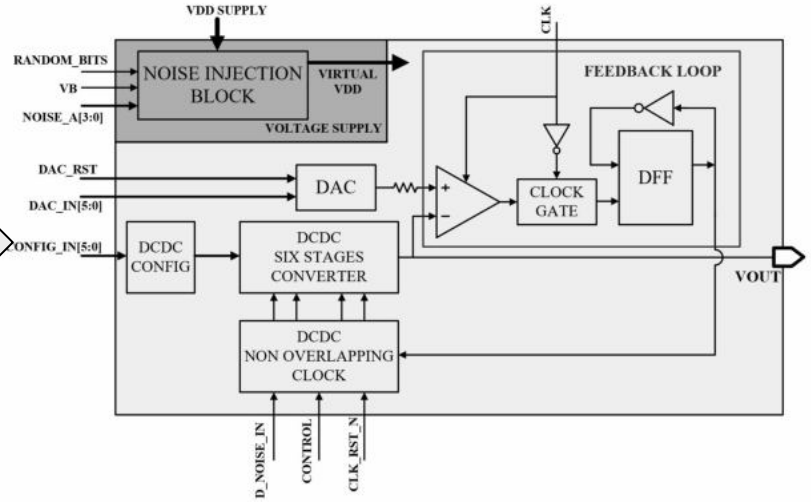
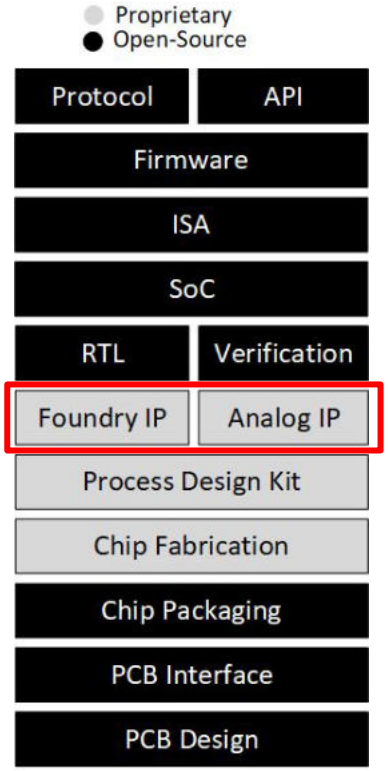




RRAM based TRNG



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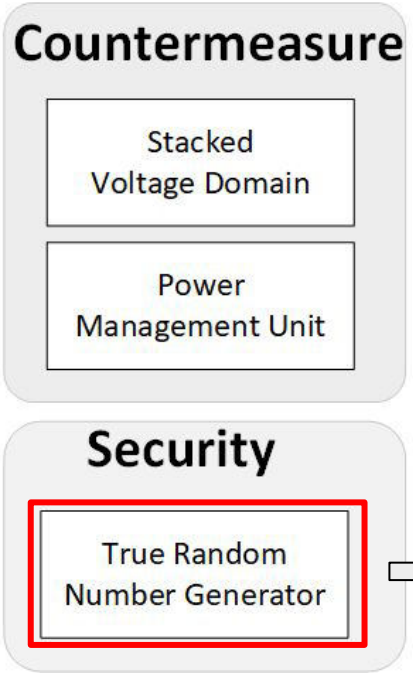
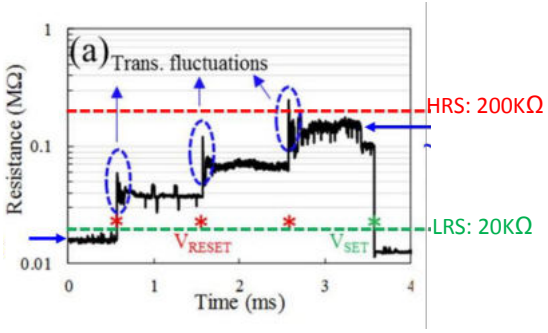
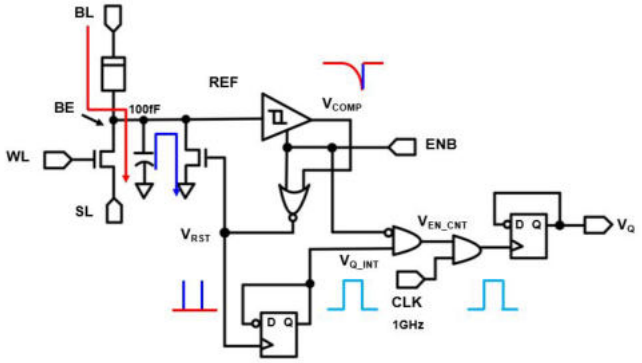


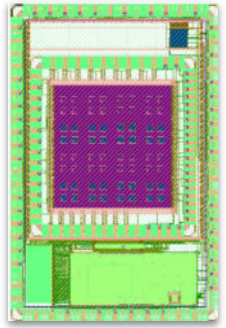




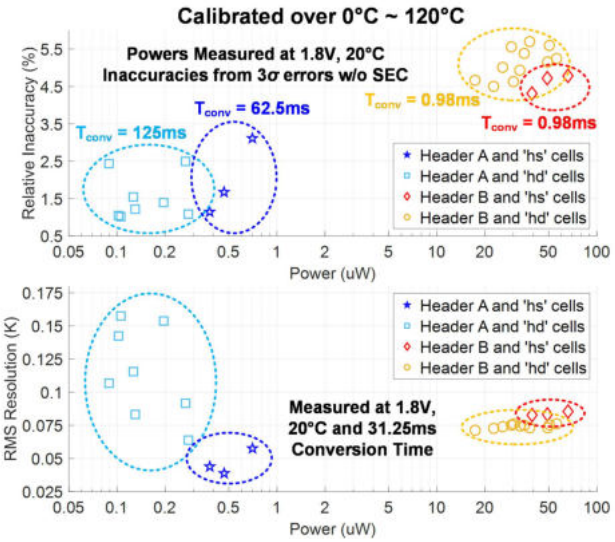
Building Confidence in Open Design

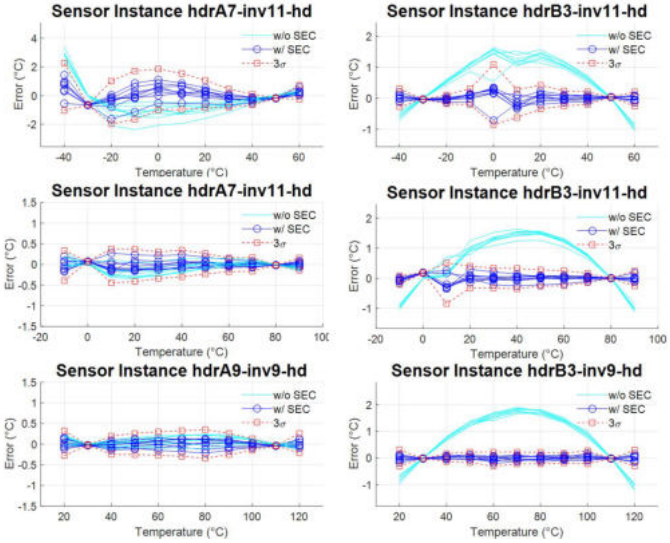
Building Confidence in *Open* Design

Start of Skywater's Open MPW Program



MPW1



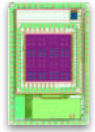


Dec .... Jun Aug Oct Dec Feb Apr Jun Aug Oct Dec Feb Apr Jun

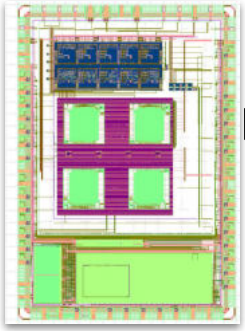
End of 2020 2021 2022 80 2024

Building Confidence in *Open* Design

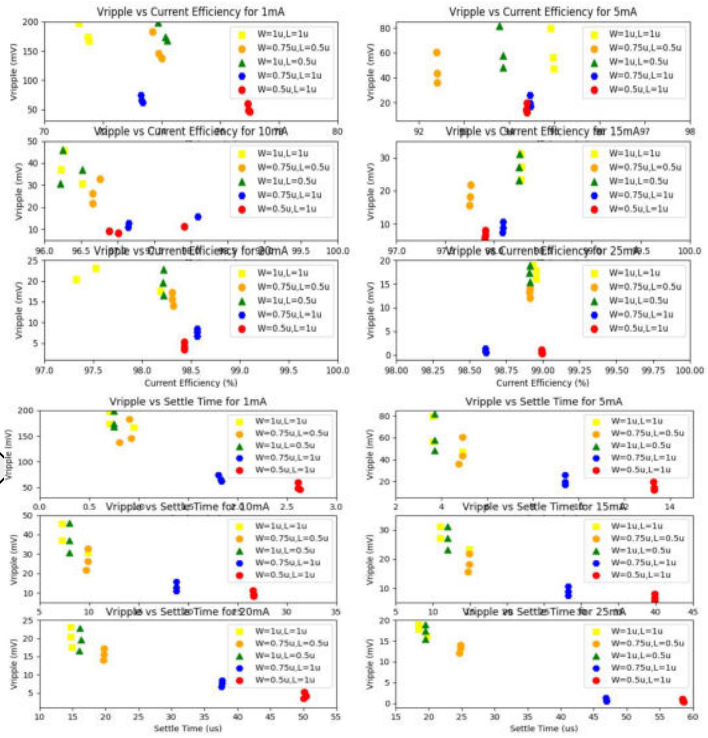
Start of Skywater's Open MPW Program

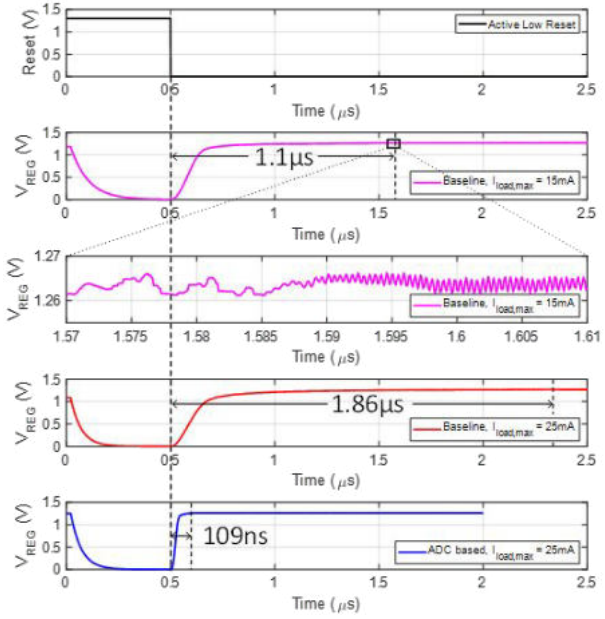


SKY130



MPW1 **MPW2**





Dec .... Jun Aug Oct Dec Feb Apr Jun Aug Oct Dec Feb Apr Jun

End of 2020 2021 2022 2024

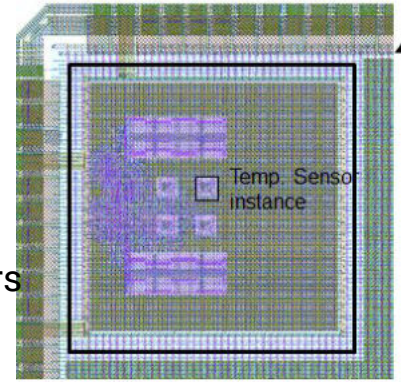
Building Confidence in *Open* Design

Tapeout throughDARPA IDEA Program

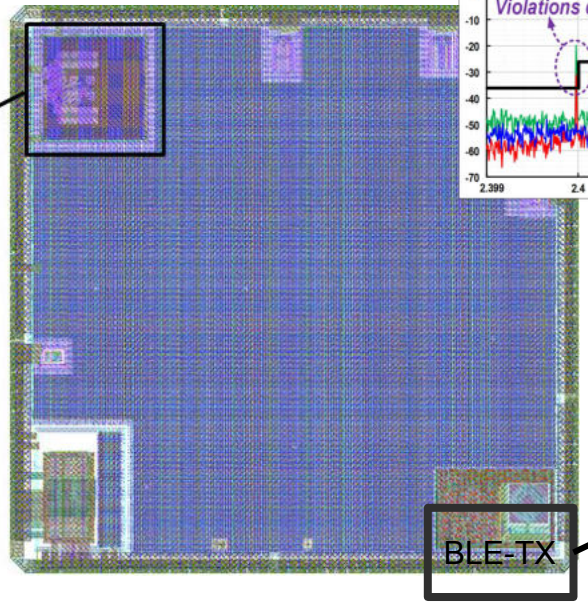
- 1st tapeout in GF12LP using open source tools

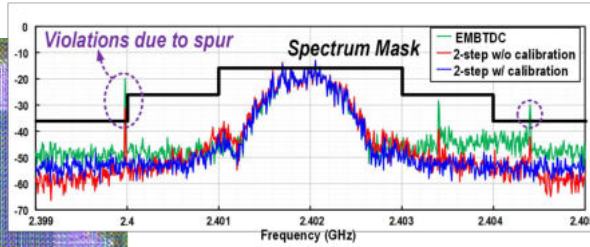
- Signoff using PT
  - @ TT|25C|0.8v|funcmax

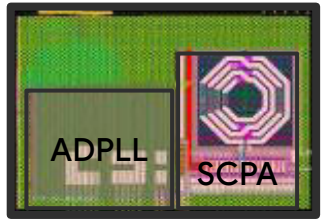
  350MHz
- Temperature sensors
  - T_{RANGE}: -20 to 100ºC
  - Error: +/- 0.2ºC (post-PEX)



GF 12-nm

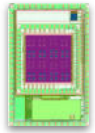


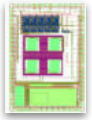




- ADPLL supports **1.8 to 2.7GHz**

SKY130





MPW1 **MPW2** MPW3

Dec .... Jun Aug Oct Dec Feb Apr Jun Aug Oct Dec Feb Apr Jun

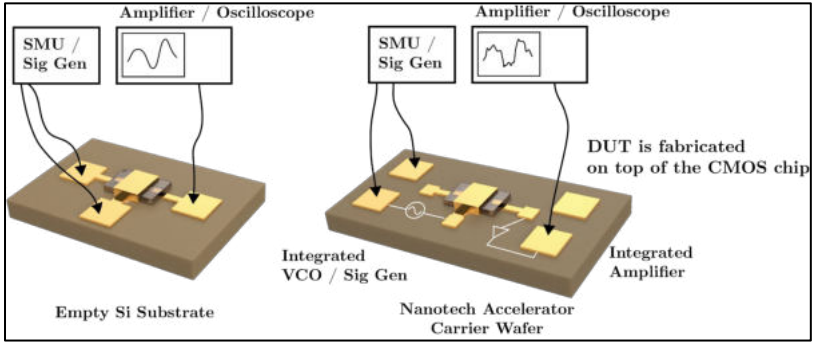
End of 2020 2021 2022 **Feb 24th** **May 28th** 82 2024

Building Confidence in *Open* Design

NIST

Start of Skywater's Open MPW Program

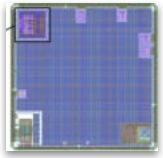
DARPA IDEA Program

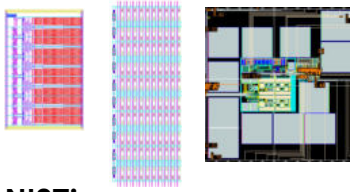


Nanofab. Accelerator program w. NIST

4 Testchips Already!
***Big* tapeout mid-June**

GF 12-nm





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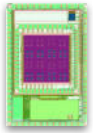
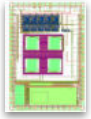
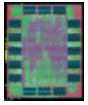
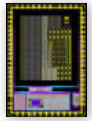






1st TO



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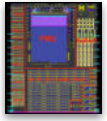
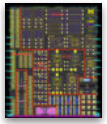
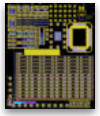


3rd TO



4th TO



NIST's Nanofabrication Tapeout

MPW1	**MPW2**	MPW3	MPW4	**MPW5**	**MPW6**	**MPW7**	**MPW8**				
Dec	.... Jun	Aug	Oct	Dec	Feb	Apr	Jun	Aug	Oct	Dec	Feb	Apr	Jun

End of 2020 — 2021 — 2022 — **Feb 24th** — **May 28th** — 83 — 2024

Building Confidence in *Open* Design

Start of Skywater's Open MPW Program

DARPA IDEA Program

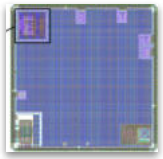
Nanofab. Accelerator program w. NIST

Globalfoundries Open MPW Program

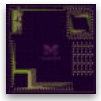
Accelerating Fitbit's Custom Silicon Goals!

fitbit

GF 12-nm

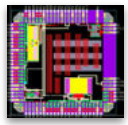


GF 180

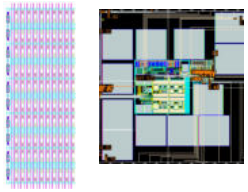


MPW0

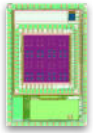
GF 180



Project w. Fitbit

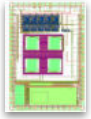


NIST's Nanofabrication Tapeout



SKY130

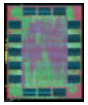
MPW1 Dec



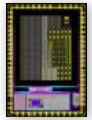
MPW2 .... Jun

MPW3 Aug

Oct

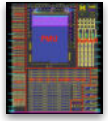


MPW4 Dec



1st TO

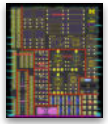
MPW5 Feb



2nd TO

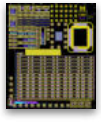
MPW6 Apr

Jun



3rd TO

MPW7 Aug



4th TO

MPW8 Oct

Dec

Feb

Apr

Jun

End of 2020

2021

2022

Feb 24th

May 28th

84

2024

Building Confidence in *Open* Design

Intel's University Shuttle

intel foundry services

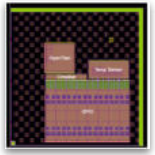
Start of Skywater's Open MPW Program

DARPA IDEA Program

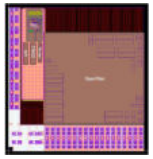
Nanofab. Accelerator program w. NIST

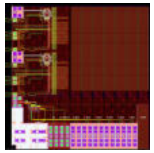
Globalfoundries Open MPW Program

Intel 16-nm

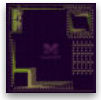


Intel 16-nm



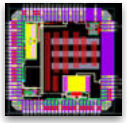


GF 180

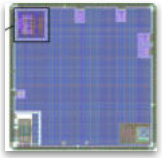


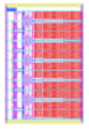
MPW0

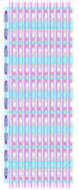
GF 180



GF 12-nm

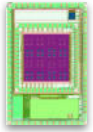


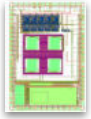


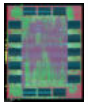


Project w. Fitbit

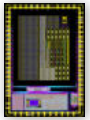
SKY130



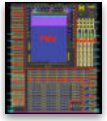




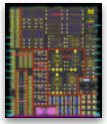
1st TO



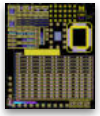
2nd TO



3rd TO



4th TO



NIST's Nanofabrication Tapeout

MPW1	MPW2	MPW3	MPW4	MPW5	MPW6	MPW7	MPW8
Dec	.... Jun	Aug	Oct	Dec	Feb	Apr	Jun	Aug	Oct	Dec	Feb	Apr	Jun

End of 2020

2021

2022

Feb 24th

May 28th

85

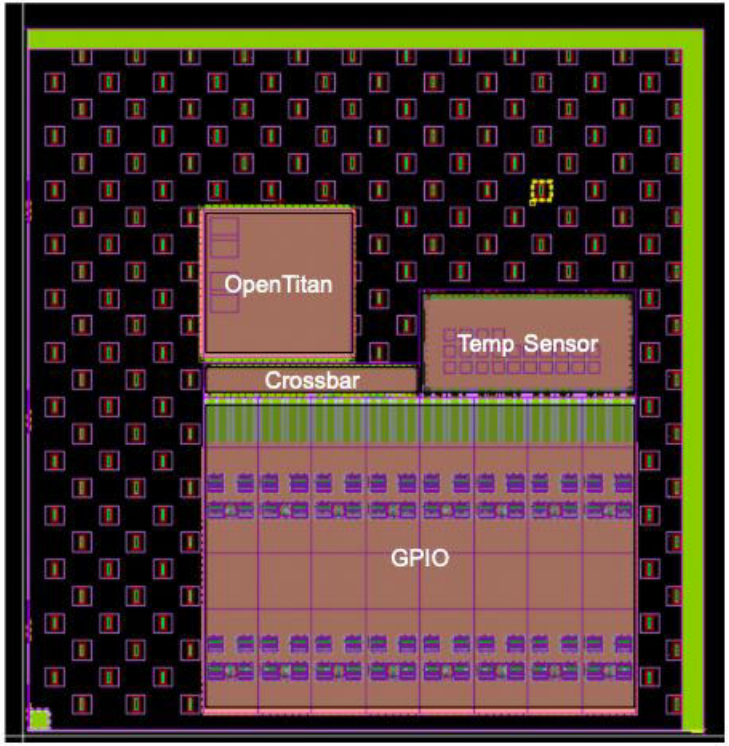
2024

We *Need* More Shuttles!

Tape Outs in Intel 16 - OpenTitan SoC

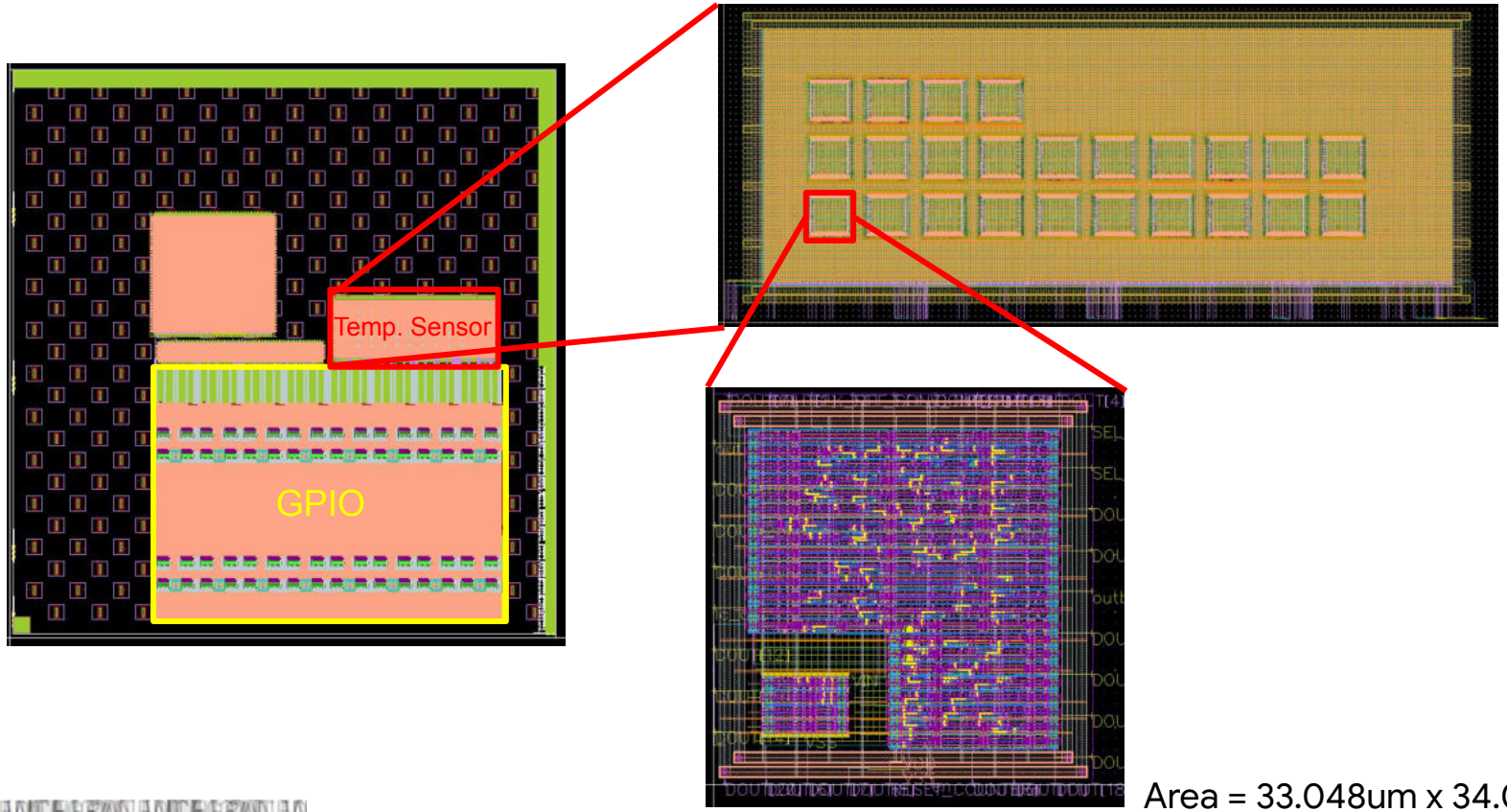
- Tapeout in Intel 16nm using OS tools
- PD and timing optimization using OpenROAD
- Used a modular flow to smoothly fill-in the gaps using proprietary tools

- Temperature Sensor RTL to GDS flow is fully Open-Source



Floorplan of Intel 16 tapeout Including Opentitan, Temperature sensor array and crossbar using OpenROAD

24 Temperature Sensors Array

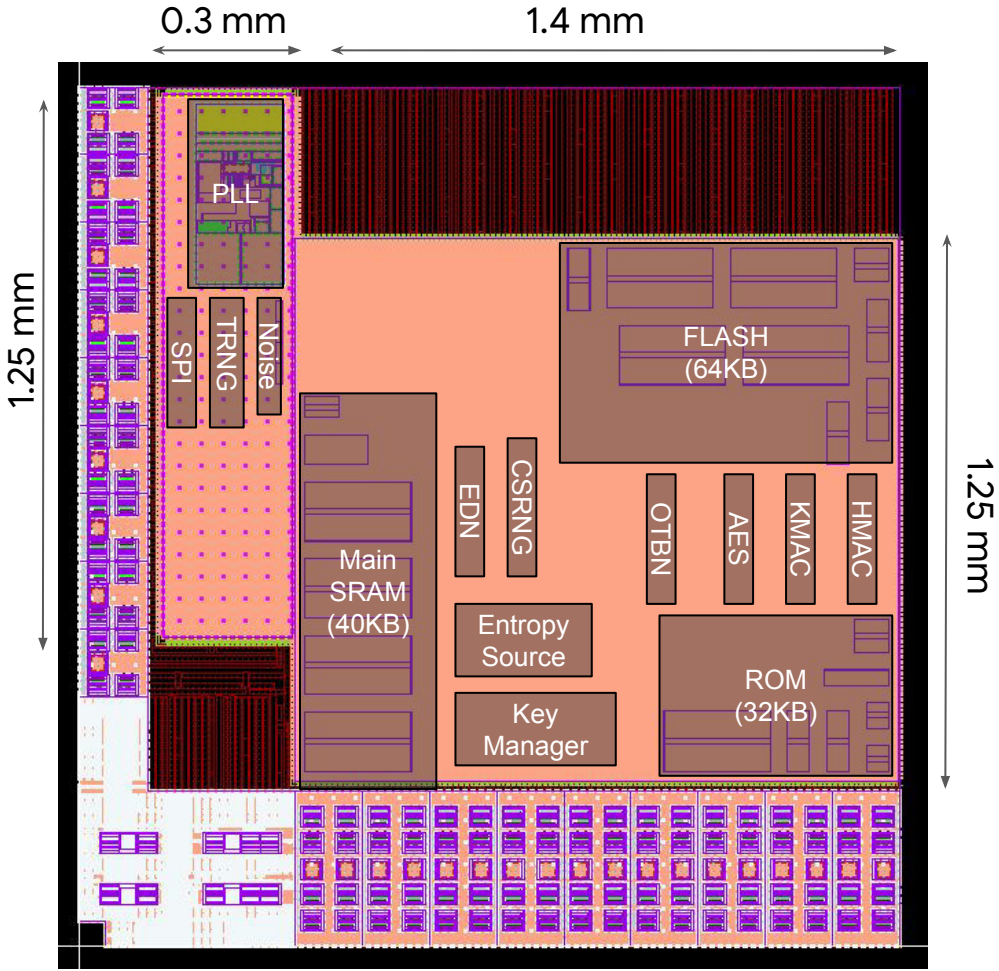


Area = 33.048um x 34.02um

OpenTitan Root of Trust SoC - Final Version

- All digital edge tracing TRNG
- Tunable Noise Injection
- On-chip high speed PLL
- OpenTitan security subsystem
  - Crypto + Key Manager
  - Secure Memory

Frequency	28MHz
Memory Size	16KB
Gate Count	20K
# of Macros	26
Area	2.18mm^2



What is next?

Bridging Gaps between Hardware & Software

Make custom silicon easier to build, at scale, just like software

“My god,
it’s full of software!”

```
$ gcc -OSilicon
```

Bridging Gaps between Hardware & Software

Packaging
conda-eda
github.com/hdl/conda-eda

```
conda install --channel litex-hub \
              open_pdks.sky130a   \
              openlane            \
              xls
```

“My god,
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Bridging Gaps between Hardware & Software

Packaging
conda-eda
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```
conda install --channel litex-hub \
              open_pdks.sky130a   \
              openlane            \
              xls
```

"My god,
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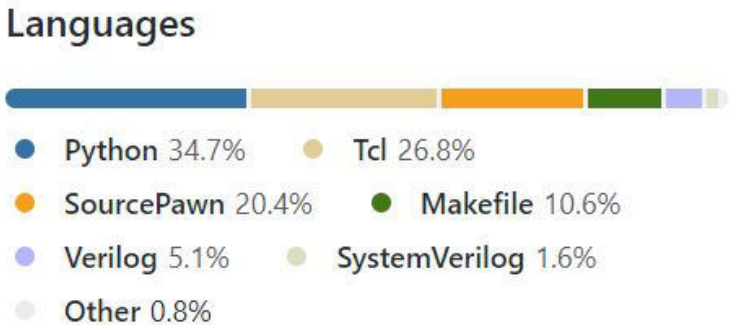
Reproducible, Reusable
Jupyter Notebook
github.com/chipsalliance/silicon-notebooks/

Bridging Gaps between Hardware & Software

- OpenFASOC GitHub Repo is mainly Code and Documentation



"My god,
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Bridging Gaps between Hardware & Software

- OpenFASOC GitHub Repo is mainly Code and Documentation
  - Auditable and Transparent
  - Regression Tests
  - Systematic Metrics Extraction
  - Dashboards

"My god,
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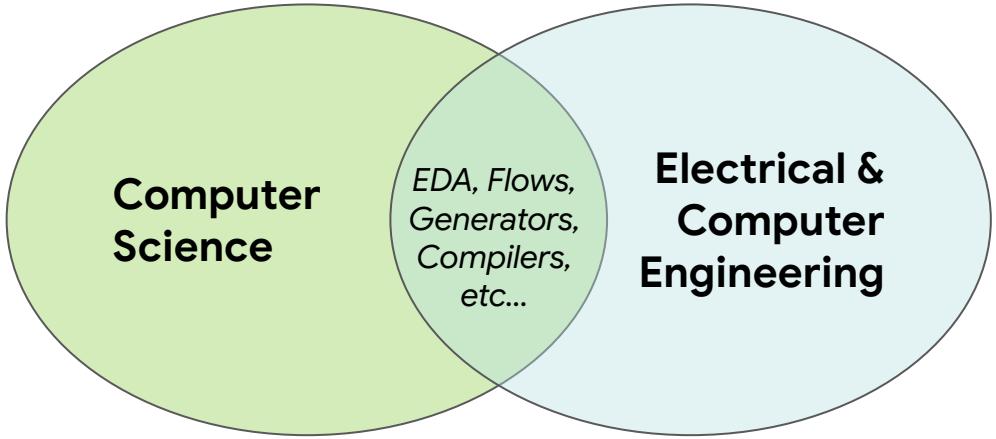
Bridging Gaps between Hardware & Software

- OpenFASOC GitHub Repo is mainly Code and Documentation
  - Auditable and Transparent
  - Regression Tests
  - Systematic Metrics Extraction
  - Dashboards
- Analog Automation requires collaborative Work
  - EDA, Analog/RF/Circuits, Software

"My god,
it's full of software!"

Bridging Gaps between EE & CS

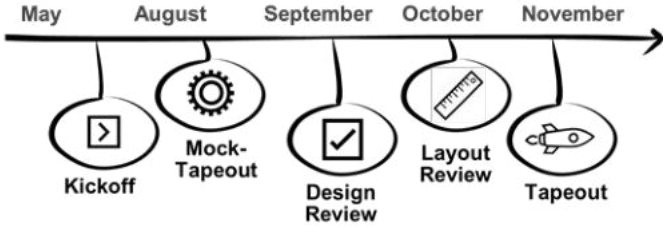
- Existing efforts around Open-Source IC design

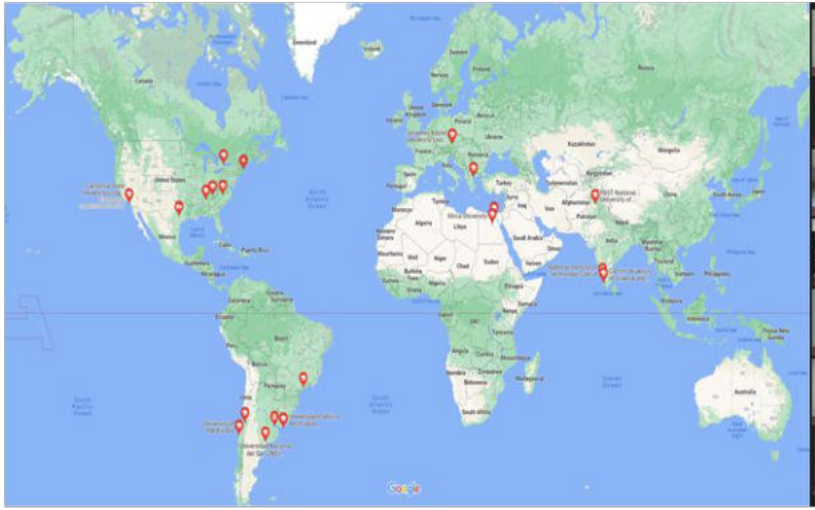


"My god,
it's full of software!"

SSCS PICO Chipathon

- 2021: 61 submissions, 18 selected (11 taped out)
- 2022: 54 submissions, 22 selected (14 taped out)

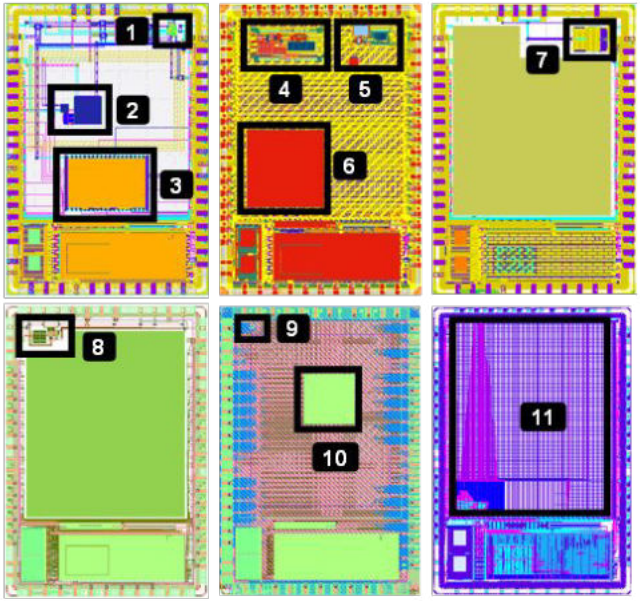




2022 selected teams from 10 countries, 5 continents

June 22, 2022, kick-off meetup with over 100 attendees

2021 Chipathon

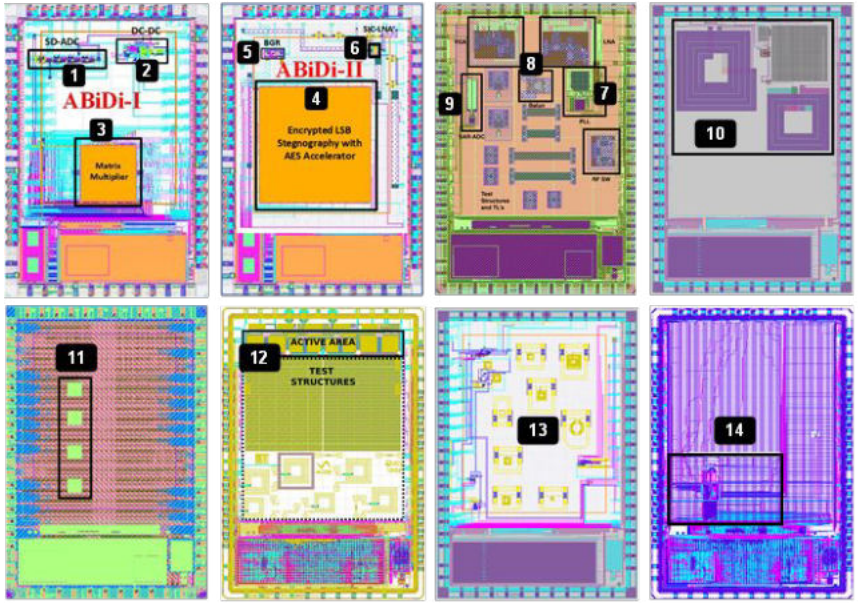


	Function	Team	Chip URL
1	5G bidirectional amplifier	Pakistan3 (FAST National University)	https://efabless.com/projects/560
2	Wireless power transfer unit	Pakistan2 (FAST National University)	
3	Variable precision fused multiply-add unit	Pakistan1 (FAST National University)	
4	Oscillator-based LVDT readout	India2 (Anna University)	https://efabless.com/projects/474
5	Temperature sensor	India1 (Anna University)	
6	GPS baseband engine	India3 (Anna University)	
7	Ultra-low-power analog front-end for bio signals	Brazil2 (U. Federal de Santa Catarina)	https://efabless.com/projects/476
8	TIA for quantum photonics interface	USA4 (University of Virginia)	https://efabless.com/projects/470
9	Bandgap reference	Egypt (Cairo University)	https://efabless.com/projects/473
10	Neural network for sleep apnea detection	USA2 (University of Missouri)	
11	SONAR processing unit	Chile (University of the Bio-Bio)	https://efabless.com/projects/540

- Paid runs via Efabless chipIgnite (130 nm SkyWater)
- All designs are open source

Magazine article: "SSCS PICO Contestants Cross the Finish Line," https://ieeexplore.ieee.org/document/9694491

2022 Chipathon

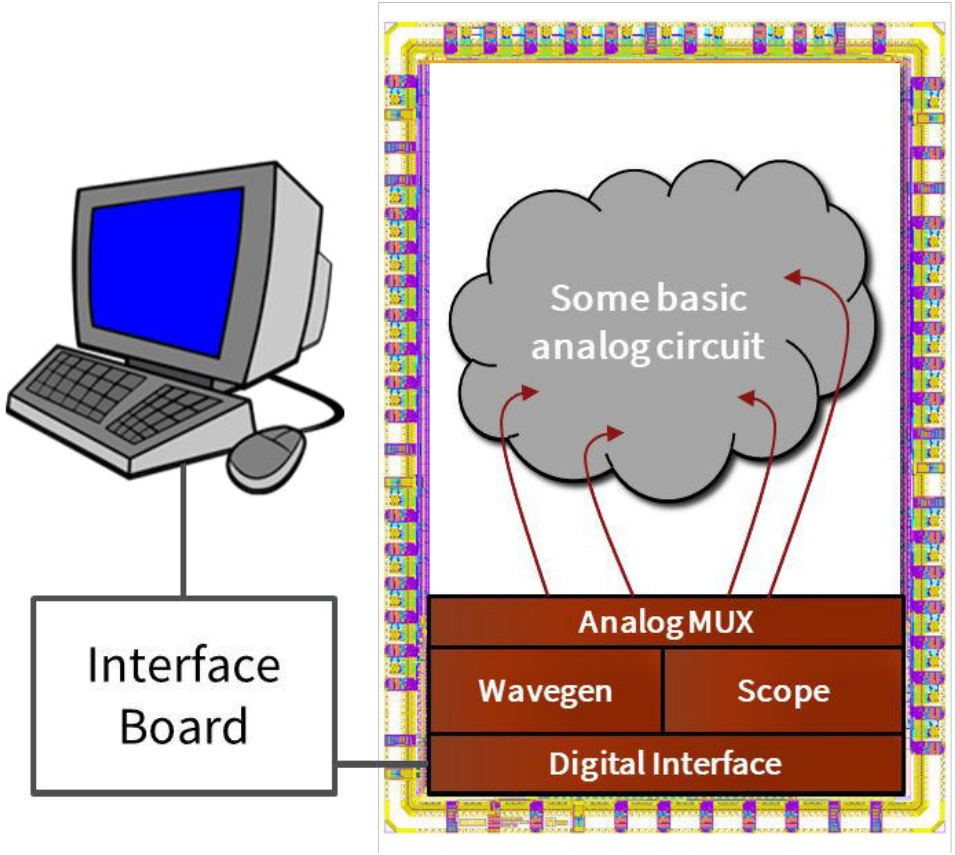


	Function	Team	Chip URL
1	Spatial Sigma-Delta ADC	Pakistan1 (FAST National University)	https://platform.efabless.com/projects/1486
2	On-Chip DCDC Converter with Fast Transient Response	Pakistan4 (FAST National University)	
3	Matrix Multiplier for AI at the Edge	Pakistan7 (FAST National University)	
4	Encrypted LSB Steganography with AES Accelerator	Pakistan2 (FAST National University)	https://platform.efabless.com/projects/1443
5	CMOS Bandgap Reference	Pakistan3 (FAST National University)	
6	Self-Interference Cancellation LNA	Pakistan4 (FAST National University)	
7	Sub-Sampling PLL for SerDes Applications	Austria (Johannes Kepler Univ., Linz)	https://platform.efabless.com/projects/1431
8	60 GHz Demonstrator Chip	Brazil (University of São Paulo)	
9	Low-Power 10-bit SAR ADC	USA1 (University of Alabama & MIT Lincoln Lab)	
10	Boost Converter for Battery-Powered IoT Applications	Greece (Aristotle University of Thessaloniki)	https://platform.efabless.com/projects/1457
11	Radiation-Hardened ALU	USA2 (North Carolina A&T State University)	https://platform.efabless.com/projects/1593
12	DC-DC Buck Converter for CubeSat	Chile[1]/Argentina[2]/Uruguay[3] [1]Universidad Técnica Fed. Santa María [2]Universidad Nacional del Sur & Instituto Nacional de Tecnología Industrial [3]Universidad Católica	https://platform.efabless.com/projects/1427
13	Electrochemical Water Quality Monitoring	USA5 (University of Tennessee)	https://platform.efabless.com/projects/1469
14	Mix-Pix - A Mixed-Signal Circuit for Smart Imaging	Chile (Universidad del Bío-Bío)	https://platform.efabless.com/projects/1494

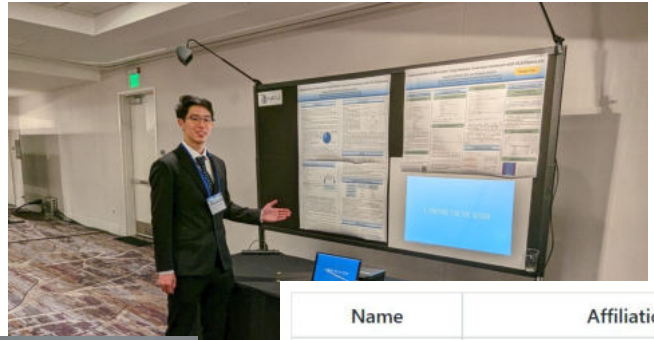
Magazine article: "Meet the SSCS PICO Chipathletes," https://ieeexplore.ieee.org/document/9950763

2023 Chipathon (Ongoing)

- Build on-chip waveform generator and “oscilloscope” macros
  - Collection of generally useful IP blocks
- Enable testing of low frequency analog circuits using only a PC
- Tape out first prototypes and improve with community over time



Notebook Code a Chip Competition at ISSCC'23



Name	Affiliation	Notebook Title
Yihai Zhang	Tsinghua-Berkeley Shenzhen Institute, Tsinghua University China	GreenRio 2: A Linux-compatible RISC-V Processor Developed with A Fully Open-Source EDA Flow
Anawin Opasatian	University of Tokyo (Japan)	Bernstein-Yang Modular Inversion with XLS/OpenLane
Mauricio Montanares	University of Concepción (Chile)	Sonar On Chip Project
Nealson Li	Georgia Institute of Technology (USA)	Coordinate Rotation Digital Computer (CORDIC) with OpenLane
HyungJoo Park	Hanyang University (South Korea)	Scan Register layout generation using laygo2
Ali Hammoud	University of Michigan (USA)	OpenFASoC: Digital LDO Generator
Nimish Shah	KU Leuven (Belgium)	DPU: DAG Processing Unit for probabilistic ML and sparse matrix algebra

Notebook Code a Chip Competition at VLSI'23

Example: Winner of VLSI 2023 Code-a-Chip Contest

Open in Colab

Design and Optimization of Analog LDO with Relational Graph Neural Network and Reinforcement Learning

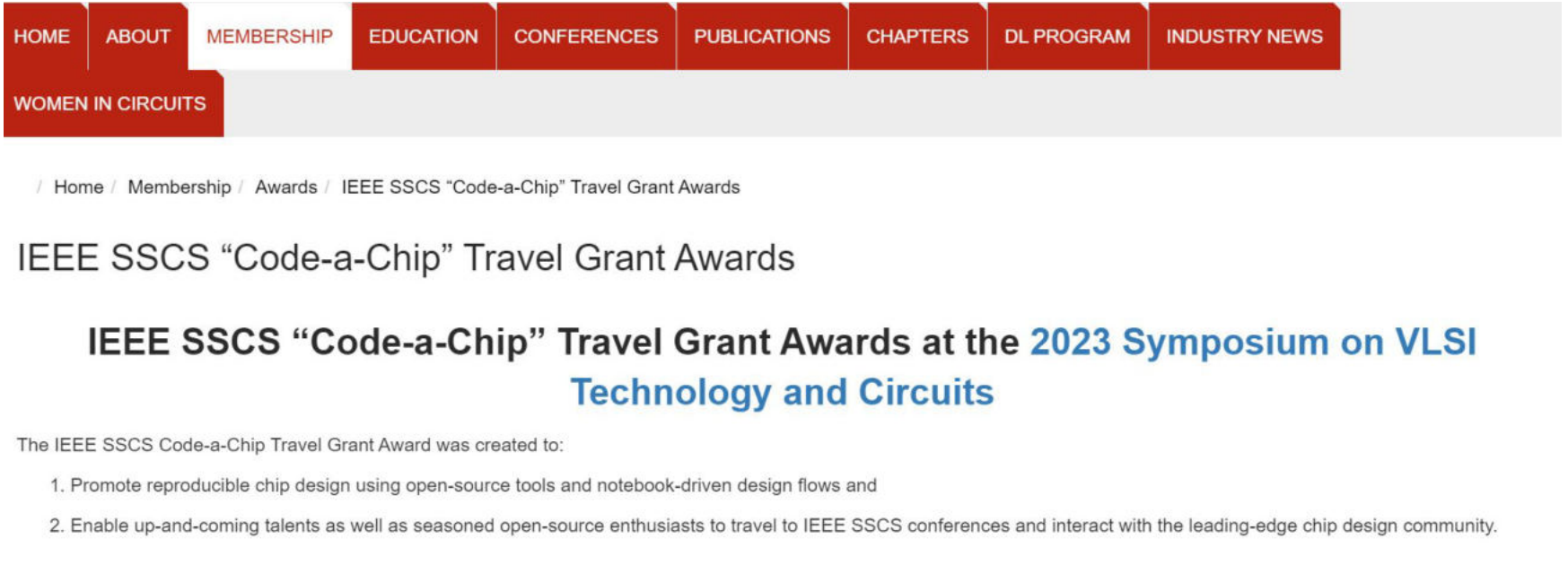
Zonghao Li Team, March 2023
SPDX-License-Identifier: Apache-2.0

Name	Affiliation	IEEE Member	SSCS Member
Zonghao Li (Lead) Email ID: zonghao.li@isl.utoronto.ca	University of Toronto	Yes	Yes
Anthony Chan Carusone (Advisor) Email ID: tony.chan.carusone@isl.utoronto.ca	University of Toronto	Yes	Yes

https://github.com/sscs-ose/sscs-ose-code-a-chip.github.io/blob/main/VLSI23/accepted_notebooks/ldo_rgcn_rl/ldo_rgcn_rl.ipynb

“Code-a-Chip” Notebook Competition at VLSI'23 - Kyoto

- IEEE Solid-State Circuits Society (SSCS) Open-Source Ecosystem (OSE)
  - https://github.com/sscs-ose/sscs-ose-code-a-chip.github.io



Monday AM Session @ ISCAS 2023

11:30 – 13:00
Review of the First Silicon Results in the Open Source Ecosystem
Room: San Carlos III (Marriott)
Session Chair(s): Mehdi Saligane, *University of Michigan*
Priyanka Raina, *Stanford University*

11:30
2273: An Open Source Compatible Framework to Fully Autonomous Digital LDO Generation
Yaswanth Kumar Cherivirala, Mehdi Saligane, David Wentzloff
University of Michigan, Ann Arbor, United States

11:48
2290: Design of Cryo-CMOS Analog Circuits Using the Gm/ID Approach
Christian Enz, Hung-Chi Han
École Polytechnique Fédérale de Lausanne, Switzerland

12:06
2314: SRAM Design with OpenRAM in SkyWater 130nm
Jesse Cirimelli-Low{2}, Muhammed Hadir Khan{2}, Samuel Crow{2}, Amogh Lonkar{2}, Bugra Onal{2}, Andrew Zonenberg{1}, Matthew Guthaus{2}
{1}IO Active, United States; {2}University of California, Santa Cruz, United States

11:24
2326: An Open-Source 4x8 Coarse-Grained Reconfigurable Array Using SkyWater 130 nm Technology and Agile Hardware Design Flow
Po-Han Chen, Charles Tsao, Priyanka Raina
Stanford University, United States

12:42
2327: Open-Source, End-to-End Auditable Tapeout of Hardware Cryptography Module
Anish Singhani
Carnegie Mellon University, United States

180 Attendees!! Record attendance among all workshops at VLSI Symposium

Open Source PDKs and EDAs, Community Experiences toward Democratization of Chip Design

Organizer : Makoto Ikeda (The University of Tokyo)å
Mehdi Saligane (University of Michigan)

Since its launch in 2020, the Open MPW shuttle program has received over 500
to designers' experiences, including measured results, foundry perspectives, an

About Makoto Ikeda
Makoto Ikeda received his BE, ME, and Ph.D. degrees all in EE department of
d.lab, the University of Tokyo. This workshop is co-organized with Dr. Mehdi S

| 1. Design experience: "The Journey of Two Novice LSI Enthusiasts: T
Communications and Yuki Azuma, University of Tsukuba

| 2. From Zero to 1000 Open Source Custom Designs in Two Years, Mo

| 3. The SKY130 Open Source PDK: Building an Open Source Innovation

| 4. Open Source Chip Design on GF180MCU – A foundry perspective, Karthik Chandrasekaran, Global

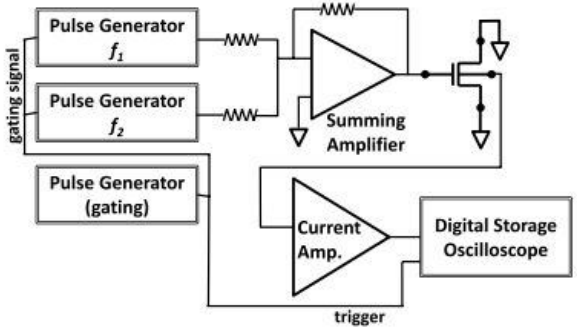
The end!

Bonus slides

Implementation Challenges

A. The quantized behavior is best shown in single-defect gate interfaces.
   a. When the device operates with a single defect, the CP current difference is either fully present or not, there is no middle values caused by randomness.
   b. It demands:
      i. Heavy binning to select a candidate device
      ii. Advanced process node that doesn't produce too much defects
B. The current is extremely small (<10fA @ 40MHz, L/W=50nm/100nm [1])
   a. Leakages are everywhere. The author suggests DRAM-optimized technology to minimize junction leakage [1].
   b. Considering lock-in amplify or other low-level signal measurement techniques. [4, 5]
   c. Direct amplification of this signal can result in a very large low-freq AC noise that's difficult to fully eliminate on-die. Considering mixed-signal circuits.

Charge Pumping (CP) Defect Measurement [5]



I_{CP} scales linearly with the CP gate pulse frequency such that

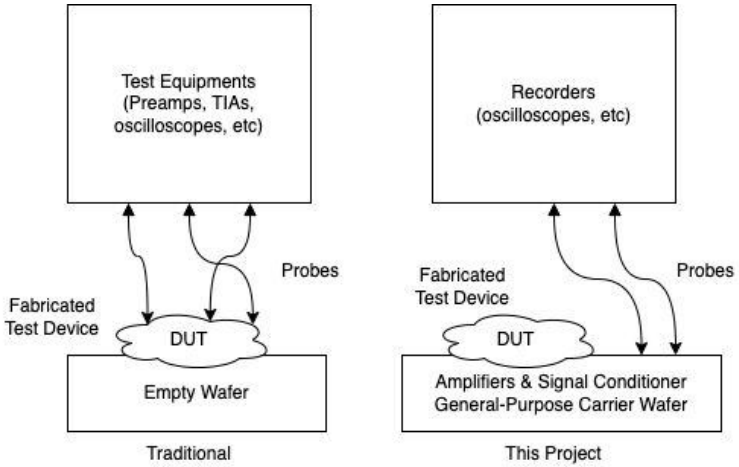
$$I_{CP} = q A f D_{it} \Delta E \quad (1)$$

where q is the electronic charge, A is the device area, D_{it} is the energetic and areal interface state density (cm^{-2} eV^{-1}), and ΔE is the CP recombination energy window [3]. For the case

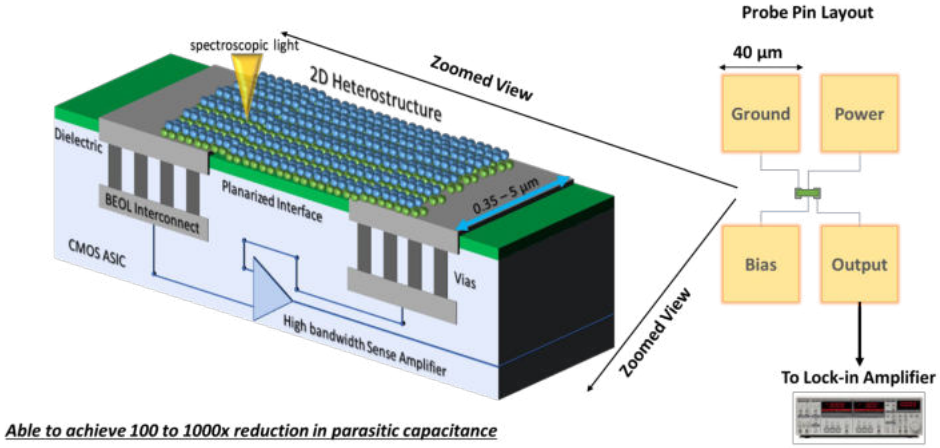
$$I_{total} = I_{cp}(f) + I_{other}$$

The number of SiO2-gate interface defects (N_{it}) can be measured by: applying a square wave to the MOS stack and measure the change in bulk current. The CP current can be isolated because it behaves differently with frequency compared to the other leakages.

Nanotechnology Accelerator



The concept

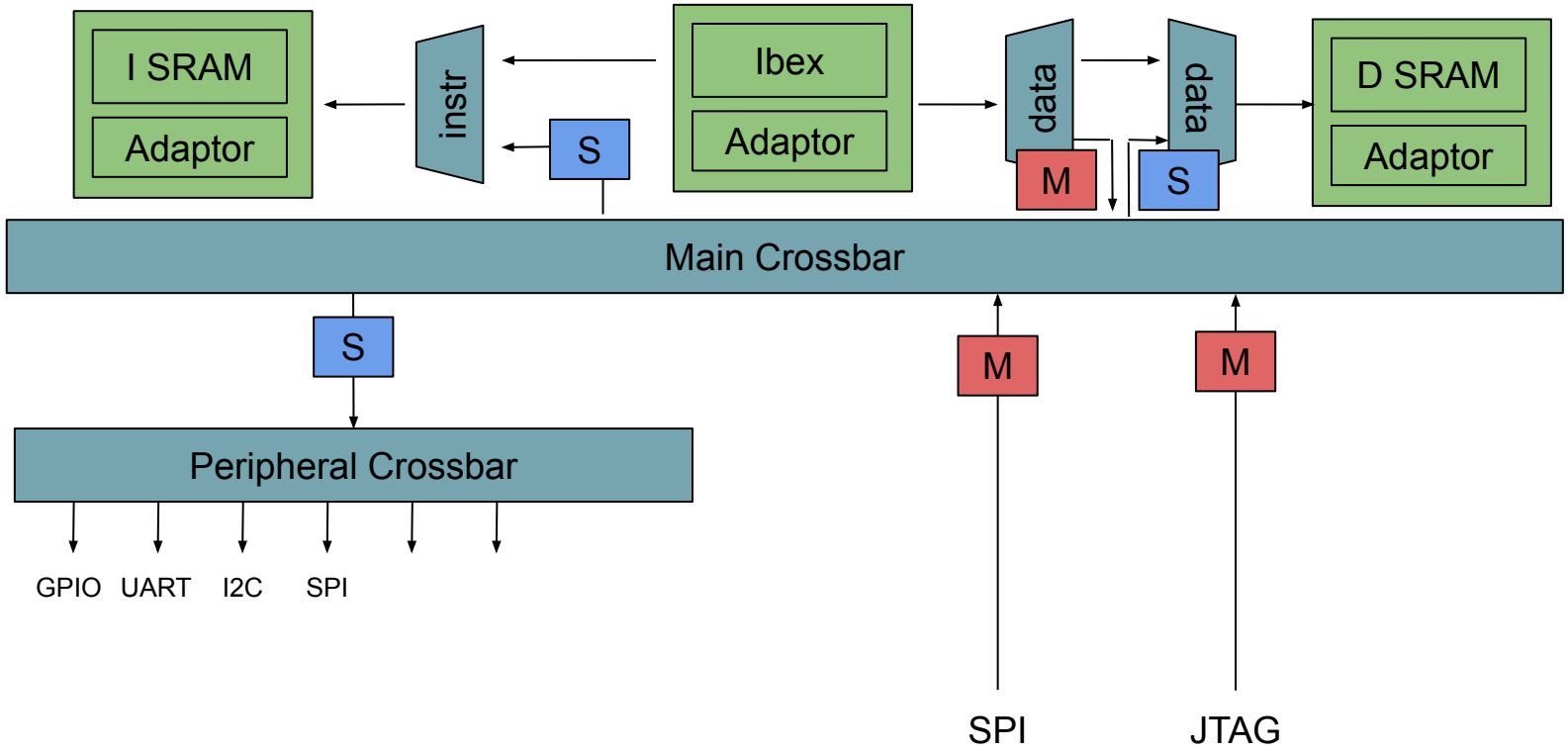


Example Usage of such a Carrier Wafer

The aim of this project is to put some test apparatus on a silicon chip, which will be used as the carrier wafer for new nano device fabrication.

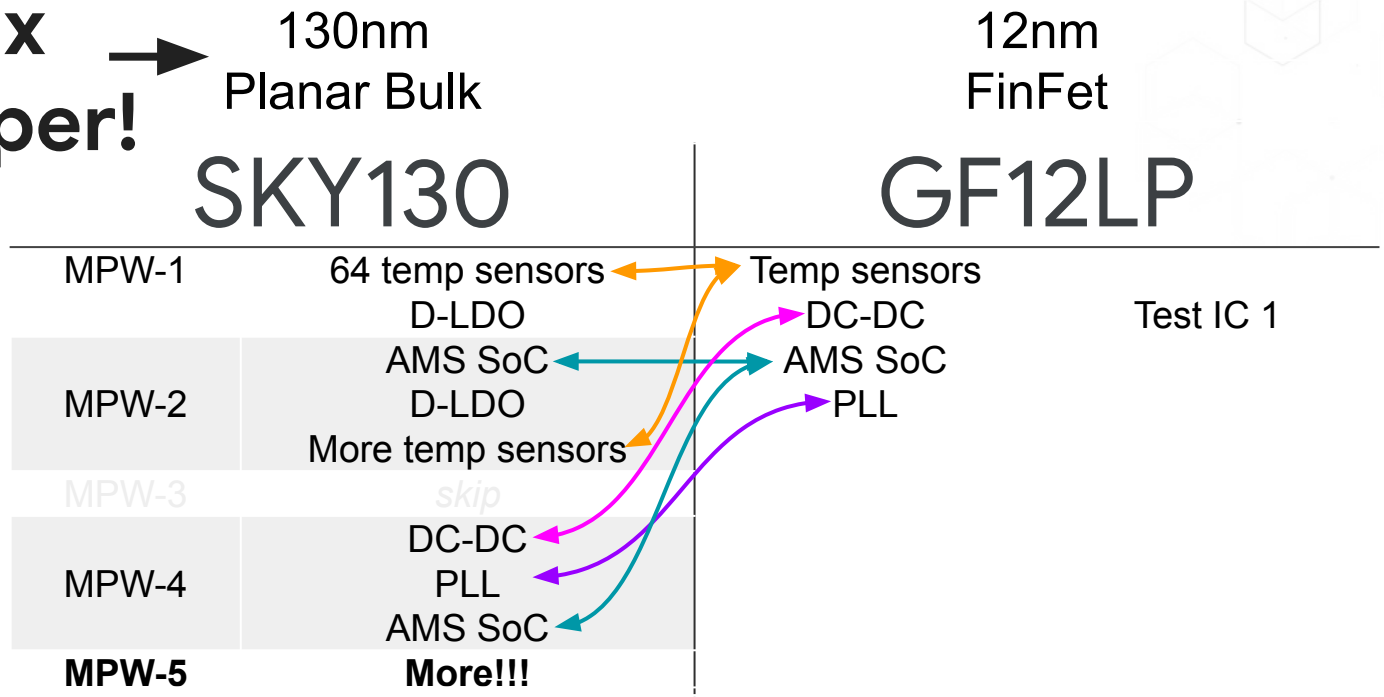
Drastically reduced parasitics can lead to improved measurement quality and test ranges.

Tape Outs in Intel 16 - OpenTitan SoC



OpenFASoC - *Portable* **Transferrable** Analog

>10x cheaper! →



Same **fully** open source tools
Same scripting generators

UNIVERSITY OF MICHIGAN

OpenFASoC - *Portable* Analog

- Analog generators - Power DCDC + LDO, Temperature Sensors, PLLs, ADCs.
- Example mixed signal SoC integration.
- Silicon proven with increasingly more tape outs, increasingly faster!

- Fully open source flow using fully open source tooling (OpenROAD, Xyce).
- Demonstrating **acceleration** of velocity and productivity.

SKY130 ⟷ GF12LP

130nm
Planar Bulk

12nm
FinFet

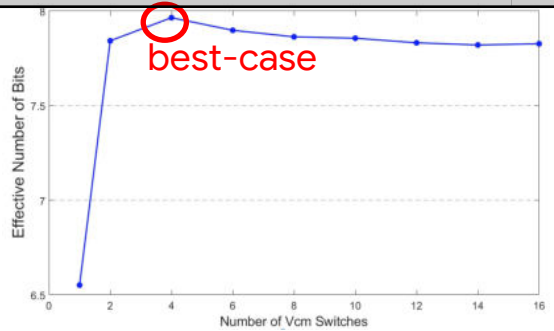
>10x ↗ cheaper!

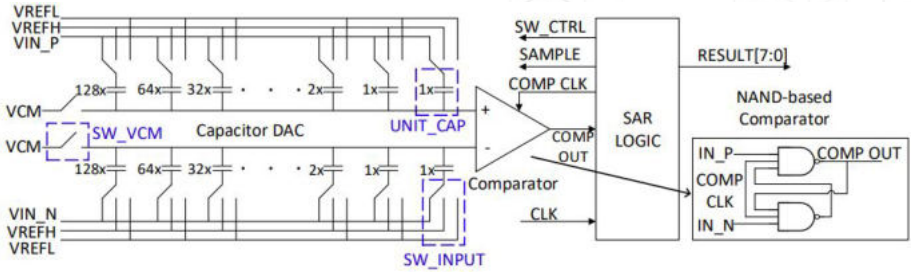
Same **fully** open source tools
Same scripting generators

SAR ADC Common Centroid Placement

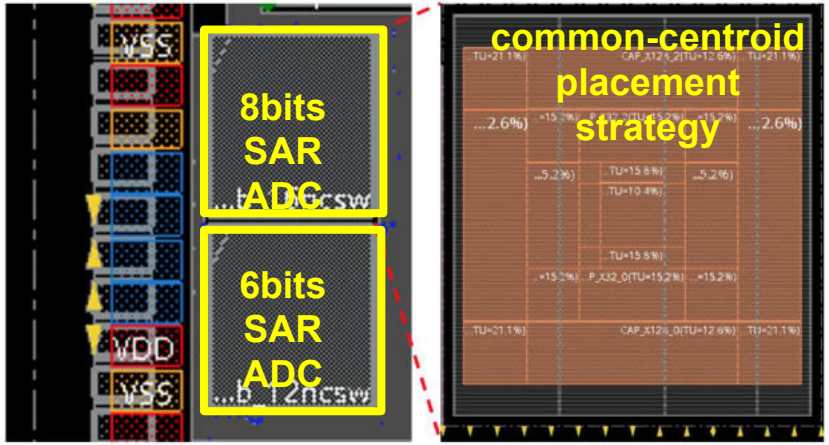
- Symmetrical Placement of unit caps and switches

Output Spec.	CDL	PEX
$F_{SAMPLING}$ (MHz)	1	
Unit Cap Value (fF)	2.6	
Area (mm^2)	-	0.04
Power (μW)	6.72	11.2
Effective Number of Bits	7.86	7.75

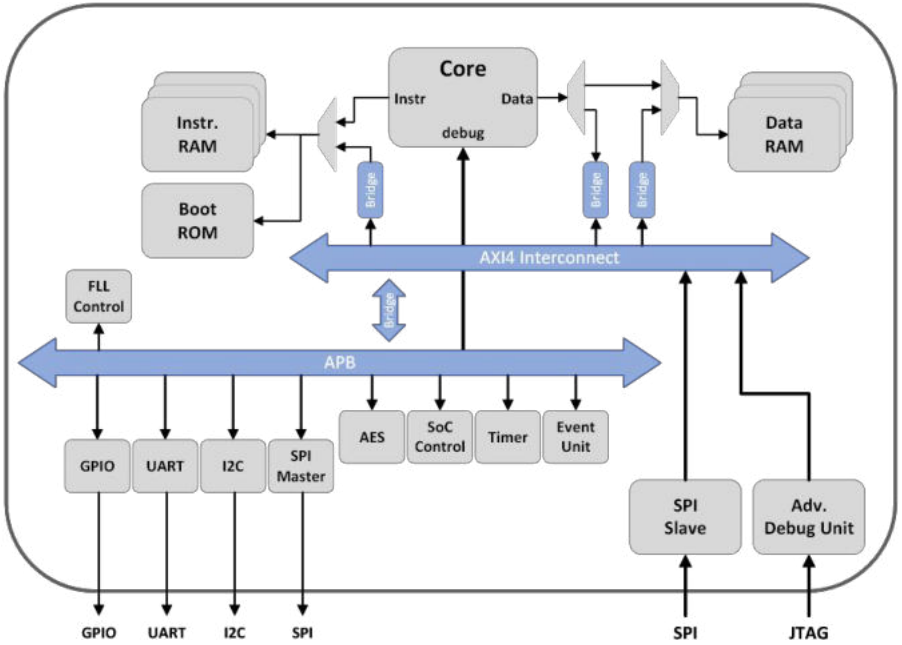


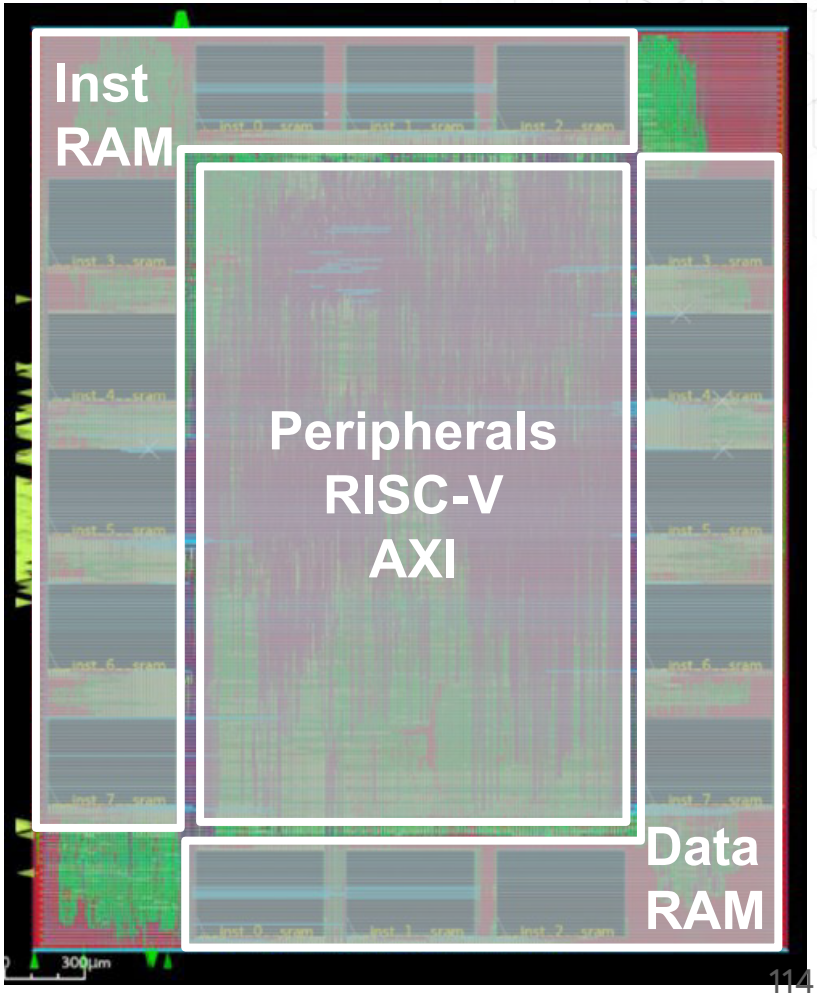


SAR ADC Block Diagram



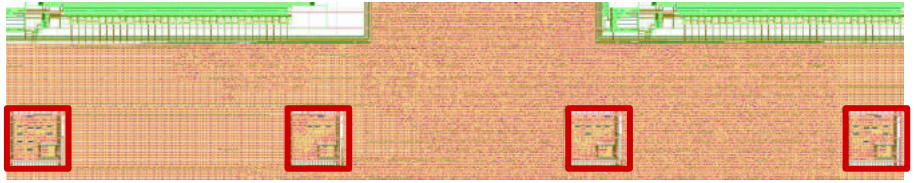
Open Source RoT

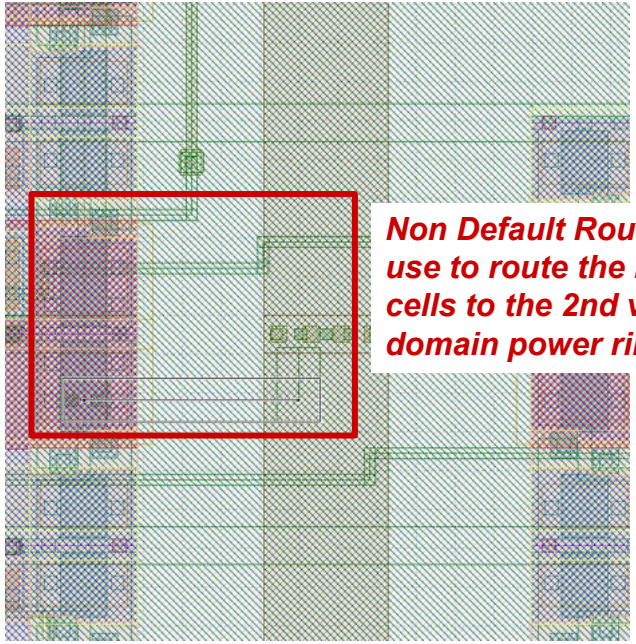




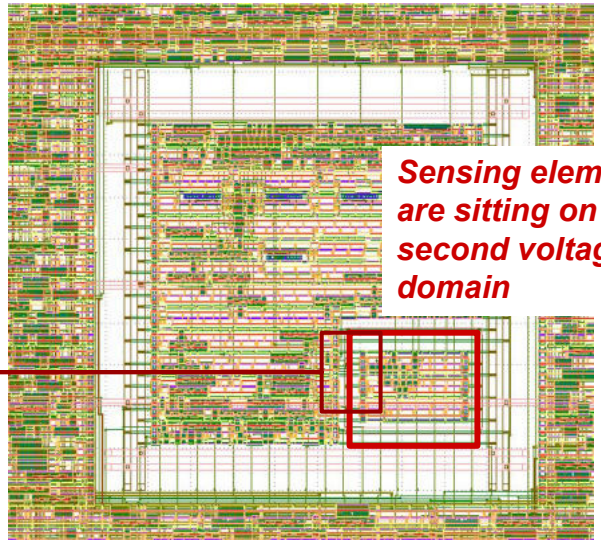
OpenFASOC on MPW-II: Integrated Temperature Sensors

Sensors are embedded inside the OpenTitan SoC and connected through tilelink

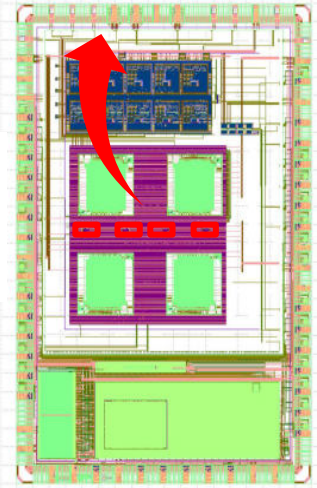




Non Default Routing is use to route the header cells to the 2nd voltage domain power ring

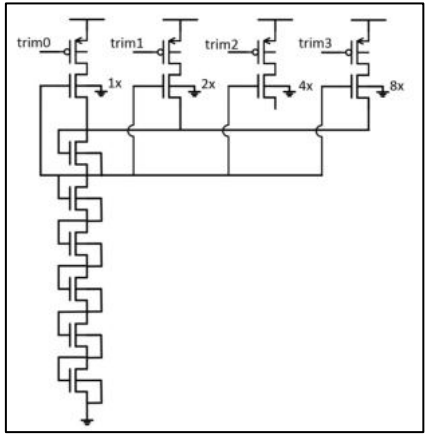


Sensing elements are sitting on a second voltage domain

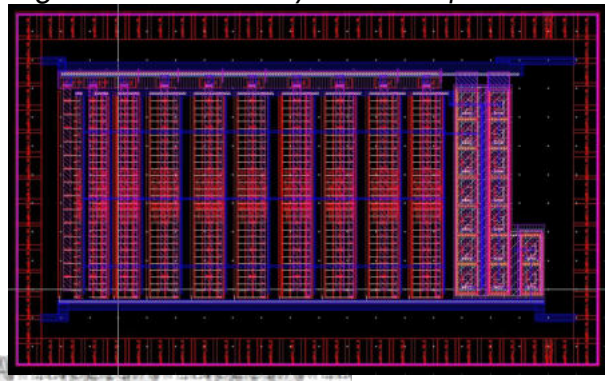


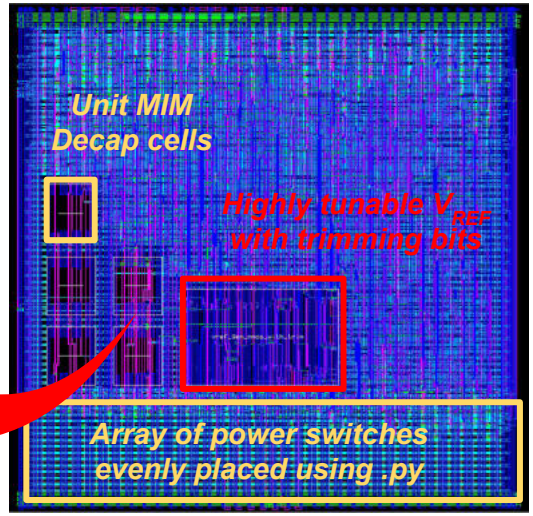
The temperature sensor generator uses a fully open source flow

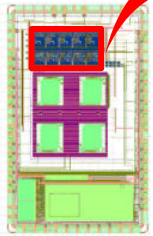
OpenFASOC on MPW-II: D-LDO generator

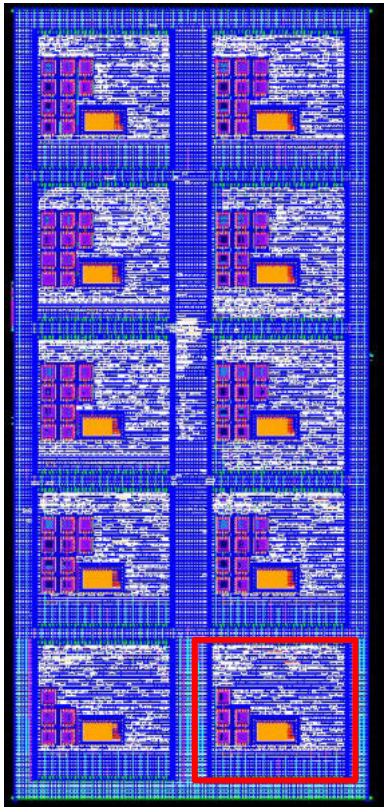


Voltage Reference with symmetrical placement



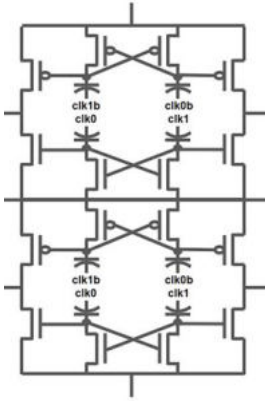




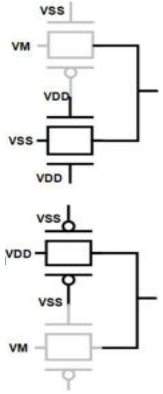


Array of D-LDOs

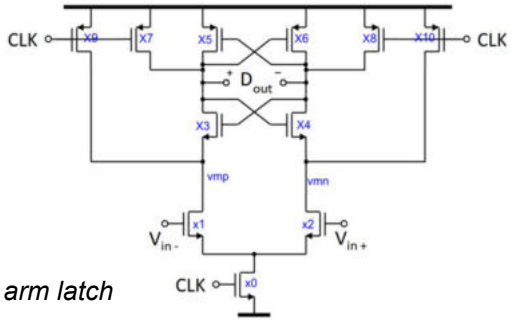
Analog Cell Generation using ALIGN



2:1 converter Slice

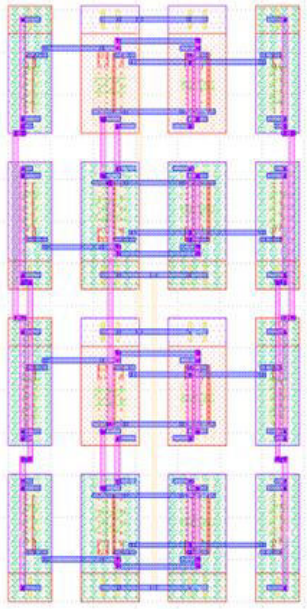


Power mux

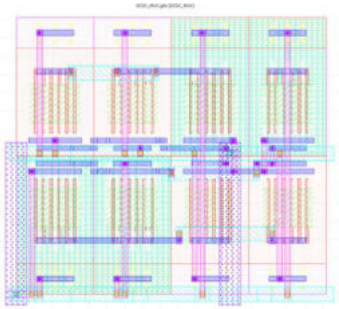


Strong arm latch

Generated Analog “Auxiliary Cells”



2:1 converter Slice

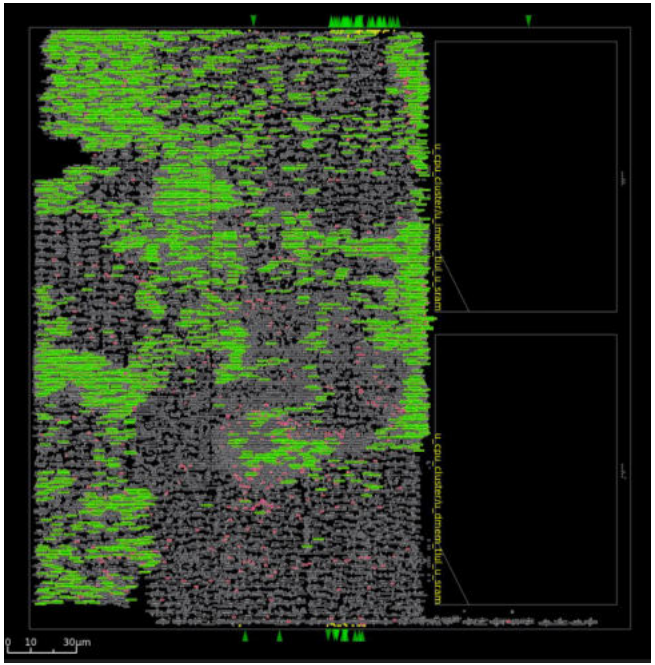


Power mux

Strong arm latch

Tape Outs in Intel 16 - OpenTitan SoC

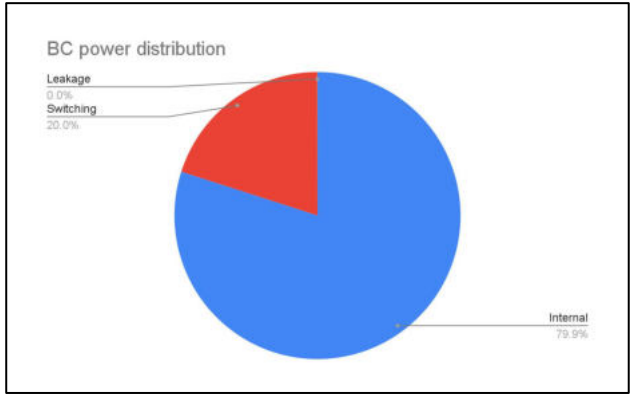
- OpenTitan SoC contains
  - SPI, GPIO interfaces
  - Ibex CPU
  - 16KB SRAM
  - Main crossbar and peripheral crossbar
  - All peripherals are connected through Tilelink

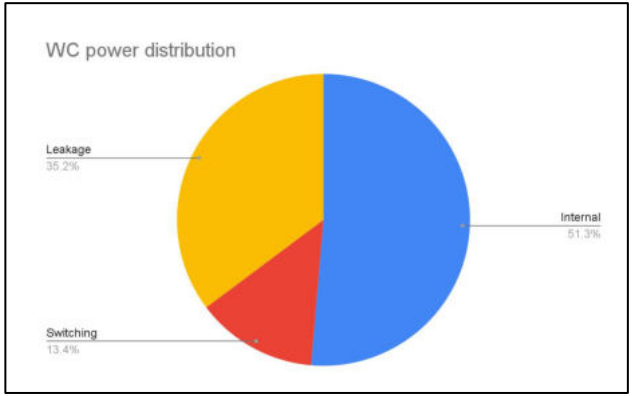


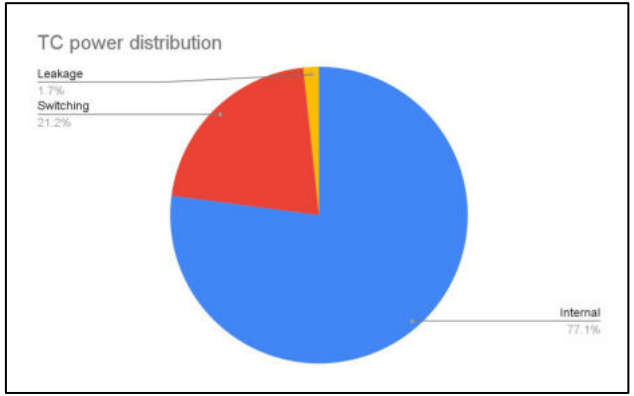
Floorplan of in Intel 16 Including RAMs and an OpenROAD based implementation of the Opentitan SoC

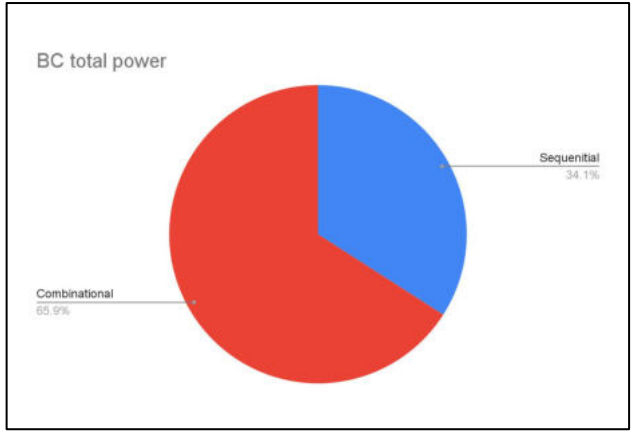
Frequency	Util.	Macro Place Channel	Macro Place Halo	Cell Pad	Area
28MHz	29% *64%	40 40	20 20	2 sites	425x425 um2

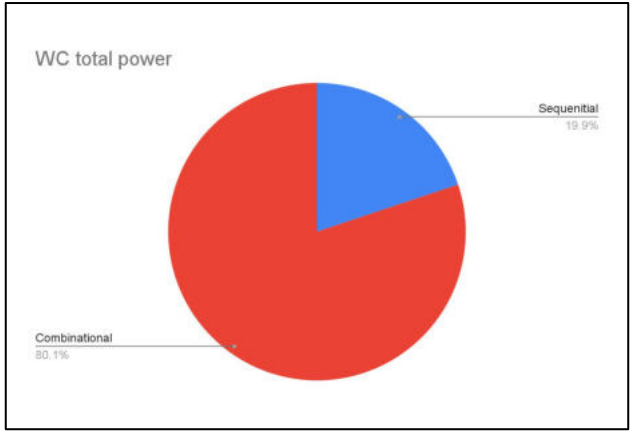
Tape Outs in Intel 16 - Power Numbers

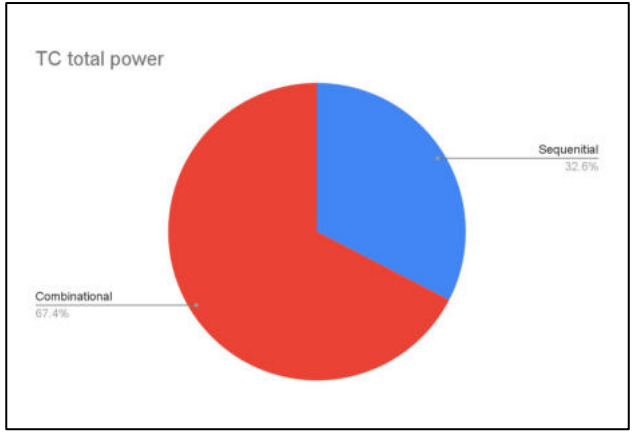




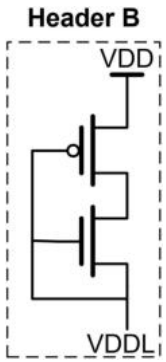




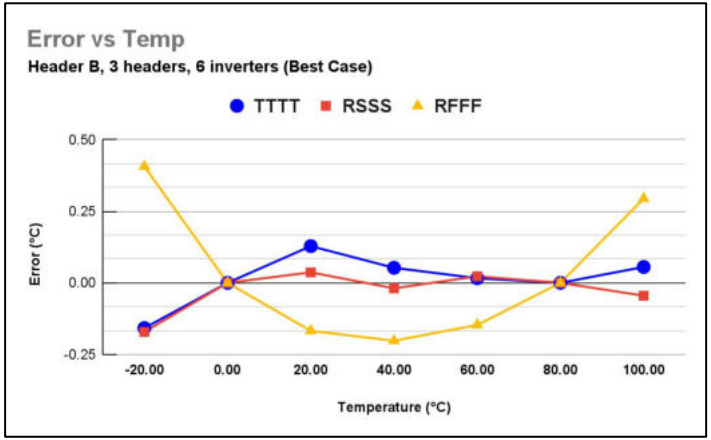


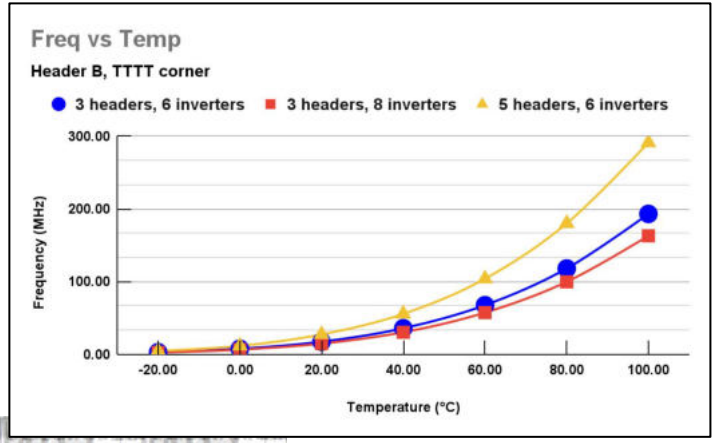


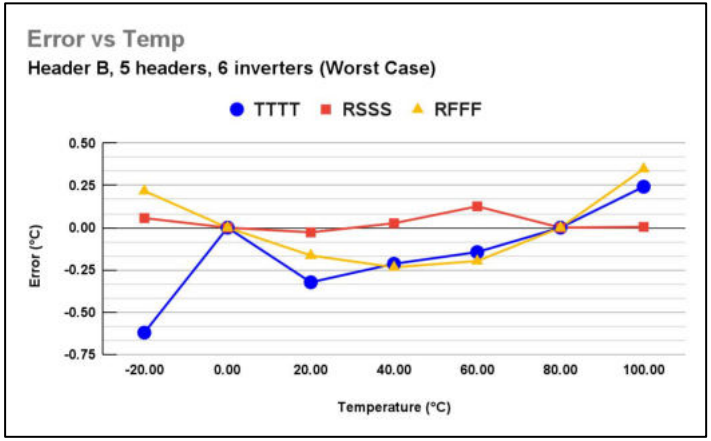
Temperature Sensor Variant B



Header B			
Corner	TTTT	RSSS	RFFF
T_{CONV} (ms)	0.1		
Energy/Conv (nJ)	1.40	0.28	6.81
$Error_{MAX}$ (°C)	0.62	0.17	0.41

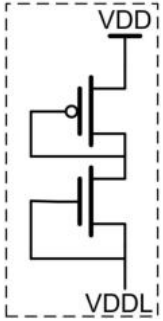




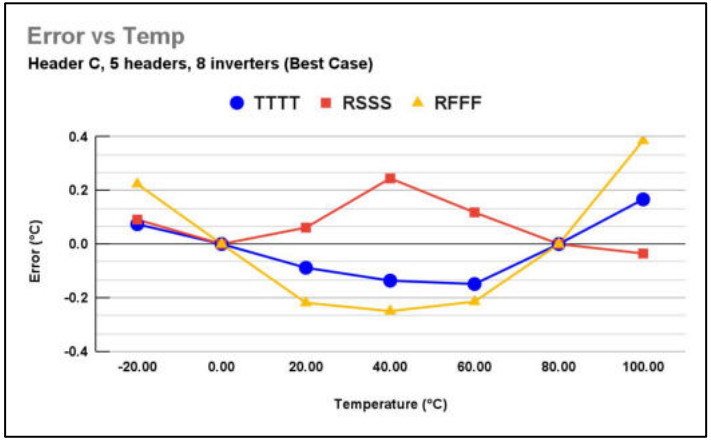


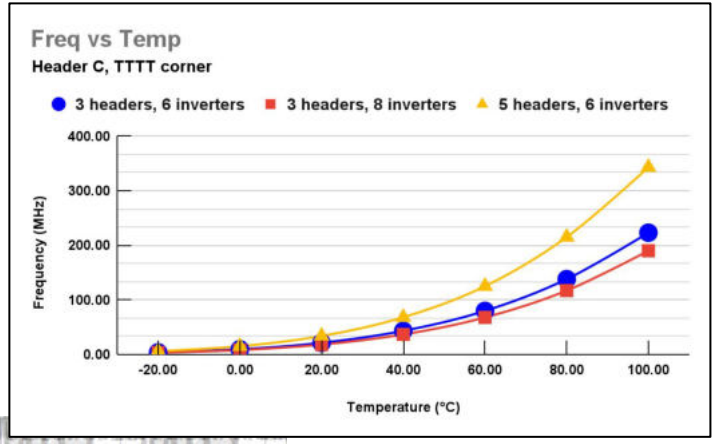
Temperature Sensor Variant C

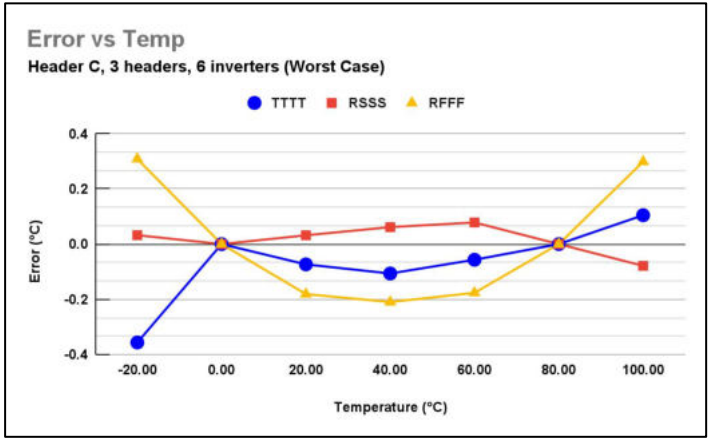
Header C



Header C			
Corner	TTTT	RSSS	RFFF
T_{CONV} (ms)	0.1		
Energy/Conv (nJ)	1.59	0.32	7.57
$Error_{MAX}$ (°C)	0.35	0.25	0.39





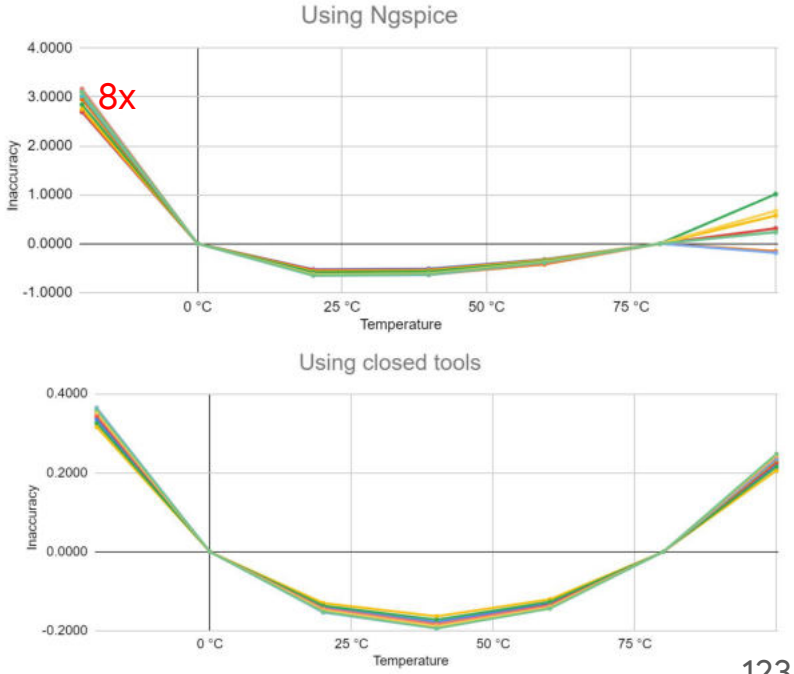


CHIPS Alliance AWG Activities
Techno/Design Loop
New Measured Data, Models, CI

Technology/Design Feedback Loop

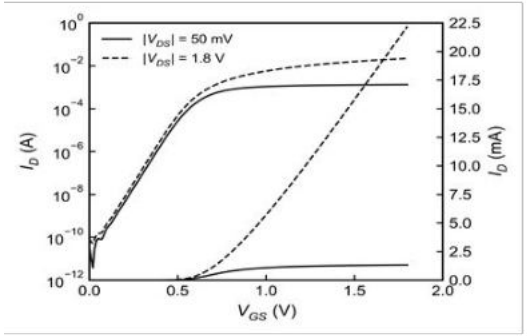
- Compatibility between open-source models versus closed models
- Quality of models (Both closed and Open-source)
- We have to define a Technology/Design feedback loop in the Open-source real

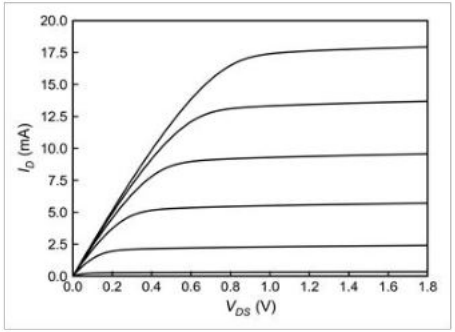
Discrepancies Closed vs Open-Source tools			
Frequency	**Power**	**VVDD**	**Inaccuracy**
-31.50%	539.63%	-0.82%	780.93%
-8.12%	181.81%	-0.85%	0.00%
-2.10%	106.59%	-1.58%	323.15%
-0.62%	87.81%	-1.78%	228.61%
-0.08%	82.38%	-1.70%	192.13%
-0.29%	80.25%	-1.09%	0.00%
-0.56%	79.70%	-0.72%	117.29%



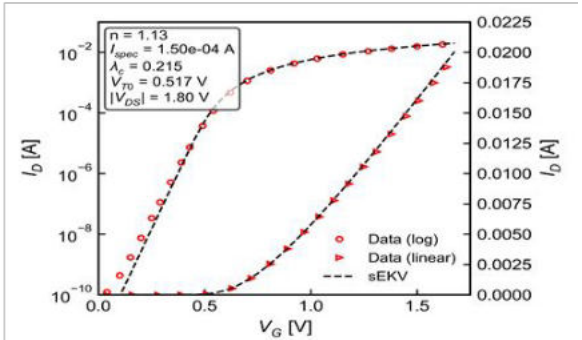
Preliminary Measurements on Skywater 130nm

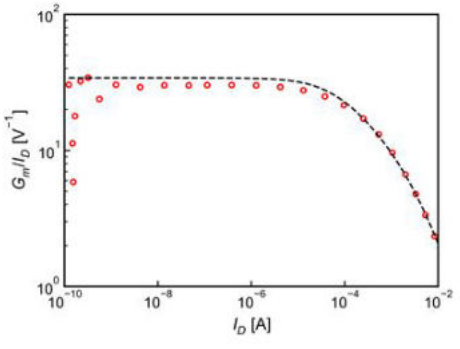
Long-channel NMOS Measurements

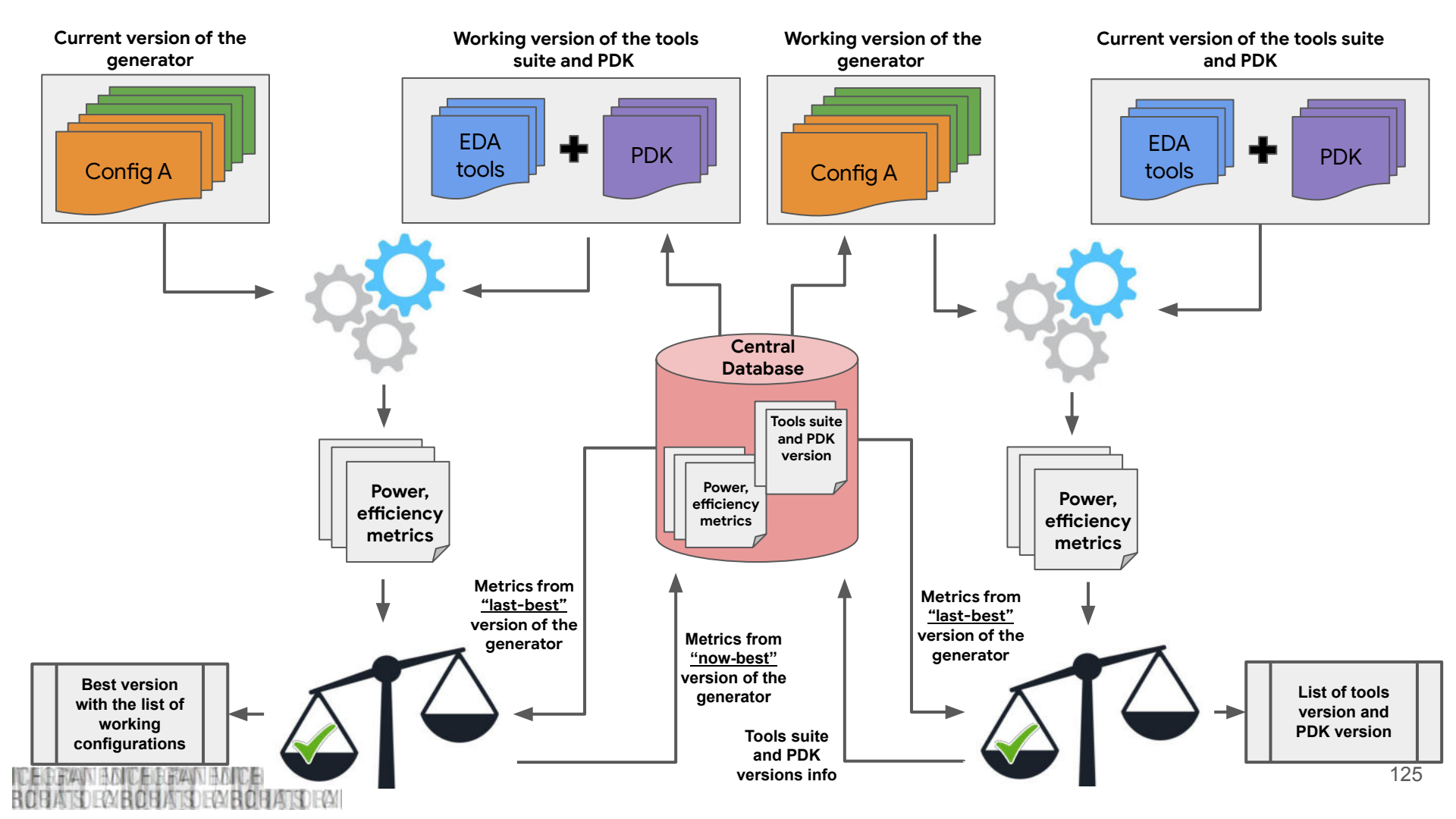


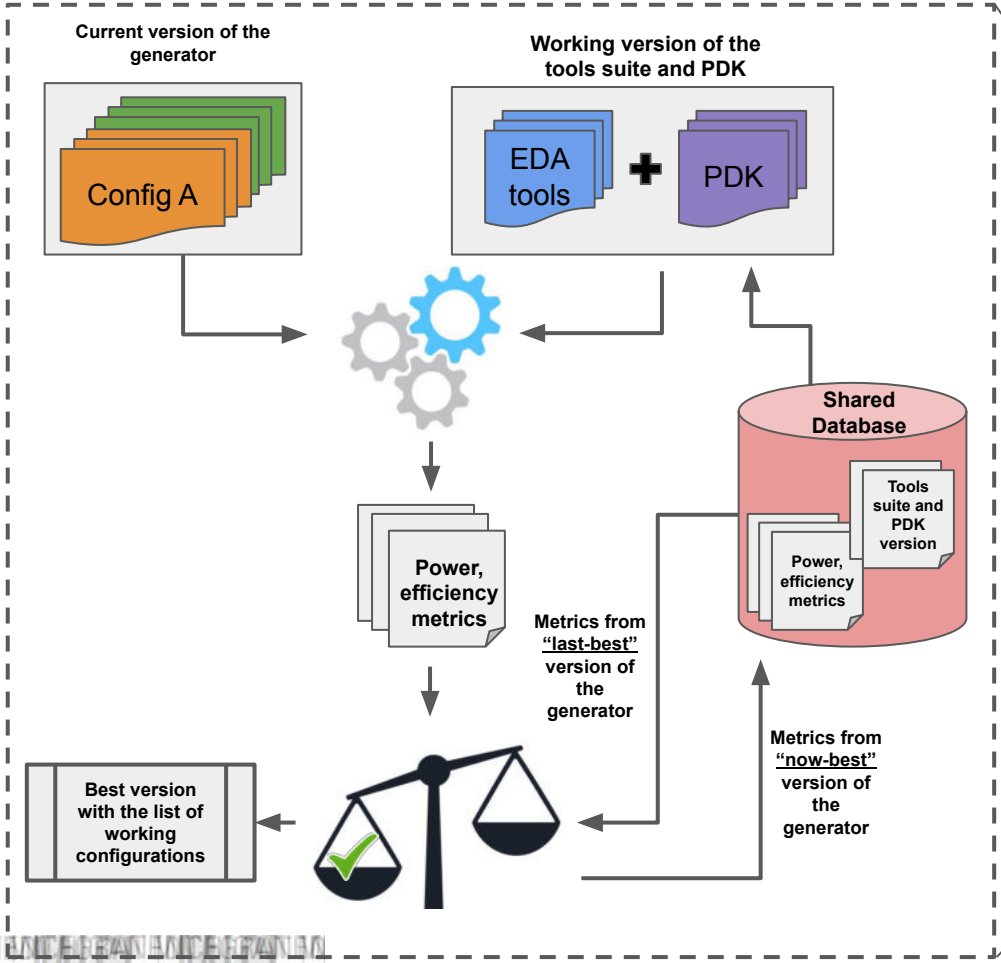


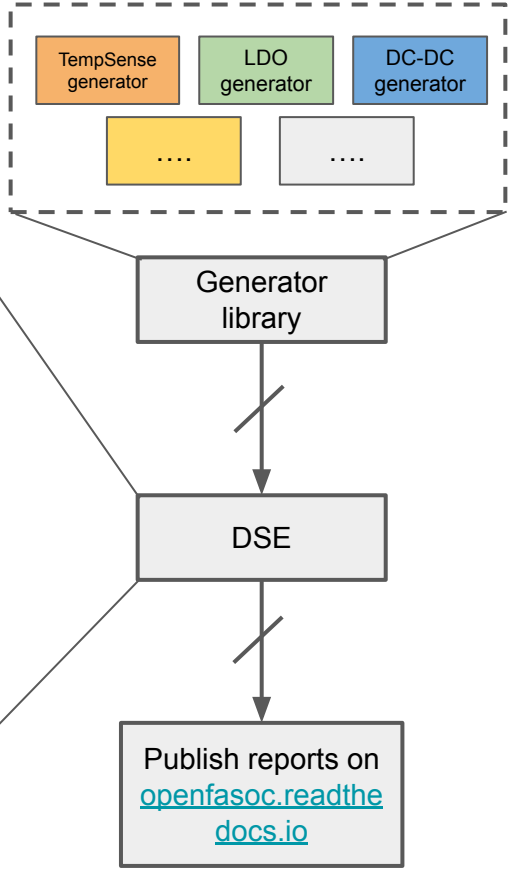
Long-channel NMOS sEKV Extraction/Model






Current version of the generator
Config A
Working version of the tools suite and PDK
EDA tools
PDK
Working version of the generator
Config A
Current version of the tools suite and PDK
EDA tools
PDK
Central Database
Tools suite and PDK version
Power, efficiency metrics
Power, efficiency metrics
Power, efficiency metrics
Metrics from "last-best" version of the generator
Metrics from "now-best" version of the generator
Metrics from "last-best" version of the generator
Tools suite and PDK versions info
Best version with the list of working configurations
List of tools version and PDK version


Current version of the generator
Config A
Working version of the tools suite and PDK
EDA tools
PDK
Shared Database
Tools suite and PDK version
Power, efficiency metrics
Power, efficiency metrics
Metrics from "last-best" version of the generator
Metrics from "now-best" version of the generator
Best version with the list of working configurations


TempSense generator
LDO generator
DC-DC generator
....
....
Generator library
DSE
Publish reports on openfasoc.readthedocs.io