# Accelerating Custom Integrated Circuit Design:
## Challenges, Innovations, and Open-Source Initiatives

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# Evolution of Software Dev

- Software Dev in the 90s
  - Vendor provided compiler
  - Toolchain incompatibilities
  - OS dependent

# Context and Background

- Software Dev in the 90s
  - Vendor provided compiler
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  - OS dependent

**Looks like current hardware dev!**

# Lowering Costs & Barriers to Chip Design

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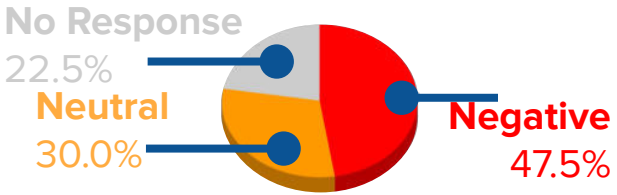


*Survey of ~ 50 Students*

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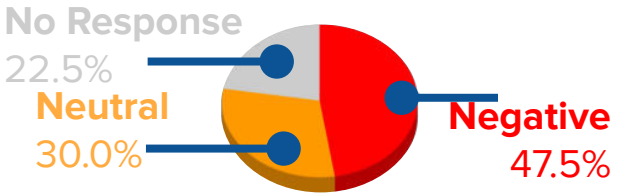


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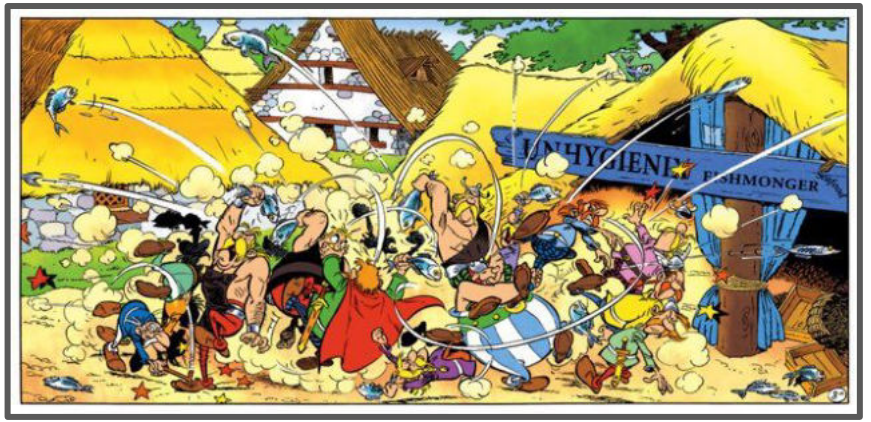

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**70 000 HW vs 830 000 SW Eng.**

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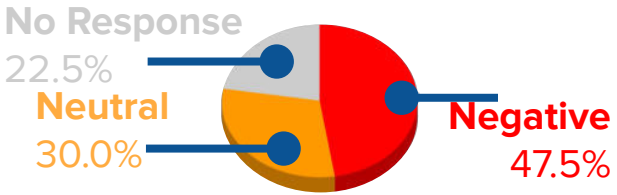


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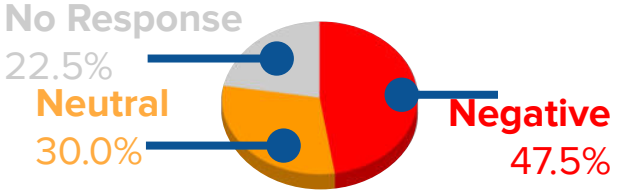


*Survey of ~ 50 Students*

## UG student Ali Hammoud to present his winning Code-a-Chip design at ISSCC 2023

*Catharine June • February 16, 2023*

ECE ELECTRICAL & COMPUTER ENGINEERING UNIVERSITY OF MICHIGAN

**Hammoud's project is based on the open-source hardware design tool called OpenFASoC, developed at Michigan.**

Ali Hammoud, a second-year student in computer engineering, is a winner in the inaugural international Code-a-Chip competition. He will present his project in open-source chip design at the 2023 International Solid-State Circuits Conference (ISSCC), along with 6 other design teams from around the world. His design is called OpenFASoC: Digital LDO Generator.

Hammoud's design is based on the open-source tool called OpenFASoC, short for Open-Source Fully Autonomous System-on-Chip, which was co-developed by his faculty advisor on the project, Dr. Mehdi Saligane. OpenFASoC was developed for analog circuit design, which is more difficult to automate than digital circuit design.

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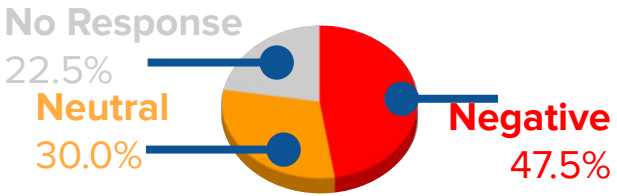


*Survey of ~ 50 Students*

| **Hardware** @ Google | **Software** @ Google |
|---|---|
| New deploy 18 months | Push once a week |
| New Deploy 18 months | Normal Push 4-6 hours |
| All Replaced ~6 years | Emergency Push <1 hours |
| ~4 versions deployed | ~1 version deployed |

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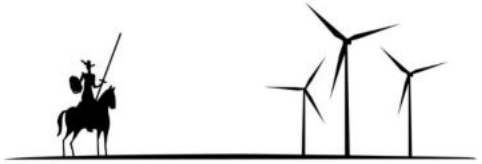
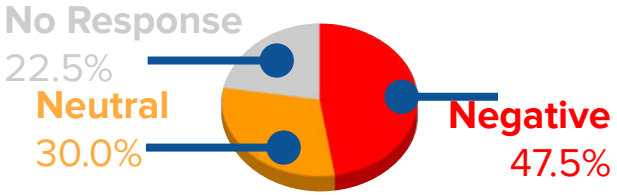


**Is Hardware Development Broken?**

***Describe your experience with (tapeout) toolchain in one word***

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# Lowering Costs & Barriers to Chip Design

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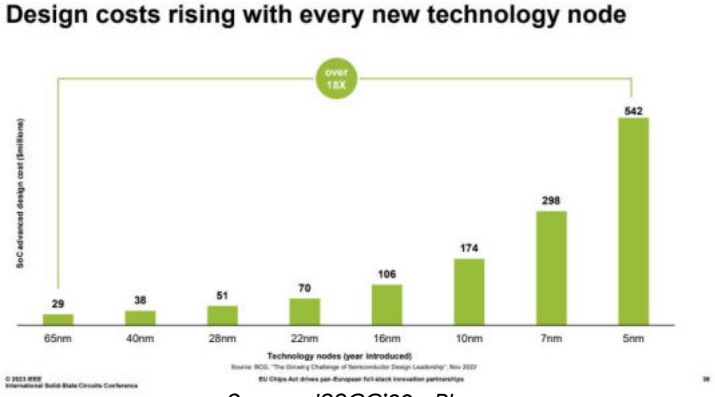



*Source: ISSCC'23 - Plenary*

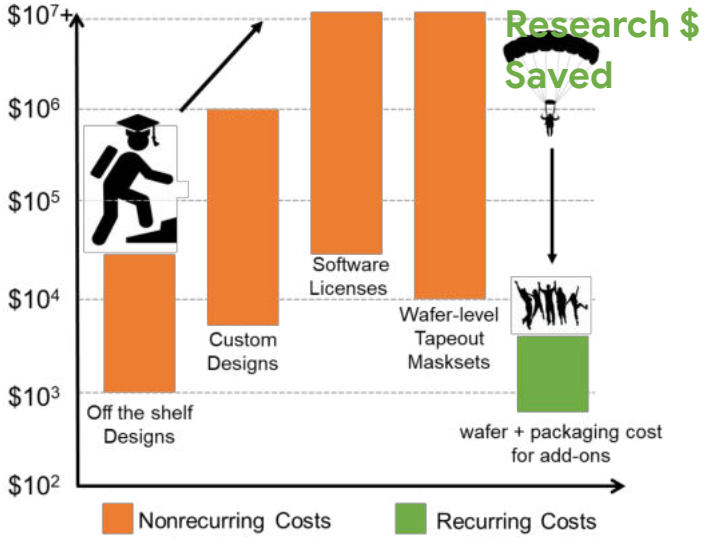
**The Missing Pieces of Open Design Enablement: A Recent History of Google Efforts**

Invited Paper

Tim Ansell
tansell@google.com
Google
Mountain View, California

Mehdi Saligane
mehdi@umich.edu
University of Michigan
Ann Arbor, Michigan

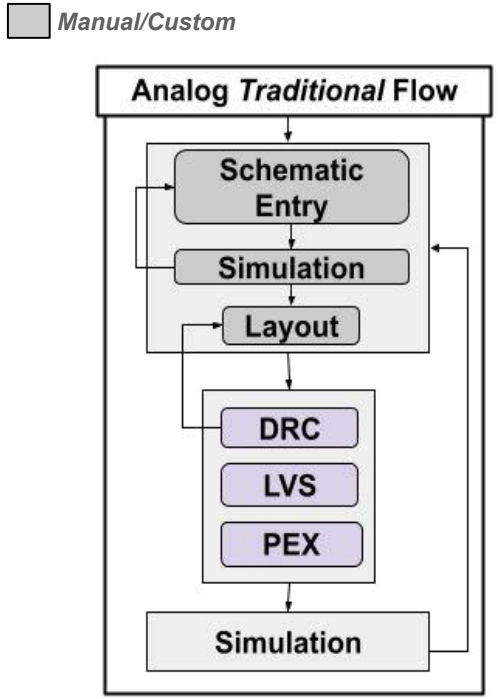
- *T. Ansell and M. Saligane, "The Missing Pieces of Open Design Enablement: A Recent History of Google Efforts : Invited Paper," 2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD), San Diego, CA, USA, 2020.*




*Source: NIST*

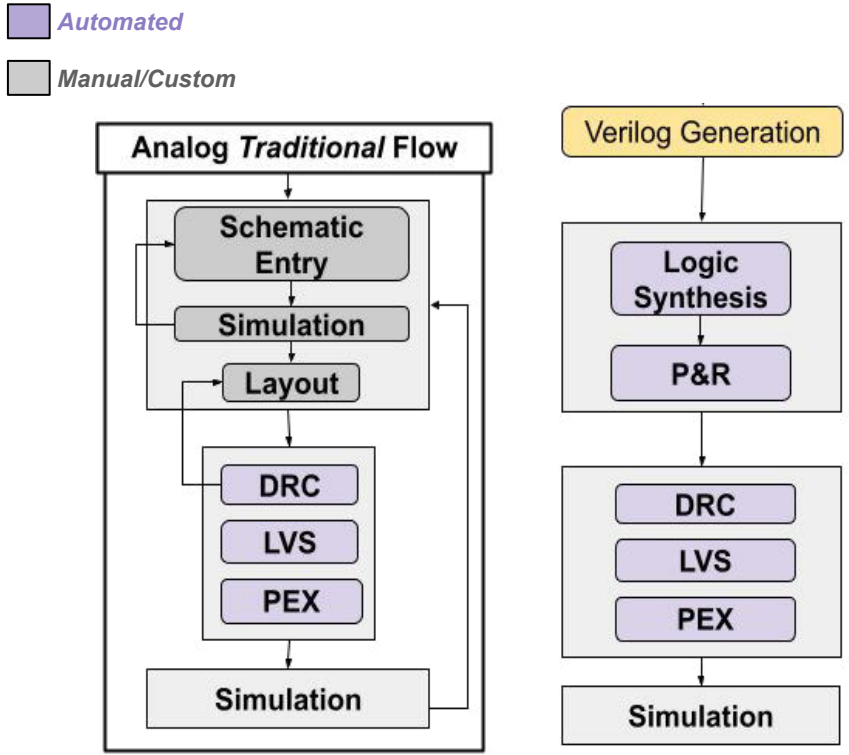
# Traditional vs Automated Analog Design

# Analog design flow




- **Analog** design flow
  *Significant number of **manual** and custom steps.*

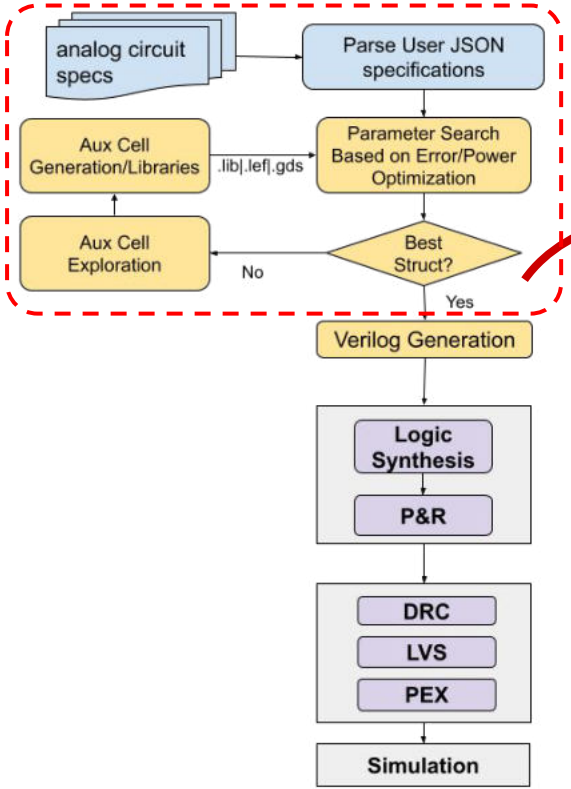
# Analog vs. Digital design flow




- **Analog** design flow
  *Significant number of **manual** and custom steps.*
- **Digital** design (*grid-based*) flow
  *Almost **entirely automated**.*

# Generated Analog *into* Digital design flow

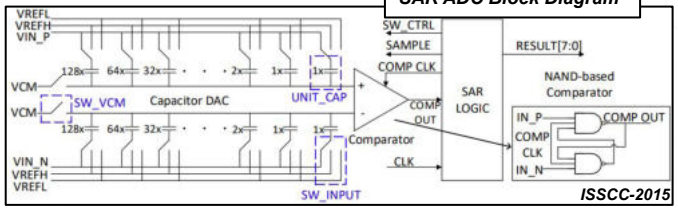
**FASoC Generator**



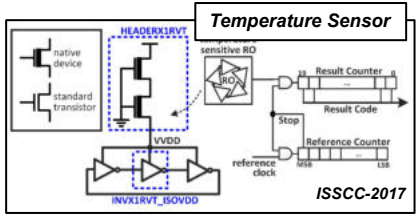

*Automated*

*Manual/Custom*

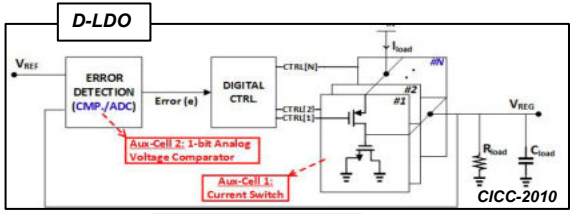
**SAR ADC Block Diagram**



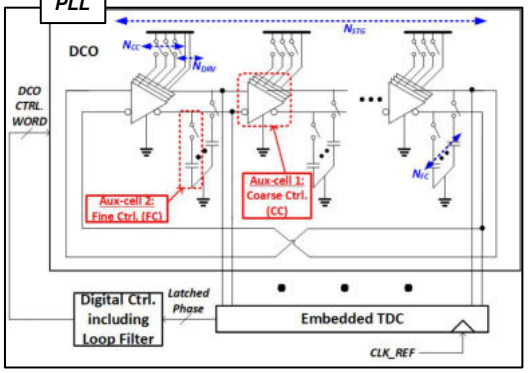

**Temperature Sensor**



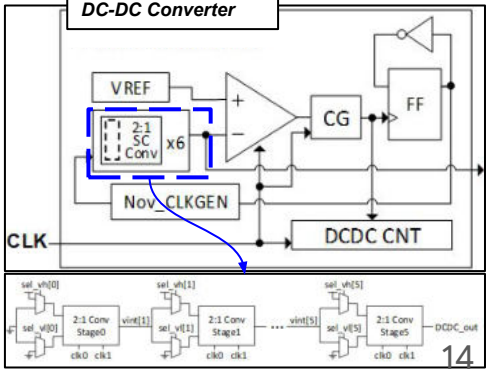

**D-LDO**




**PLL**




**DC-DC Converter**



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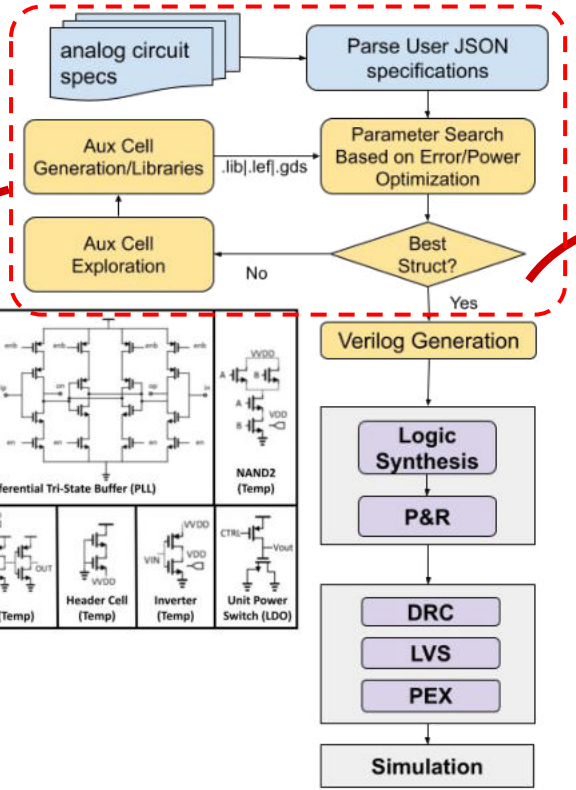





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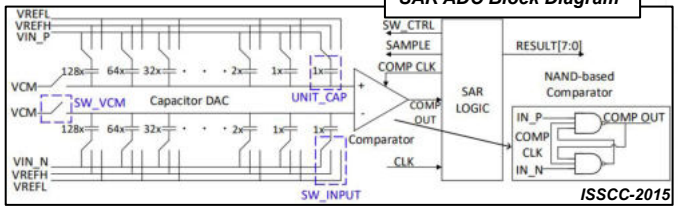


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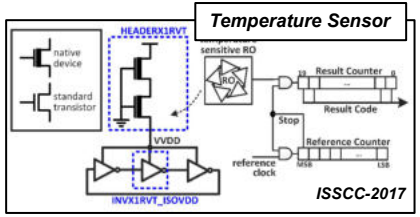


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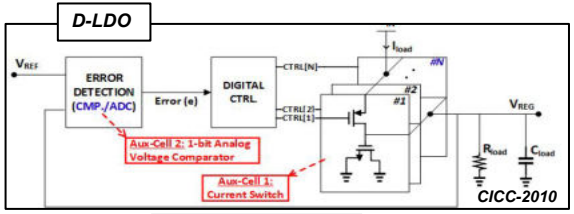


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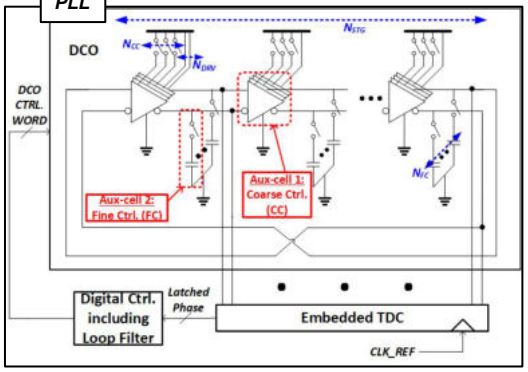


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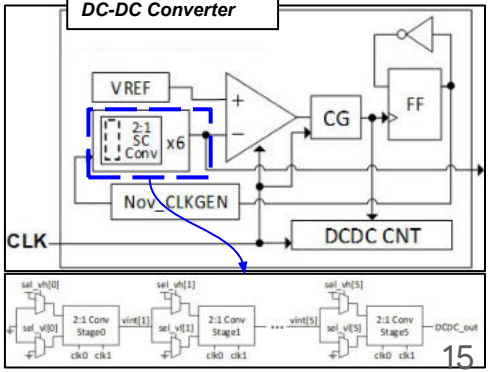

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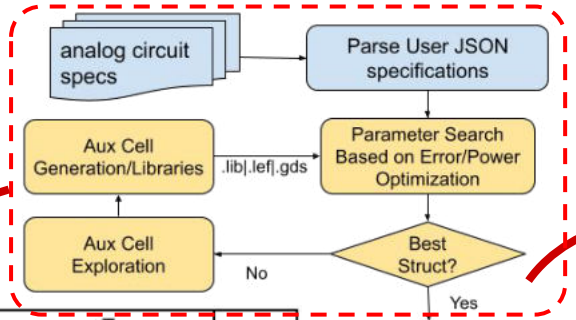
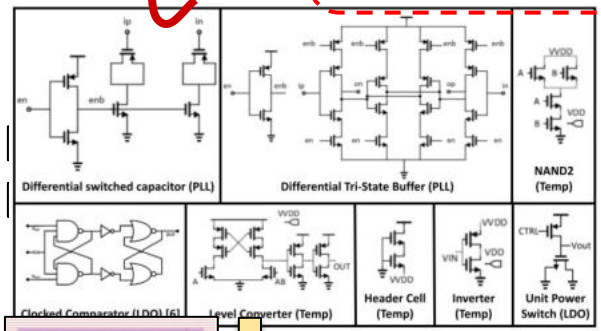
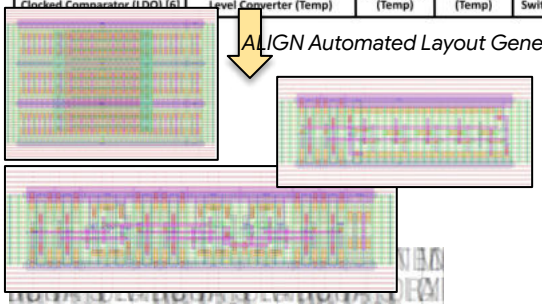



*ALIGN Automated Layout Generator*



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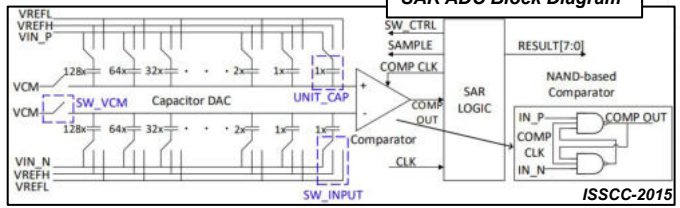
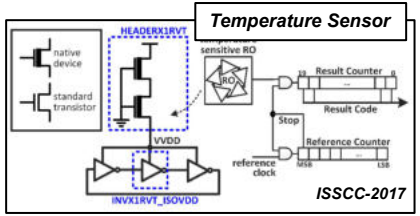


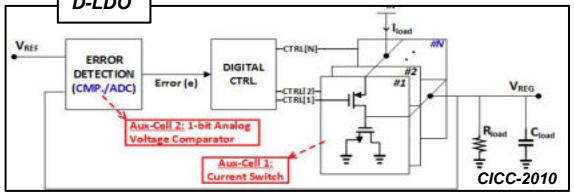

ISSCC-2015

**Temperature Sensor**



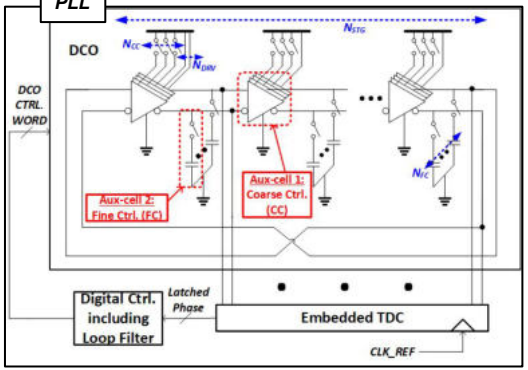

ISSCC-2017

**D-LDO**




CICC-2010

**PLL**

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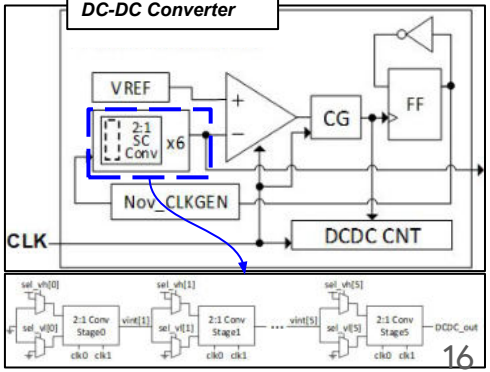
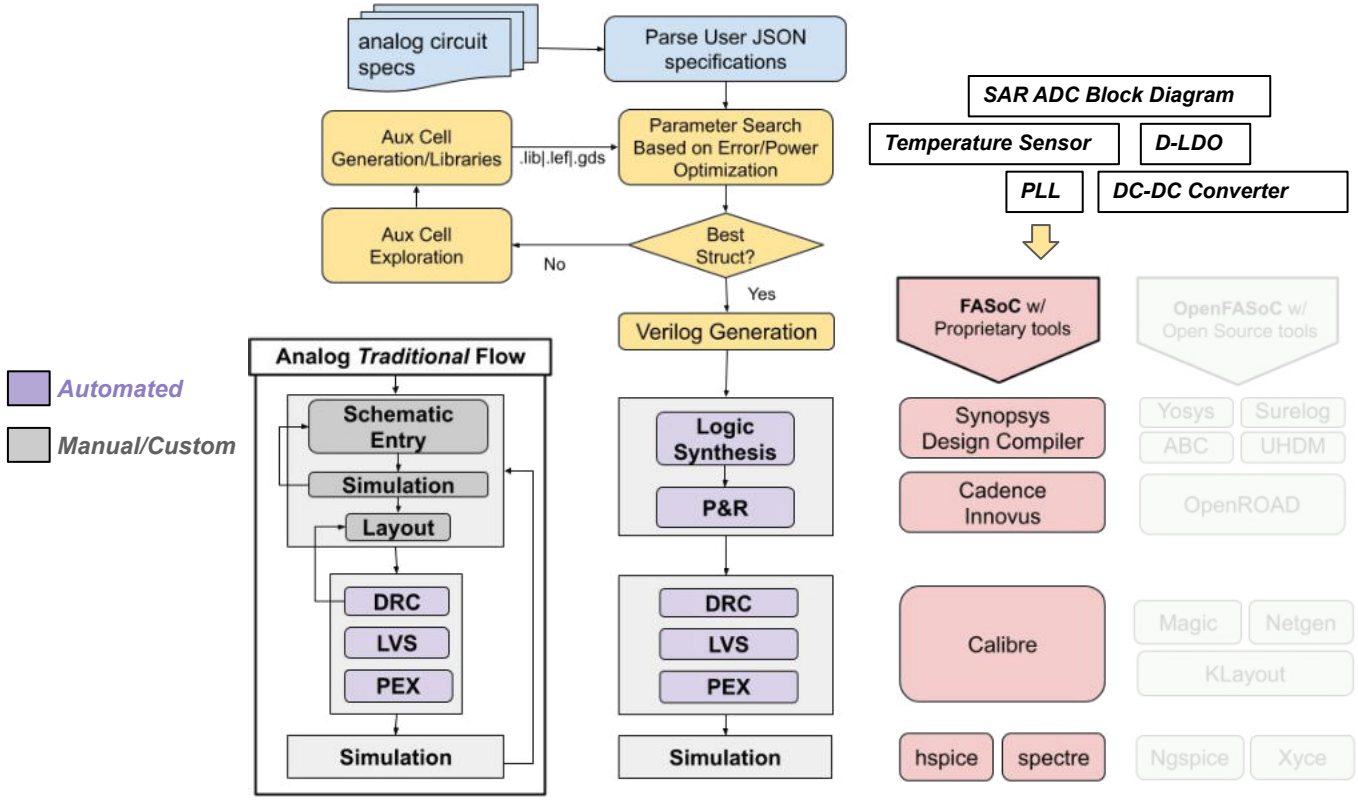
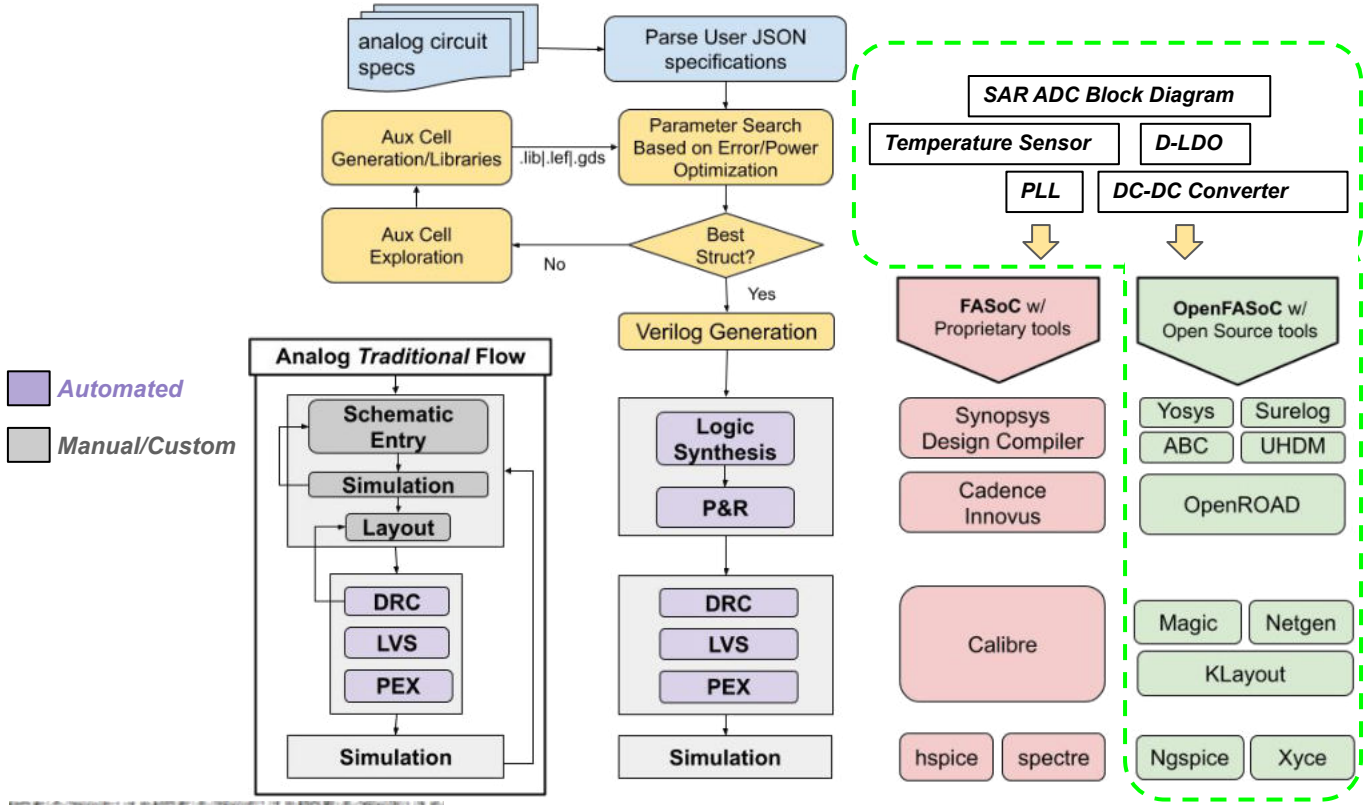


# Initially only **proprietary** design flow



# Now proprietary *or* open source design flow




**OpenFASoC!**

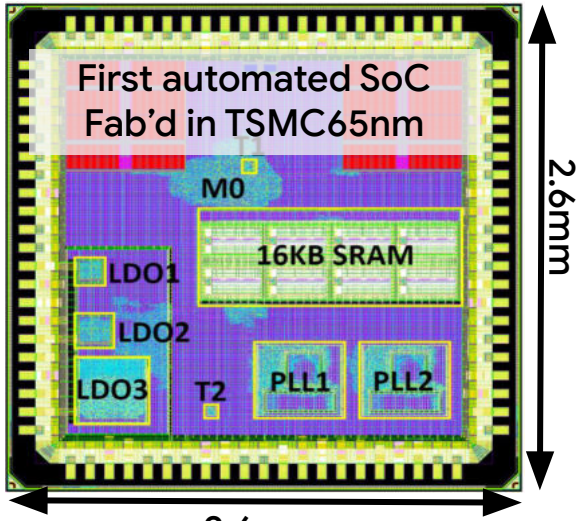
Automated **portable** analog

# Overview of FASOC

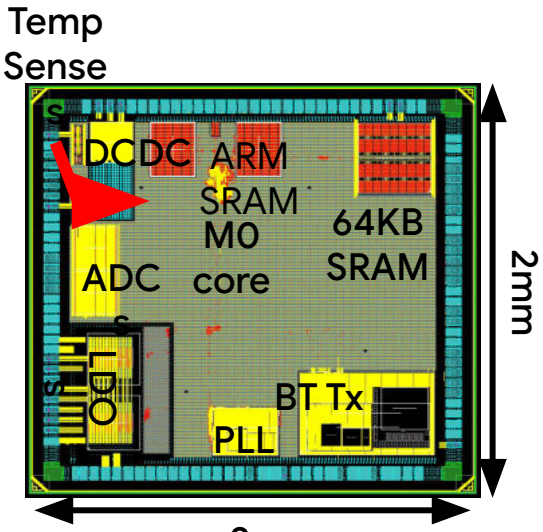
Fully Autonomous SoC Synthesis

- DARPA IDEA Program (OpenROAD and FASoC)
- Multi-University and Industry effort
- Multiple tape-outs in TSMC 65, GF12LP, SkyWater 130nm

https://fasoc.engin.umich.edu/




TSMC65LP SoC (2019-08)

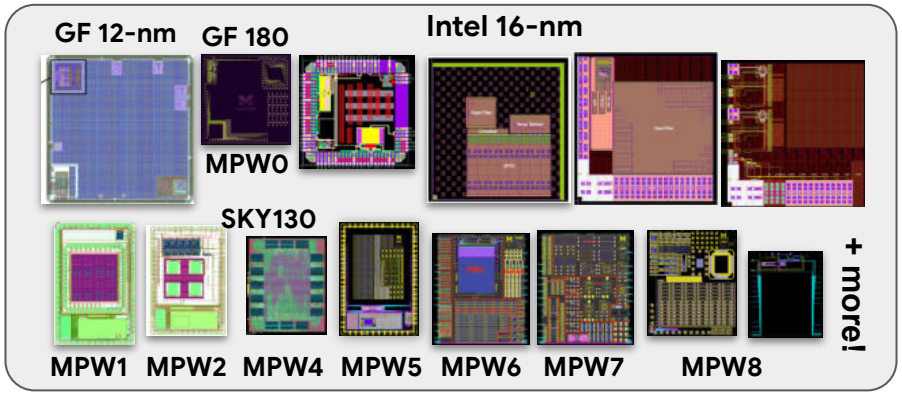



GF12LP SoC (2020-10)

# Overview of OpenFASOC Today

## Fully Autonomous SoC Synthesis

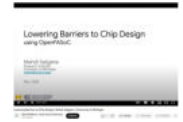
- DARPA IDEA Program, now funded by Google, NIST and others
- Multiple tape-outs in TSMC 65, GF12LP, SKY130, GF180MCU, Intel 16




**<3 years, <10 people!**

openfasoc.readthedocs.io

[CHIPS Alliance Workshop 2021-11]



[OpenPOWER AI Workshop IBM - 2022-11]

[CHIPS Alliance Technology Update 2022-12]

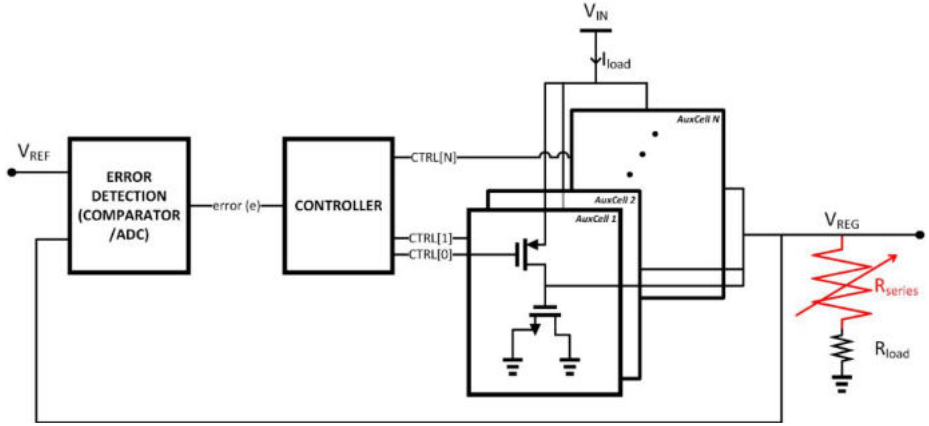
[RISCV Alliance Japan 2022-12]

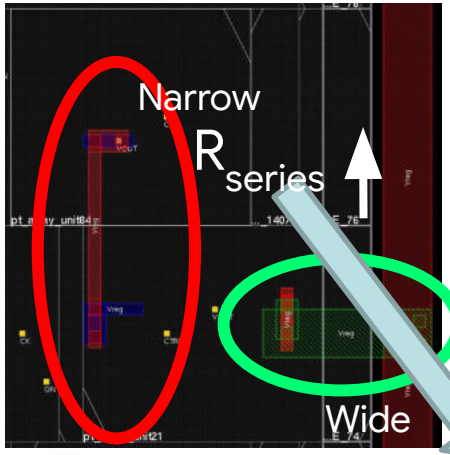
# Trade-offs & Design Constraints Examples

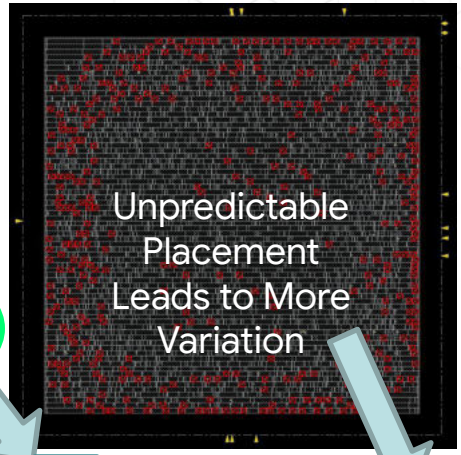
# D-LDO Power Routing Example

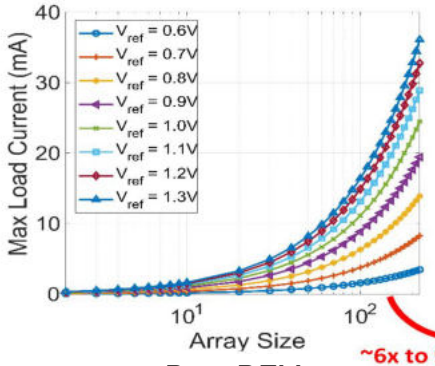
Performance loss caused by PnR

- Large Series Resistance caused by wiring congestion for increased array size
- Unpredictable wiring due to random placement of power cells



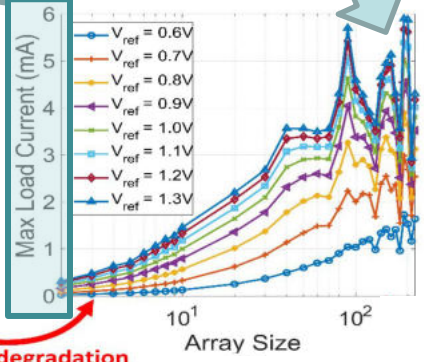




Pre-PEX

~6x to 9x degradation




Post-PEX

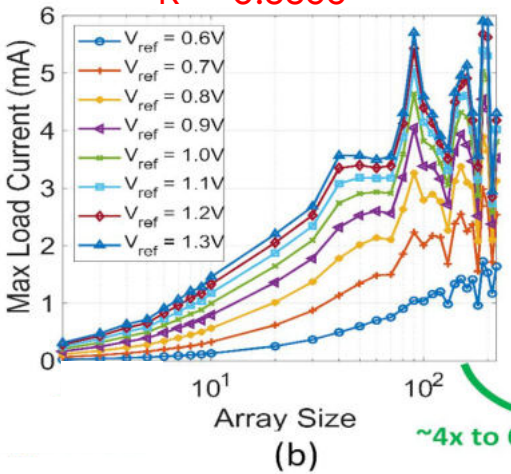
# D-LDO Power Routing Example

Constraints to improve performance

- Technology agnostic fencing to constraint placements
- Use power stripes to improve series R problem
- Automatic analysis of technology database file for determining the stripe metal layers
- Taped out in BiCMOS and bulk 130nm, TSMC 65LP and GF12LP

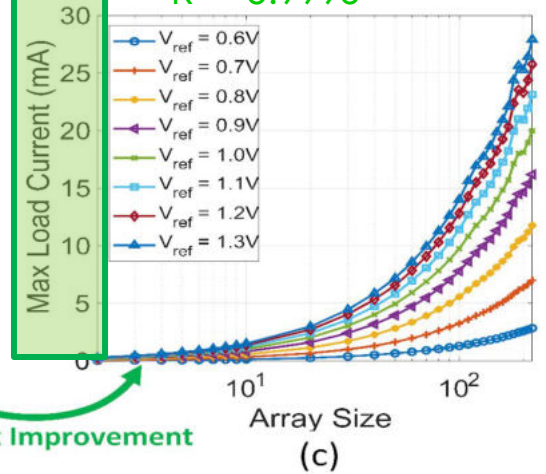
Constraint less Post-PEX

$R^2$ = 0.8865

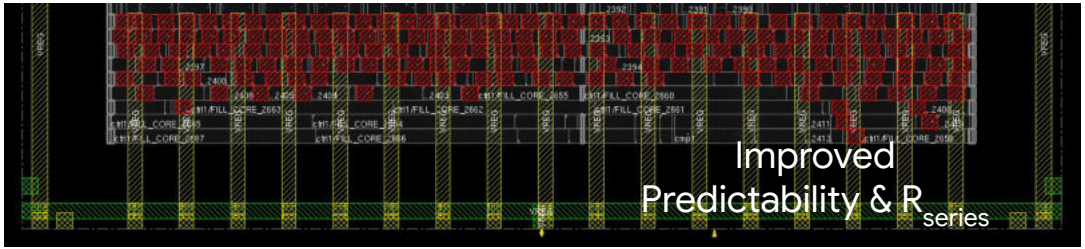



Scalable Constraint Post-PEX

$R^2$ = 0.9993

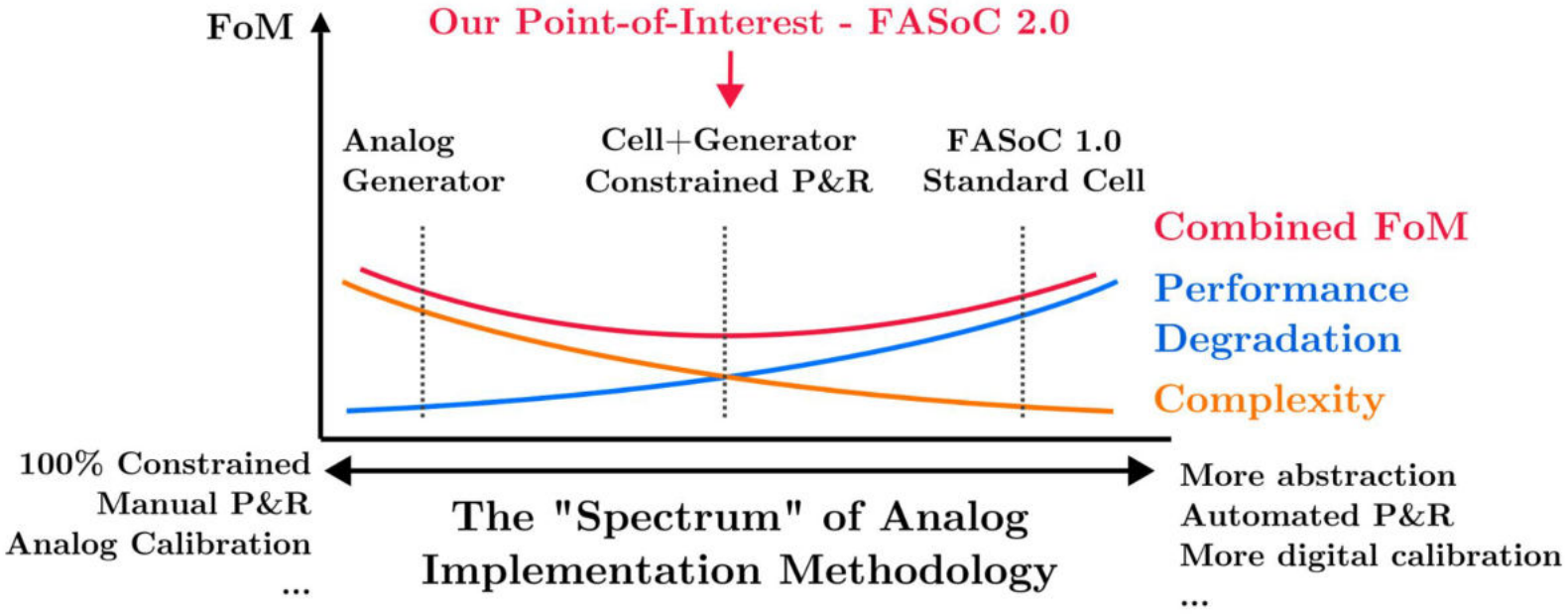



~4x to 6x Improvement



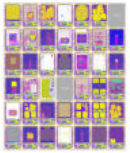
# Performance / Complexity Tradeoff

- FASoC augments digital flow with APR tool placement/routing constraints and minimizes the (performance loss * complexity)



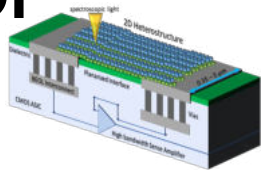
# On-Going Projects & Contributions

## Open-Source IC & tapeouts



- ➔ 1st *Open* Silicon Results

## NIST Nanofabrication Accelerator



- ➔ 1st *Open* Nanotechnology Platform
- ➔ Cryogenic CMOS

## Low-Power IC Design

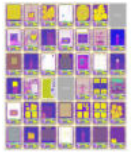
- ➔ ***Rapid*** Prototyping for Wearables

## Hardware Security

- ➔ 1st *Open* Root of Trust SoC

# On-Going Projects & Contributions

## Open-Source IC & tapeouts



➔ 1st *Open* Silicon Results

## NIST Nanofabrication Accelerator



➔ 1st *Open* Nanotechnology Platform

➔ Cryogenic CMOS

## Low-Power IC Design



➔ *Rapid* Prototyping for Wearables

## Hardware Security



➔ 1st *Open* Root of Trust SoC

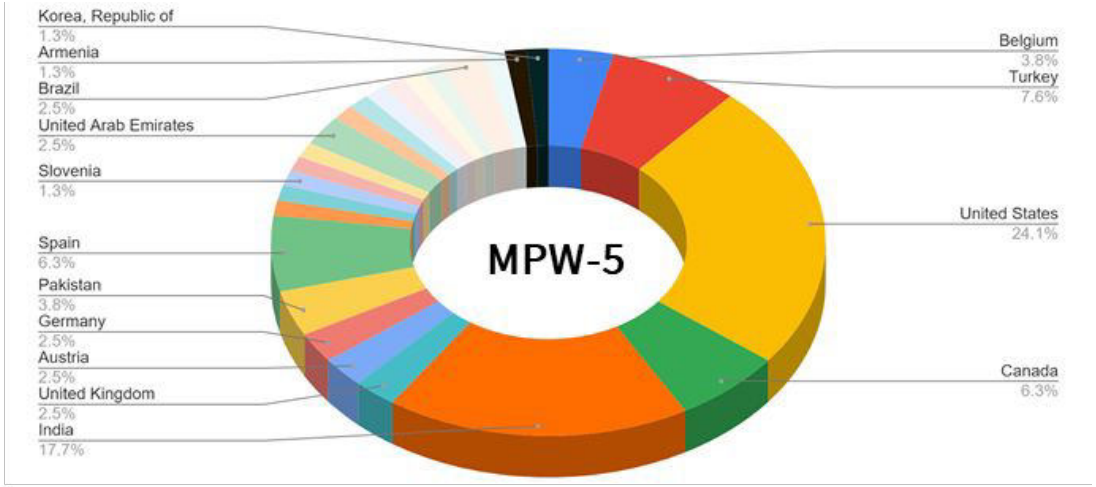
# Big-Bang Events: Open-Source PDKs

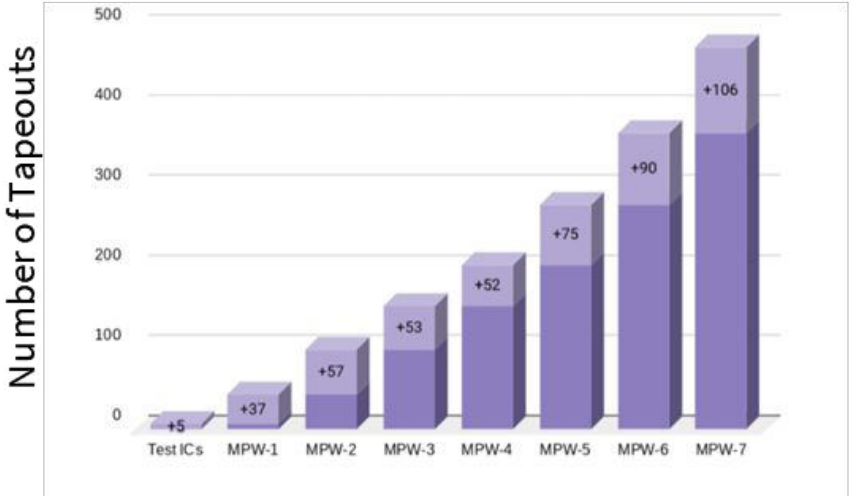
- First open-source PDK (November 2020)
  - SkyWater 130nm CMOS
  - https://github.com/google/skywater-pdk
- Second open-source PDK (October 2022)
  - GlobalFoundries 180nm MCU
  - https://github.com/google/gf180mcu-pdk
- Third open-source PDK (March 2023)
  - IHP 130nm BiCMOS
  - https://github.com/IHP-GmbH/IHP-Open-PDK



- Permissive Apache 2.0 licensing

# Efabless Caravel “Harness” SoC

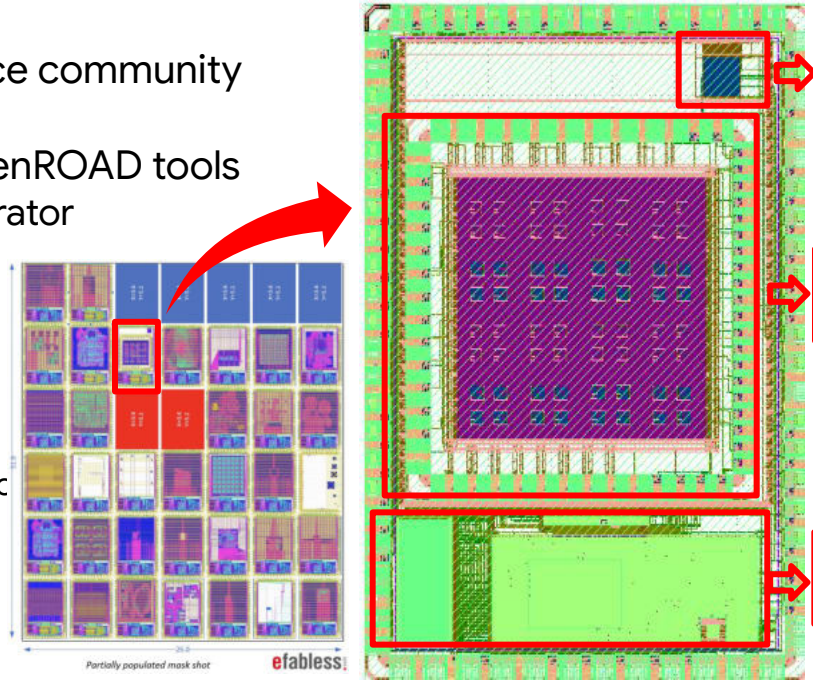



# OpenFASOC Demonstrator

## MPW-I: 64 sensors + D-LDO

- Actively contributing to the open source community
- 1st open FASoC flow built on top of OpenROAD tools
  - Focused on the Temp. Sensor Generator
- FASoC testchip in SKY130:
  - Includes Caravel SoC
  - 64 Temp. Sensor Mesh
  - LDO ported (~ a week)
    - Updated strongArm latch comparato
    - 5v native NMOS switch



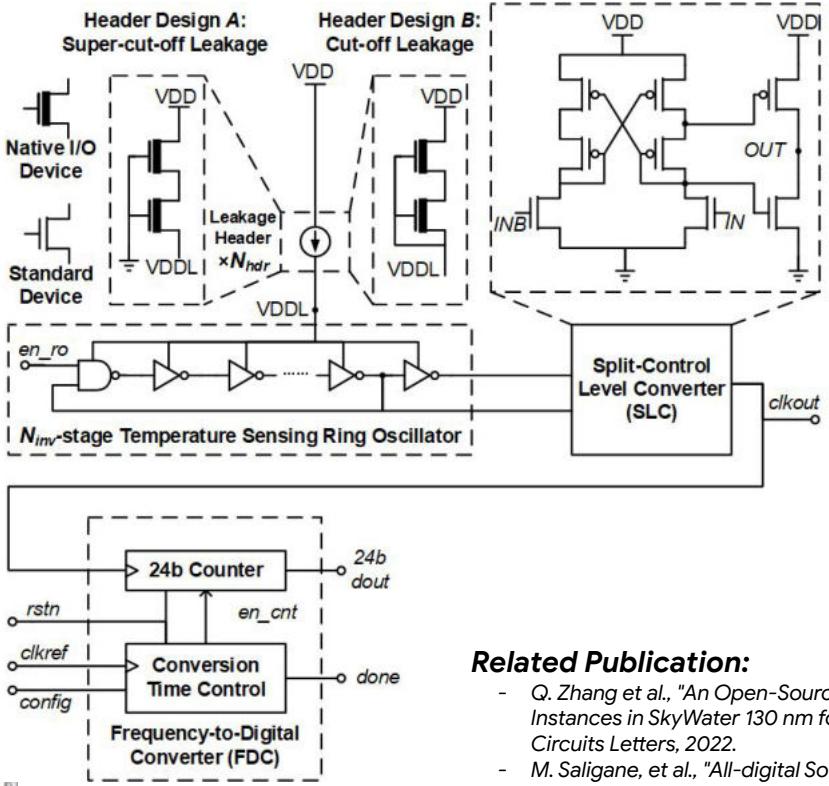

*Test-chip in MPW-I*

Open MPW Shuttle Program

efabless Sponsored by Google

# Temperature Sensor Topology

- Temperature Sensor Template Design

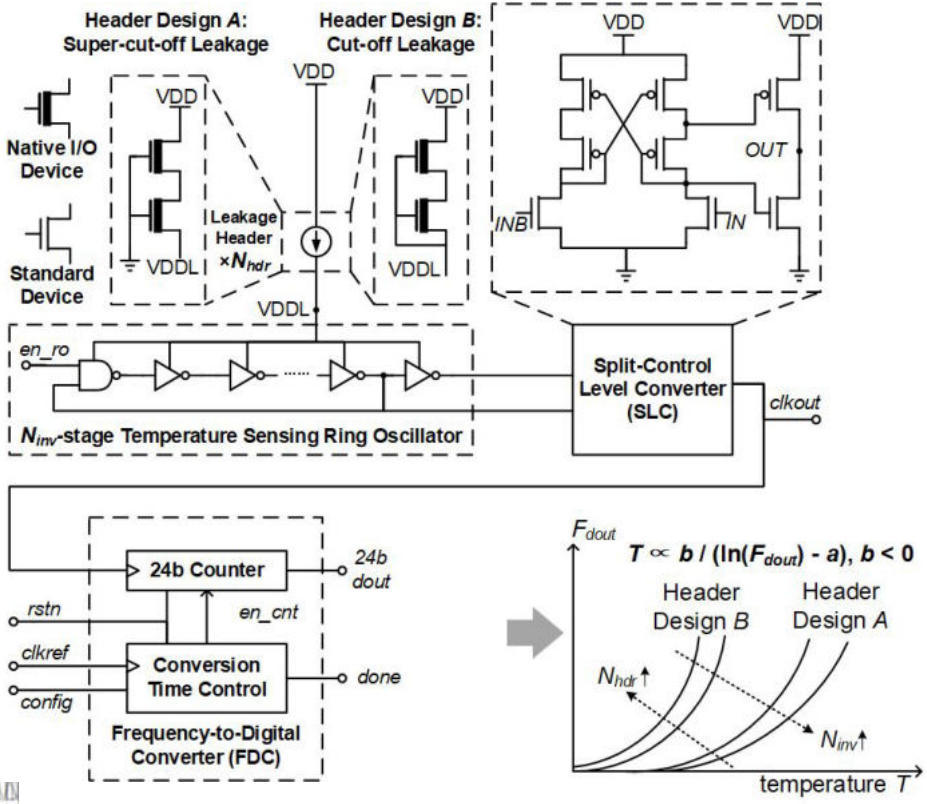



***Related Publication:***

- *Q. Zhang et al., "An Open-Source and Autonomous Temperature Sensor Generator Verified With 64 Instances in SkyWater 130 nm for Comprehensive Design Space Exploration," in IEEE Solid-State Circuits Letters, 2022.*
- *M. Saligane, et al., "All-digital SoC thermal sensor using on-chip high order temperature curvature correction," 2015 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, USA, 2015*

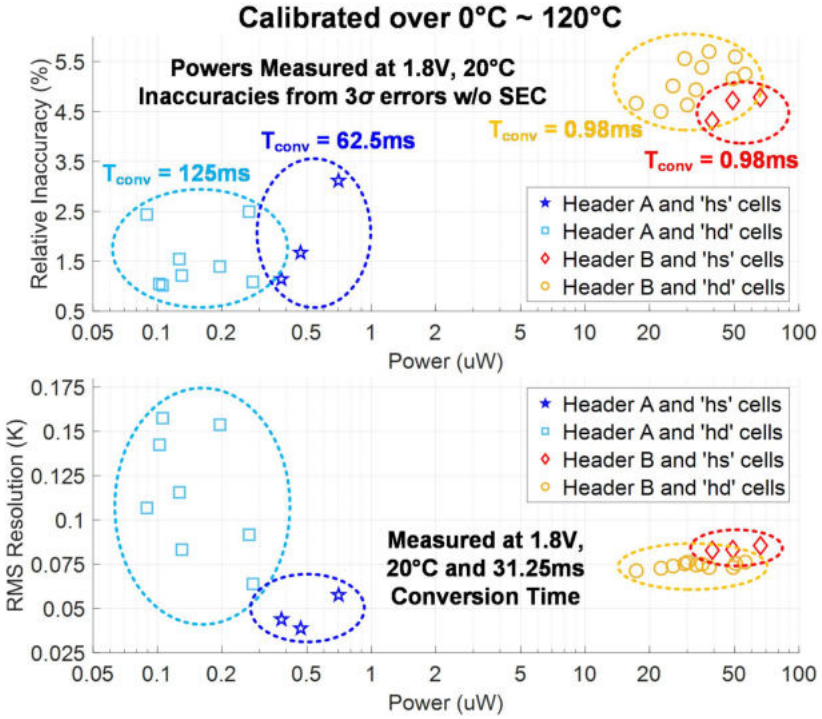
# Temperature Sensor Topology

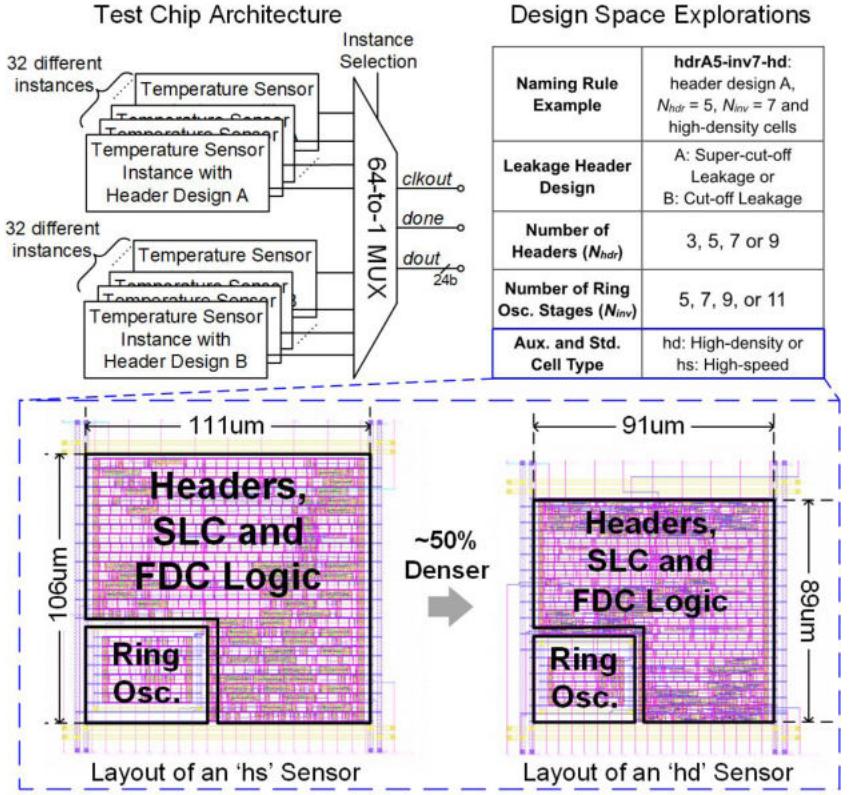
- Temperature Sensor Template Design



# Measurement Results

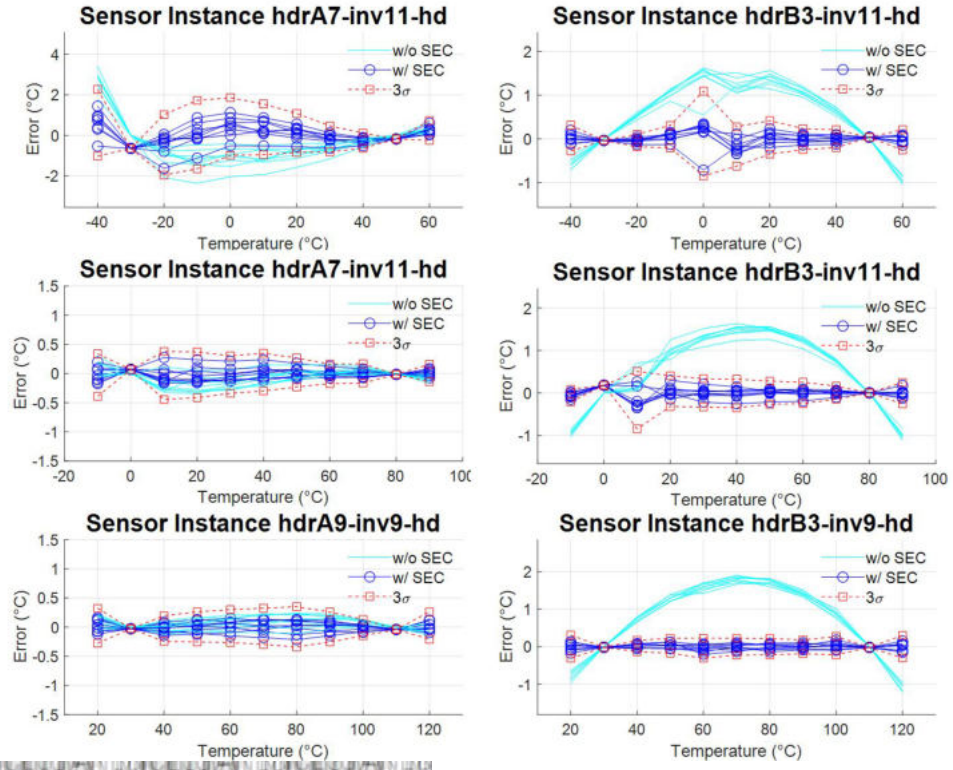
- 64 sensors array used for low-cost design space exploration

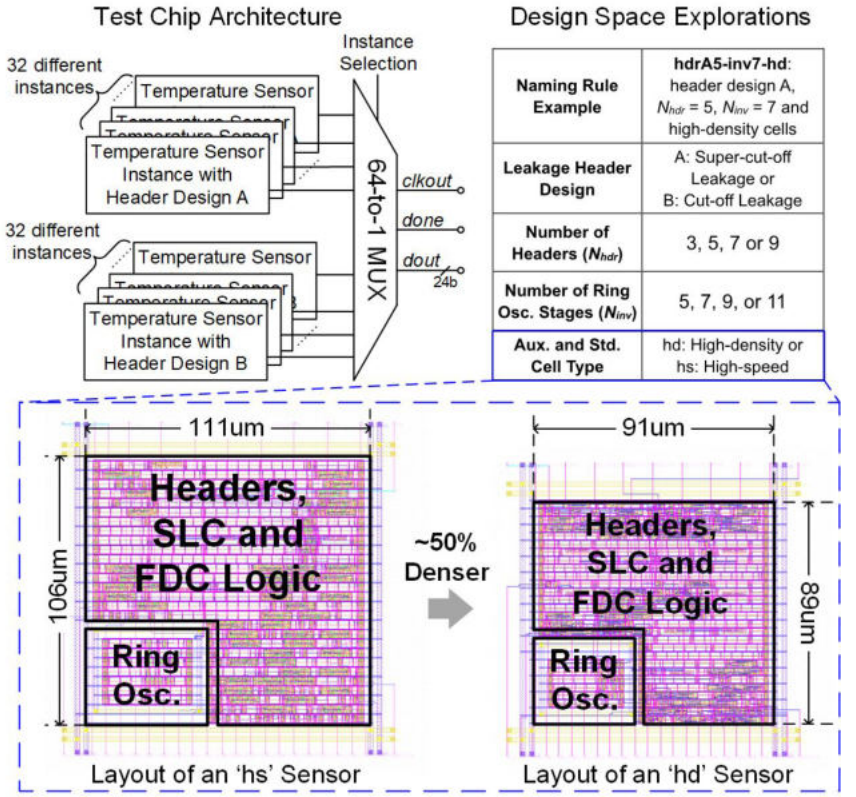


# Measurement Results

- Below 1 °C inaccuracy and SOTA results

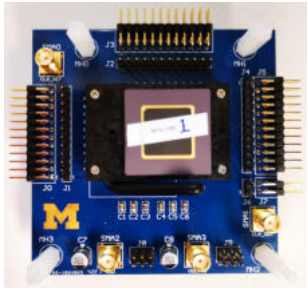


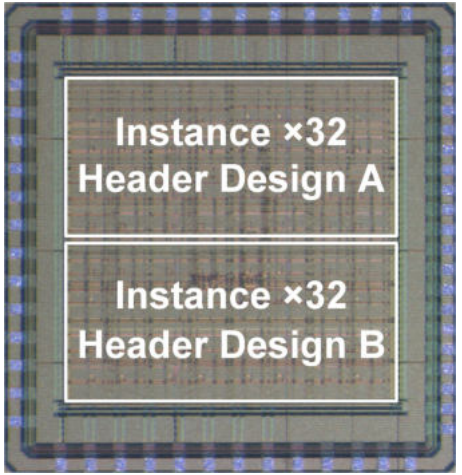



# Summary Results

- ***Only*** working Chip from MPW-I using ***Open*** Tools
- Published at the Solid-State Circuits Letters!

| | This Work | | | JSSC '20 [5] | JSSC '19 [6] | CICC '18 [7] | ISSCC '17 [4] |
|---|---|---|---|---|---|---|---|
| | B3-hd-11 | A9-hd-7 | A7-hd-9 | | | | |
| Technology | SkyWater 130nm (Open-source PDK) | | | 55nm | 65nm | 180nm | 180nm |
| Generator-based Design | Yes | | | No | No | No | No |
| Supply Voltage (V) | 1.8V | | | 0.8 ~ 1.3 | 0.5 | 0.8 ~ 1.4 | 1.2 |
| Area ($\mu m^2$) | 8095 | | | 1770 | 630000 | 65000 | 8865 |
| Temperature Range (°C) | -40 ~ 80 | -20 ~ 100 | 0 ~ 120 | -40 ~ 125 | 0 ~ 100 | -20 ~ 80 | -20 ~ 100 |
| Conversion Time (ms) | 0.98 | 125 | 125 | 1.31 | 300 | 840 | 8 |
| Inaccuracy (°C) | -0.97/1.08 3σ | -0.59/0.61 3σ | -0.67/0.74 3σ | -0.7/0.7 3σ | -1.53/1.61 Min./Max. | -0.7/+1.3 Min./Max. | -0.22/0.19 3σ |
| Relative Inaccuracy | 1.71% | 1.00% | 1.18% | 0.85% | 3.14% | 2.00% | 0.35% |
| Power (μW) | 17.33 | 0.25 | 0.13 | 9.3 | 0.000763 | 0.0013 | 0.075 |
| Energy/Conv. (nJ) | 16.92 | 31.38 | 16.25 | 12.2 | 0.23 | 11 | 0.6 |
| Resolution (mK) | 78 | 21 | 24 | 16 | 300 | 110 | 73 |
| Resolution-FoM ($pJ \cdot K^2$) | 101.9 | 13.4 | 9.7 | 3.1 | 20.7 | 140 | 3.2 |

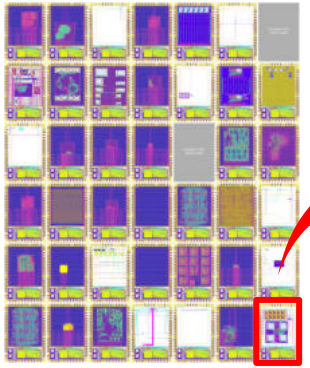


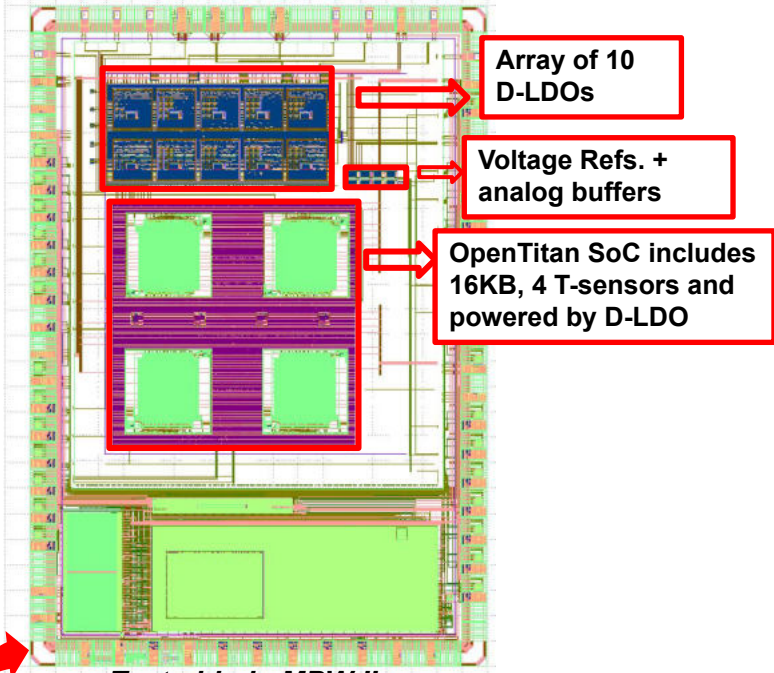


# OpenFASOC on MPW-II:
## 1st Open Source AMS SoC

- Included initial support for voltage domains in OpenROAD
- Implementation of the OpenTitan SoC using an ECO flow to fix hold timing with degrading the $F_{MAX}$
- Temperature Sensor generator is using an end-to-end Open Source flow
- Updates to the D-LDO generator:
  - Embedded voltage references
  - Decap cells using MIM cap.
  - Multiple implementations and $I_{LOAD}$

- https://efabless.com/projects/239
- https://github.com/msaligane/caravan_openfasoc.git





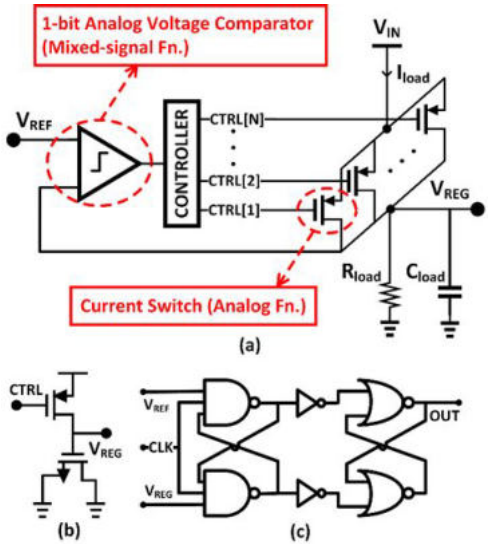

*Test-chip in MPW-II*

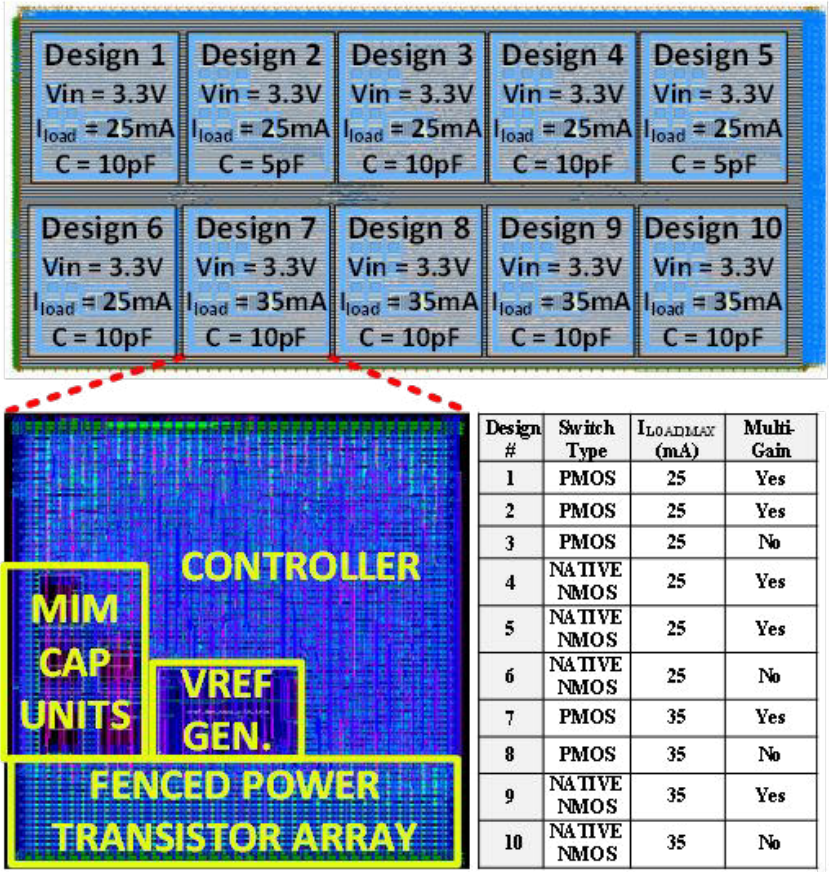
Open MPW Shuttle Program

efabless Sponsored by Google

# OpenFASOC on MPW-II: D-LDO generator

- Aux cells are swapped to experiment with different switch structures
- Multi-gain feedback loop is implemented

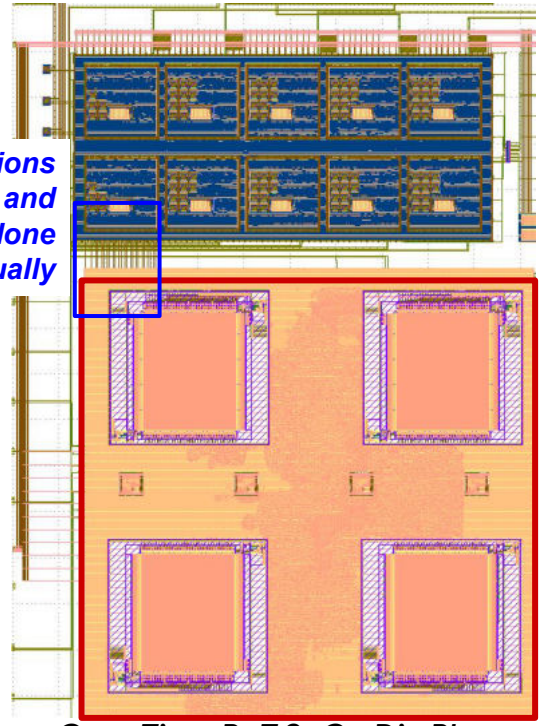



| Design # | Switch Type | $I_{LOADMAX}$ (mA) | Multi-Gain |
|---|---|---|---|
| 1 | PMOS | 25 | Yes |
| 2 | PMOS | 25 | Yes |
| 3 | PMOS | 25 | No |
| 4 | NATIVE NMOS | 25 | Yes |
| 5 | NATIVE NMOS | 25 | Yes |
| 6 | NATIVE NMOS | 25 | No |
| 7 | PMOS | 35 | Yes |
| 8 | PMOS | 35 | No |
| 9 | NATIVE NMOS | 35 | Yes |
| 10 | NATIVE NMOS | 35 | No |

# OpenFASOC on MPW-II:
## OpenTitan Root of Trust

- 1st SoC using AMS components
- The Opentitan SoC contains
  - UART, SPI interfaces
  - 16KB of SRAM (OpenRAM)
  - D-LDO is used to power-up all the blocks
  - All Peripherals are connected through Tilelink
- Timing has been carefully checked and an ECO flow has been used to avoid altering the $F_{MAX}$ while fixing hold violations




*OpenTitan RoT SoC - Die Photo*

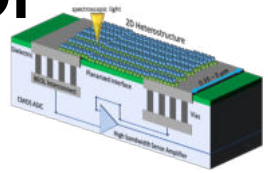
# On-Going Projects & Contributions

## Open-Source IC & tapeouts



➔ 1st *Open* Silicon Results

## NIST Nanofabrication Accelerator



➔ 1st *Open* Nanotechnology Platform

➔ Cryogenic Enablement & Design

## Low-Power IC Design



➔ *Rapid* Prototyping for Wearables

## Hardware Security



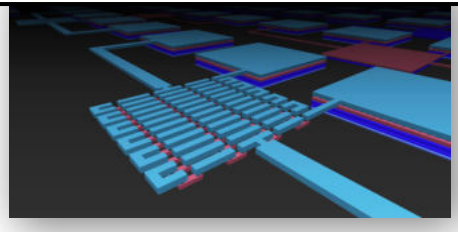
➔ 1st *Open* Root of Trust SoC

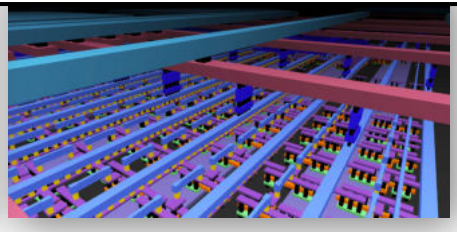
# *Automated* & *Open* Nanotechnology Platform

**NIST and Google to Create New Supply of Chips for Researchers and Tech Startups**

**Cooperative research agreement aims to unleash innovation in the semiconductor and nanotechnology industries.**

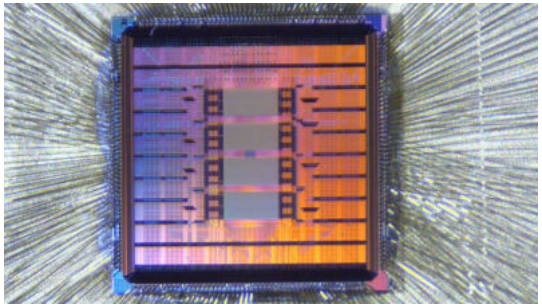
September 13, 2022





Google + NIST National Institute of Standards and Technology U.S. Department of Commerce

- Partnership with NIST:
  - Re-characterization of SKY130 with wide range temperatures including cryogenic (4K)
  - Automated test structures Generators
  - Nanofabrication Accelerator Platform



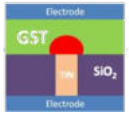
# *Automated* & *Open* Nanotechnology Platform

## CMOS Integration Critical for Measurements

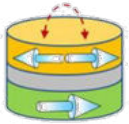
- New devices and materials are continually proposed by the academic community

Resistive switching memory (ReRAM)

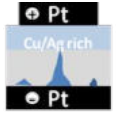

Phase Change Memory (PCM)



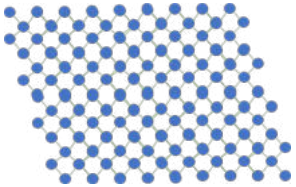

Spin Torque Transfer (STT - RAM)



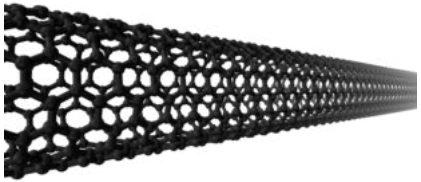
Conductive Bridge (CB-RAM)

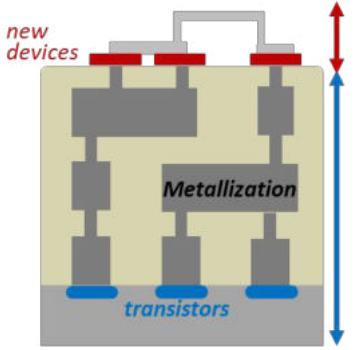



2D Materials



Nanotubes






**New devices**
ACADEMIC RESEARCHERS

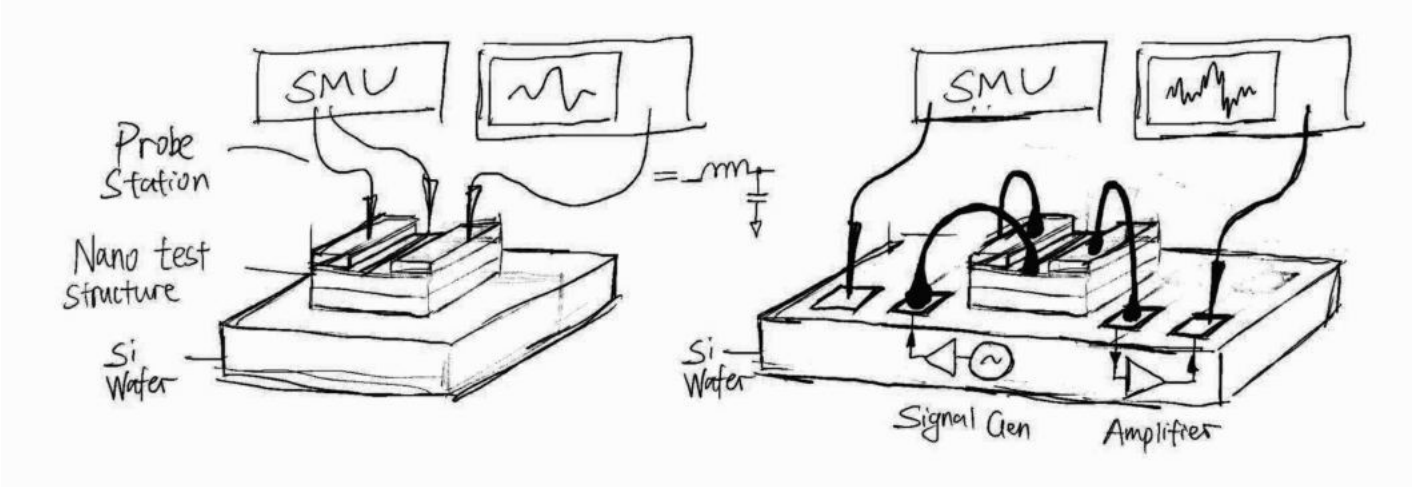
**CMOS circuitry**
FOUNDRIES

*Source: Brian Hoskins, NIST*

**Reliable monolithic integration is a requirement for experimental prototyping**

# *Automated* & *Open* Nanotechnology Platform

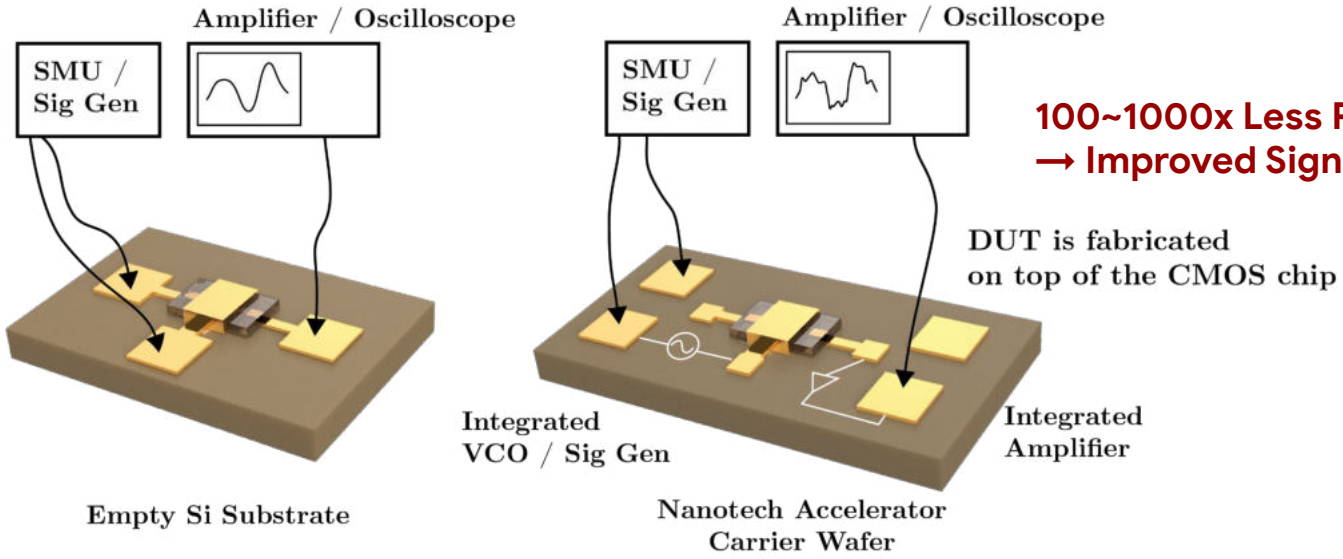
## The Concept




Monolithic Integration drastically reduces parasitics and leads to improved measurement quality and test ranges.

# *Automated* & *Open* Nanotechnology Platform

## Realization of Enhanced Parametric Test



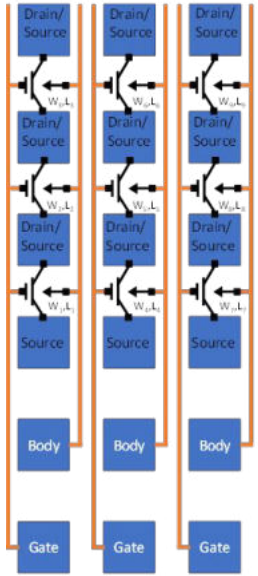

**100~1000x Less Parasitics**
**→ Improved Signal Fidelity**

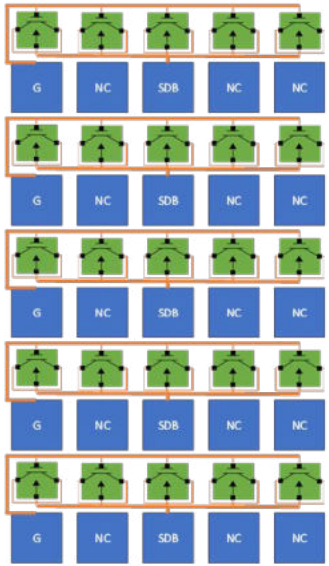
Traditional Method

This Project

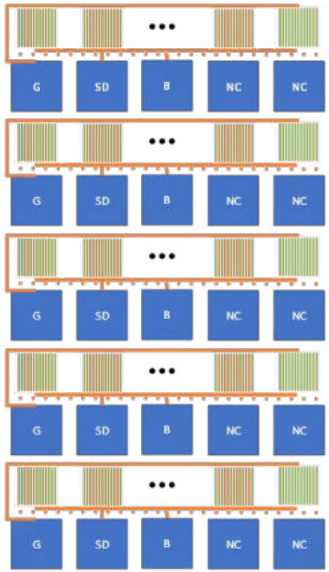
The aim of this project is to put part of the test apparatus on a silicon chip, which will be used as the carrier wafer for new nano device fabrication. Drastically reduced parasitics can lead to improved measurement quality and test ranges.

# Overview of Cryogenic Test Structures

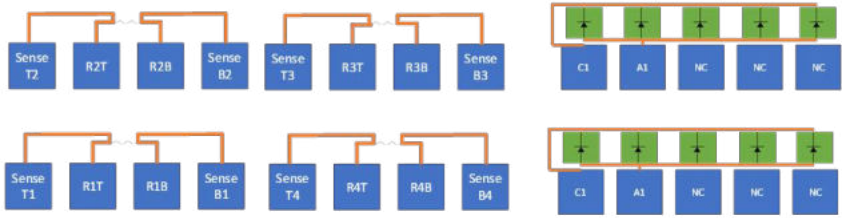


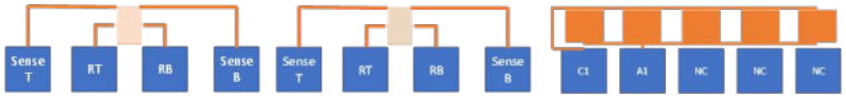

MOSCAP Arrays




Overlap MOSCAP Arrays




Precision Resistors



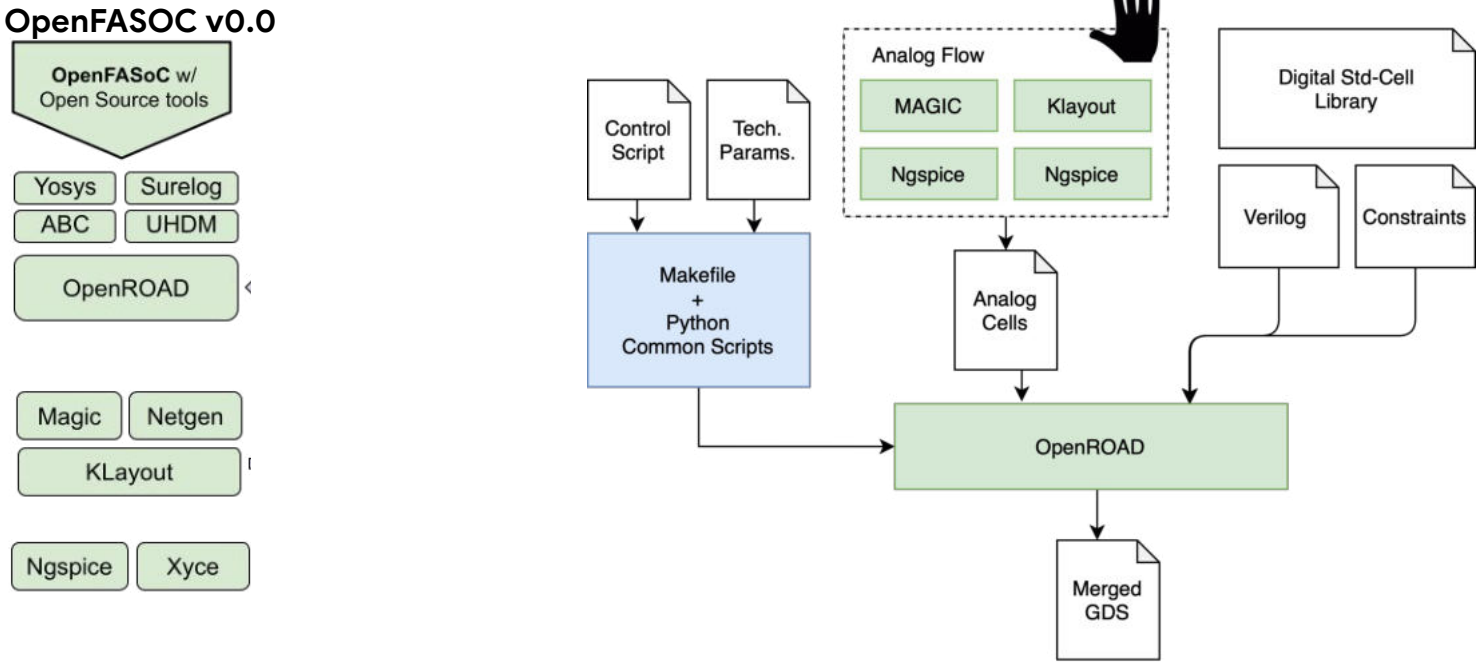

Line Resistance

Via Resistance

To Validation Modules

# OpenFASOC is Evolving

## New tools and Python-based APIs

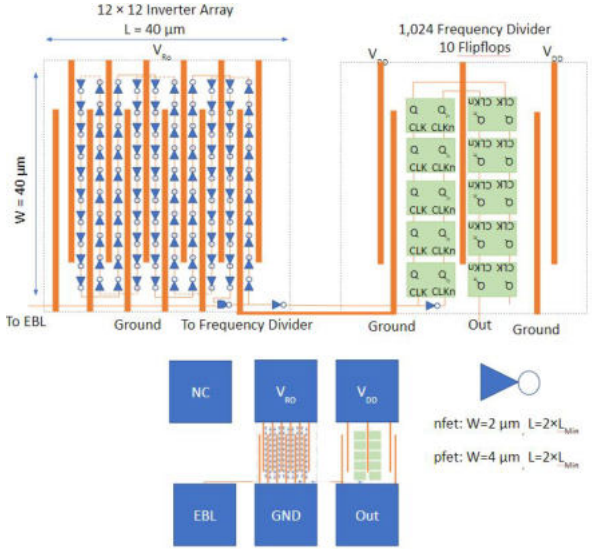



https://github.com/idea-fasoc/OpenFASOC

# OpenFASOC is Evolving

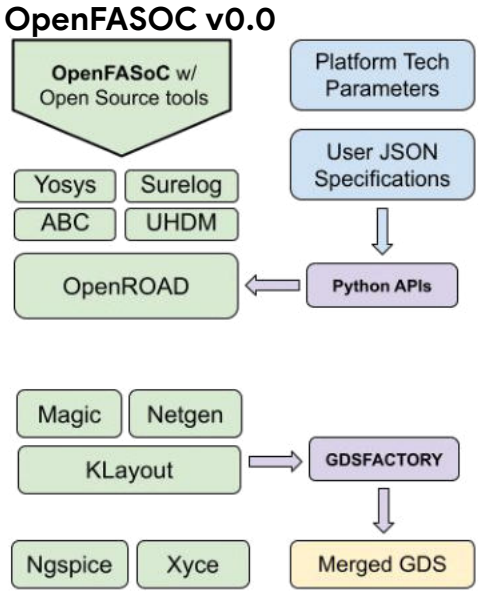
## New tools and Python-based APIs

**OpenFASOC v0.0**

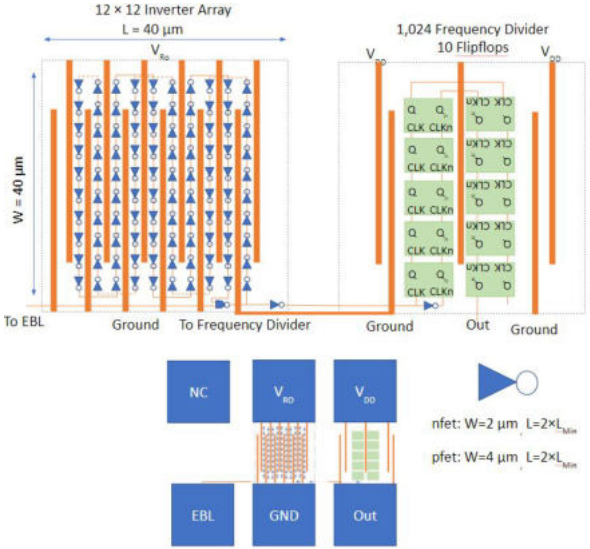



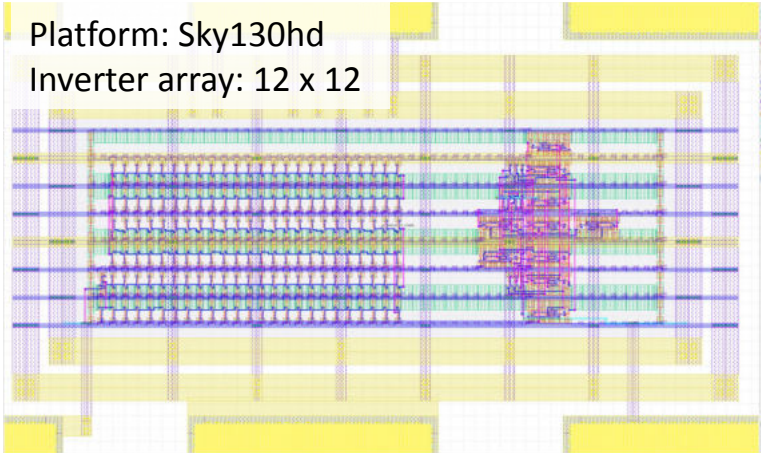

https://github.com/idea-fasoc/OpenFASOC

# Interleaved Placement in OpenROAD




Fully Automated Interleaved Ring-Oscillator VCO, with custom placement scripts



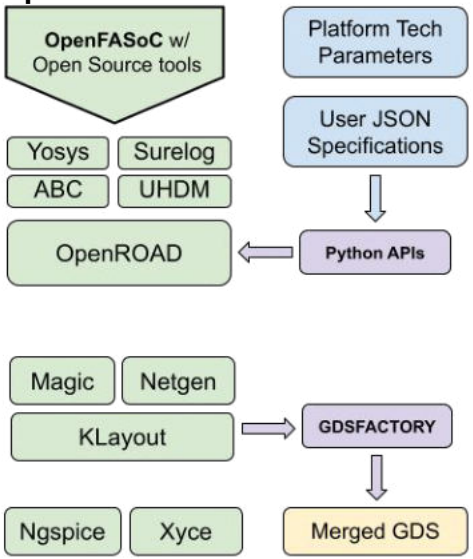




- Uses DEF manipulation using Python but could be integrated within OpenROAD

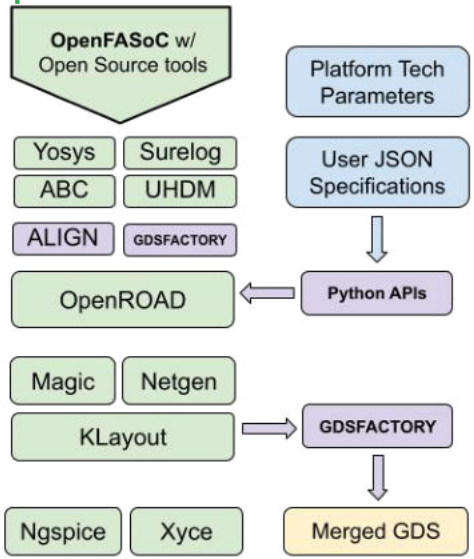
https://github.com/idea-fasoc/OpenFASOC

# OpenFASOC is Evolving
## New tools and Python-based APIs

**OpenFASOC v0.0**



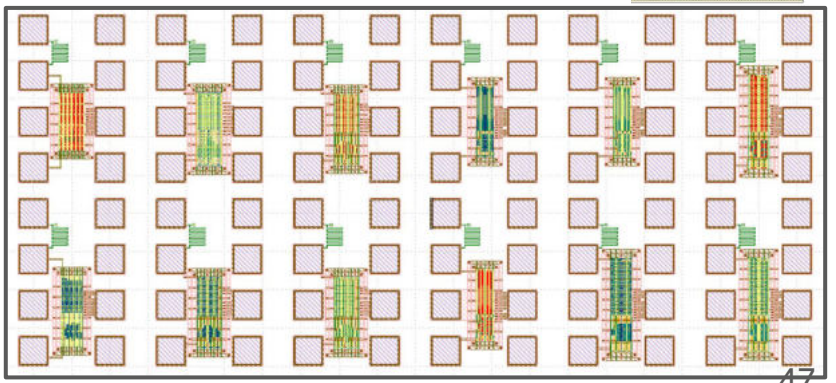

**OpenFASOC v1.0**




Fast Generation of all other RO structures

HD HS HVL
(By Skywater)

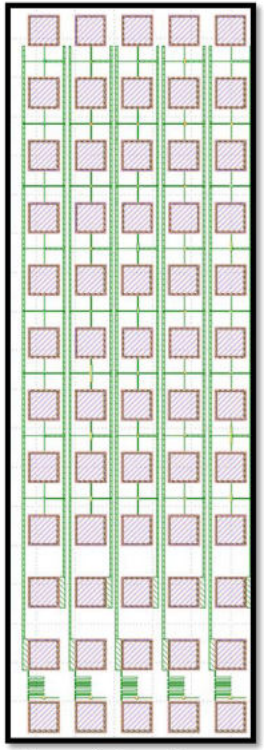
HS(12T) LS(12T) MS(12T),
HS(15T) LS(15T) MS(15T),
HS(18T) LS(18T) MS(18T)...
(Other Libs)



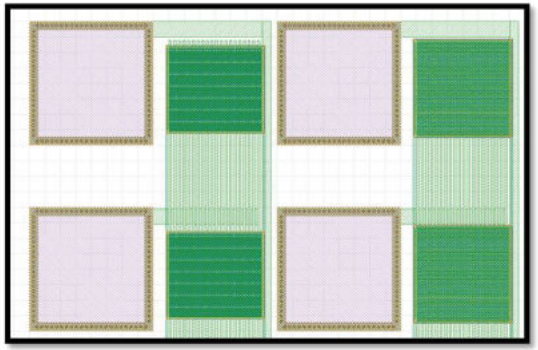
https://github.com/idea-fasoc/OpenFASOC

# Automated custom structures

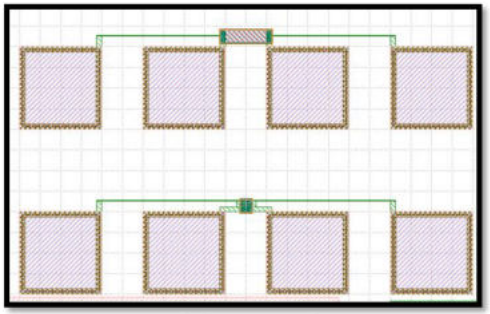
## GDSfactory



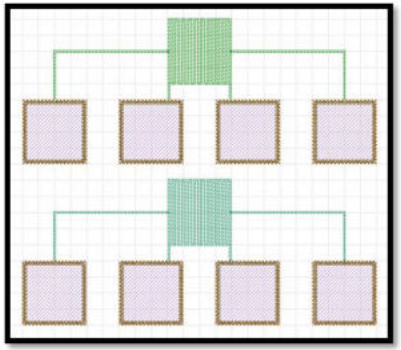
Transistor Arrays



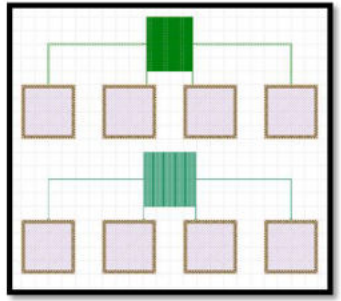
MOSCAP Arrays



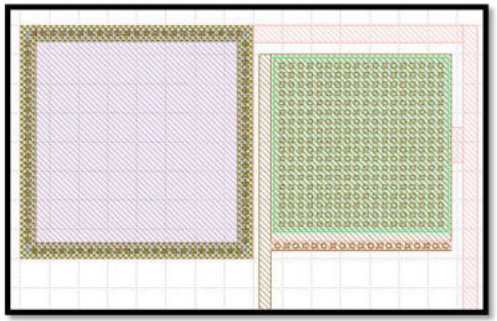
Precision Resistors



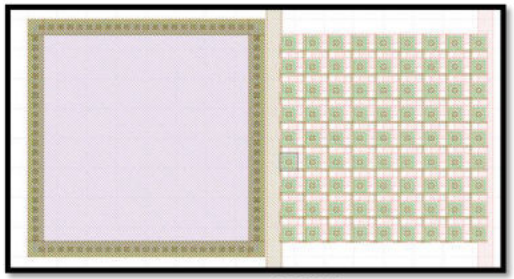
Line Resistance



Via Resistance



Diode Modules



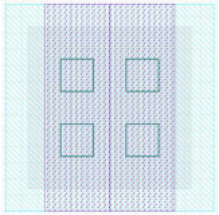
MIM
Capacitor Modules

# MIM Cap Generation using Gdsfactory

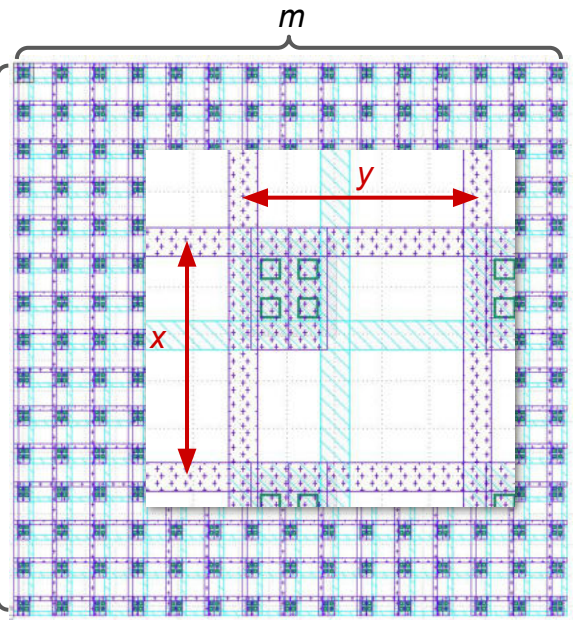
## GDSFACTORY Array creation routine

### GDSFACTORY Mesh creation routine

Inputs:
Mesh dimension *n,m*
Mesh pitch *x,y*
Mesh layers



*gf.path()*
*gf.add_ref()*
*gf.move()*



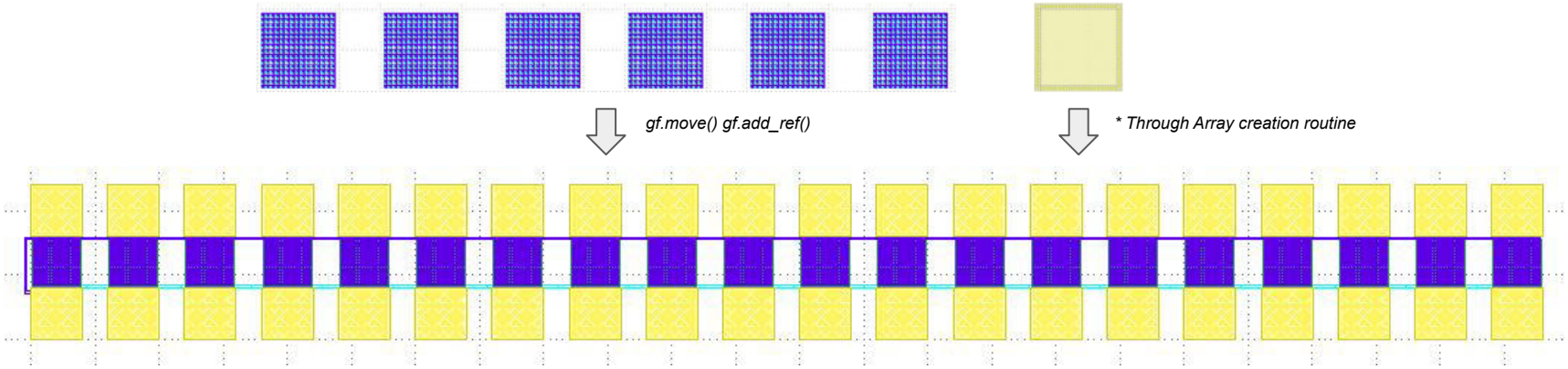

Inputs:
Multiplicity *a,b*
Offsets *x,y*

*gf.move()*
*gf.add_ref()*

# Example - Array of Flying MiM caps + Custom Padring

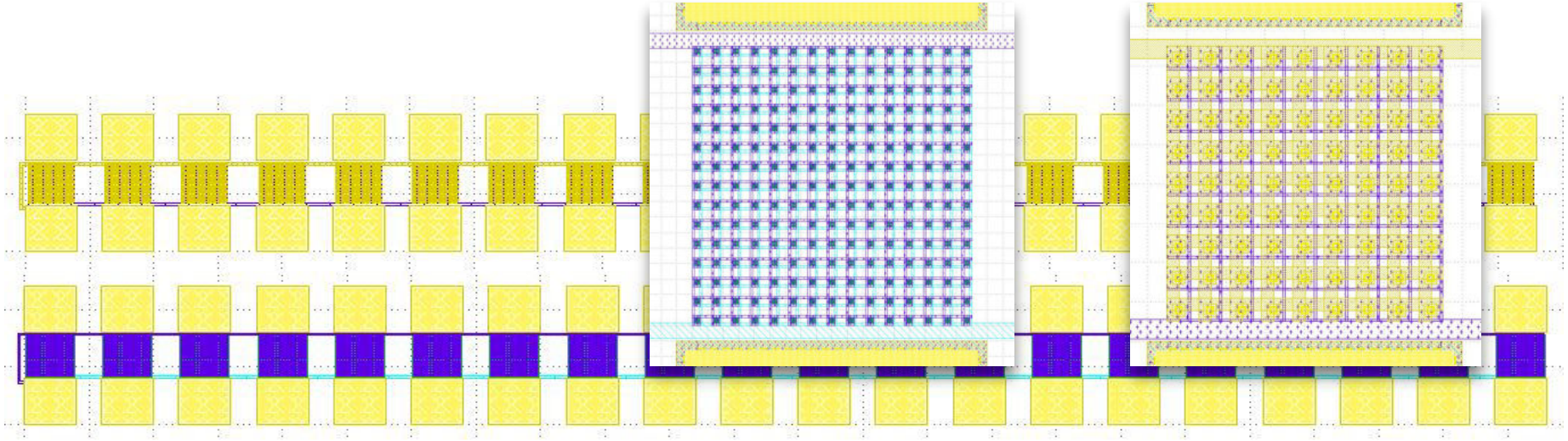
## GDSFACTORY Pad-ring place & route routine

Inputs:
Pad ring array spec
Connection definitions (semi-custom)



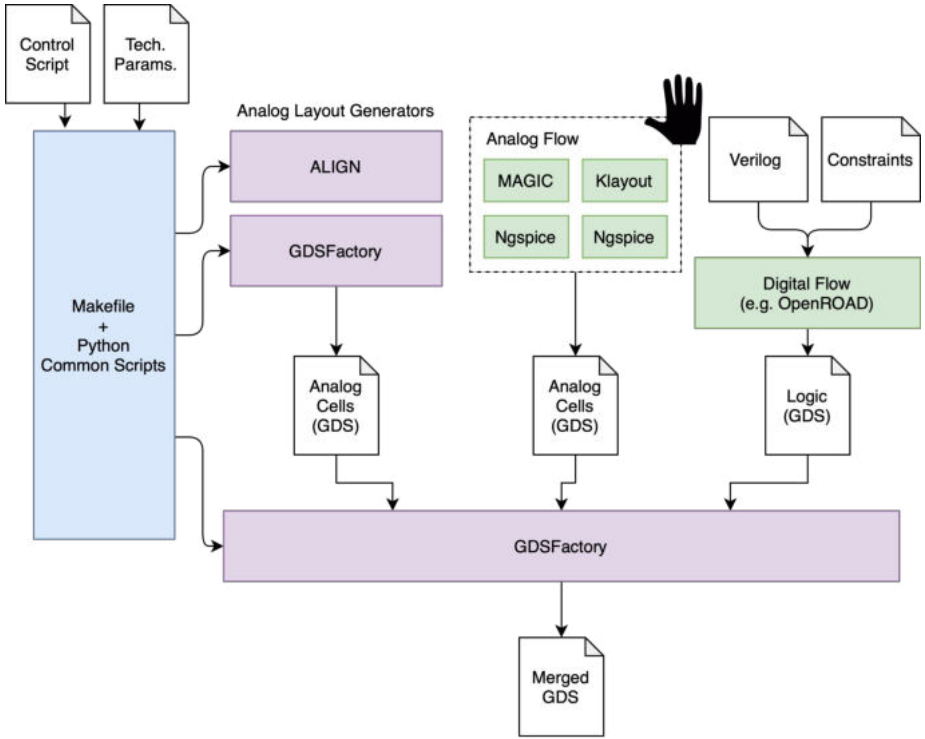
# MIM Cap Generation using Gdsfactory

- Computes the grid and places capacitor on grid
- Generates connecting metals (with minimum metal spacing)
- Replicates and connects the structures to pads

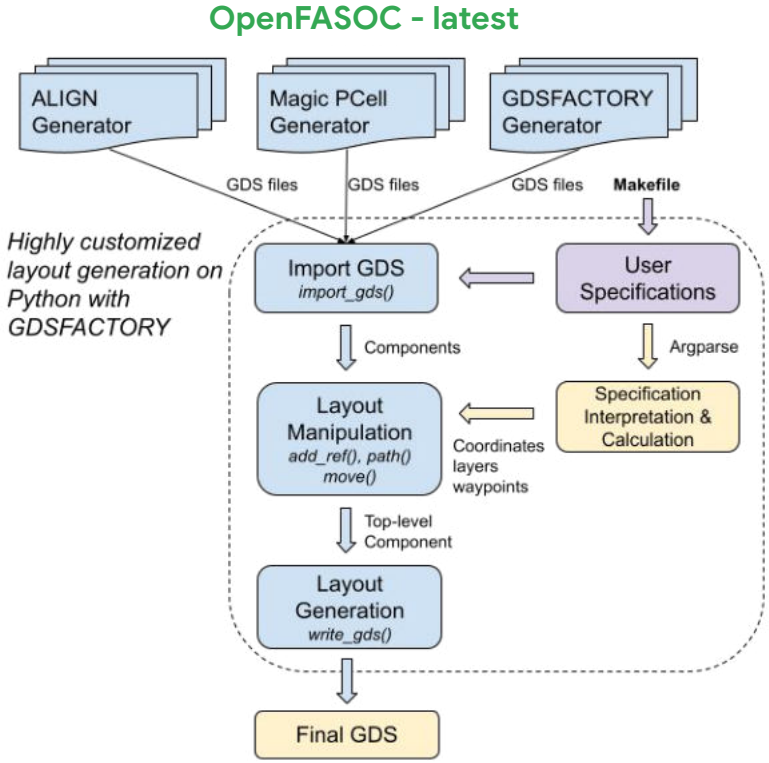


# OpenFASOC is Evolving

## New tools and Python-based APIs



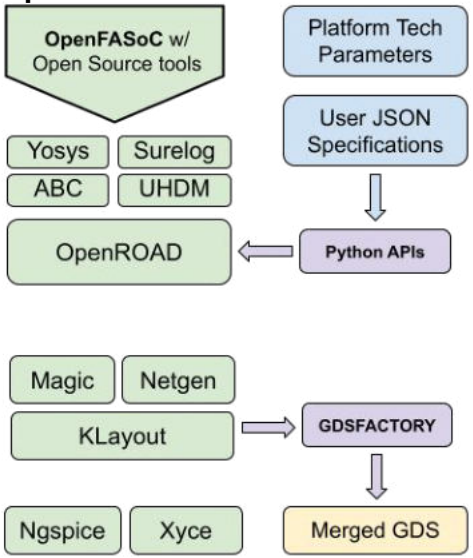

https://github.com/idea-fasoc/OpenFASOC



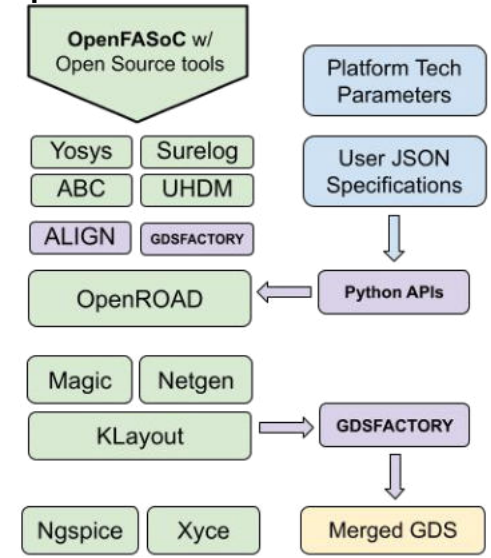
# OpenFASOC is Evolving

## New tools and Python-based APIs

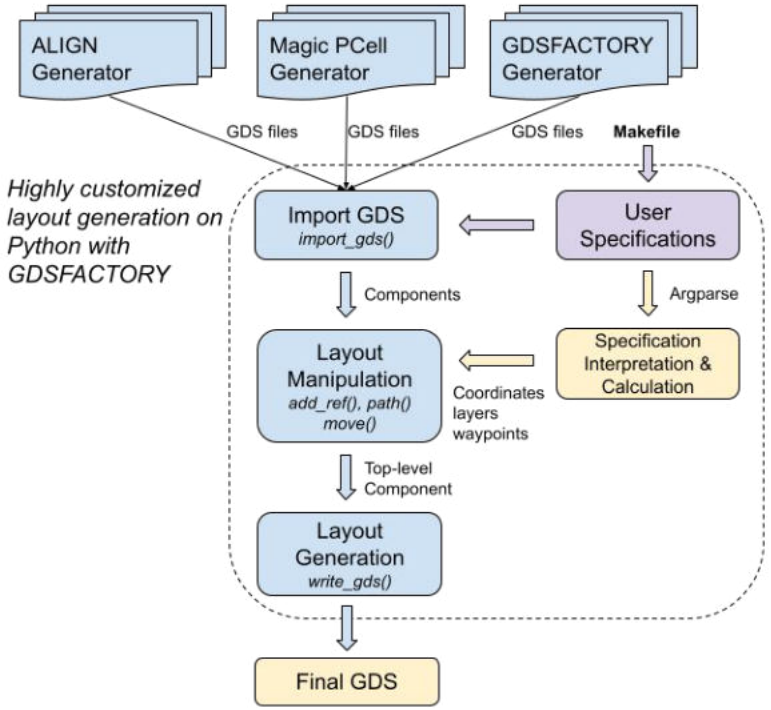
**OpenFASOC v0.0**




**OpenFASOC v1.0**




**OpenFASOC - latest**

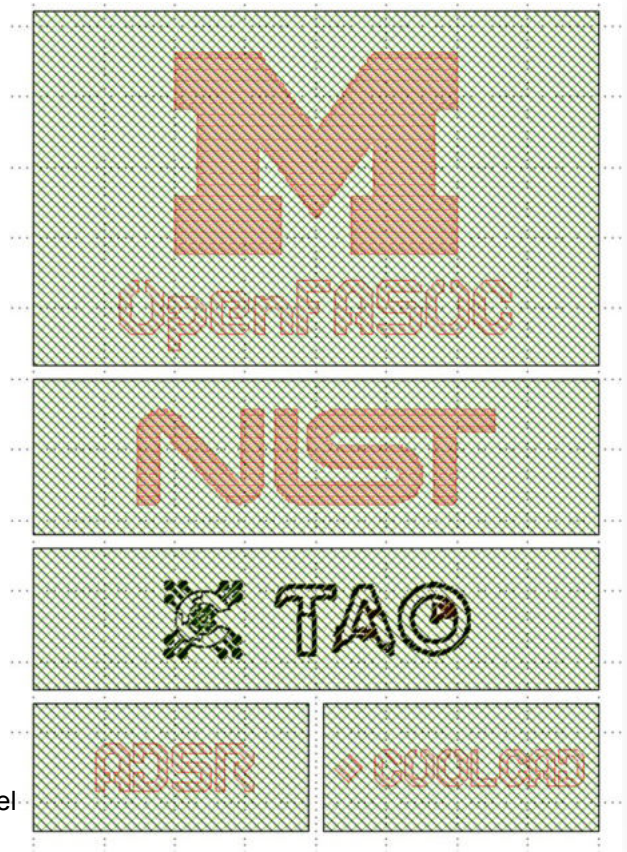


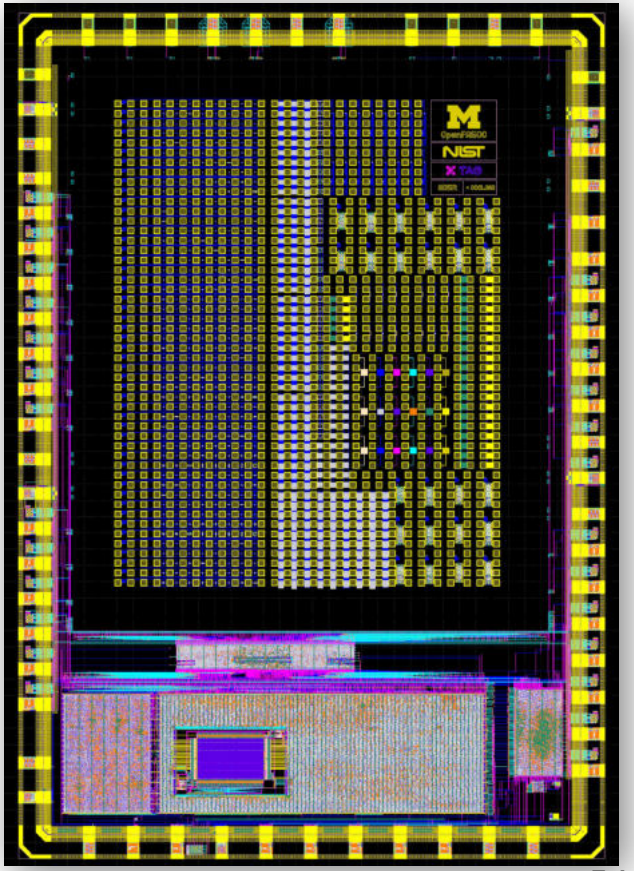

https://github.com/idea-fasoc/OpenFASOC

# Resultant Test Die MPW-5

**Major Highlights!**

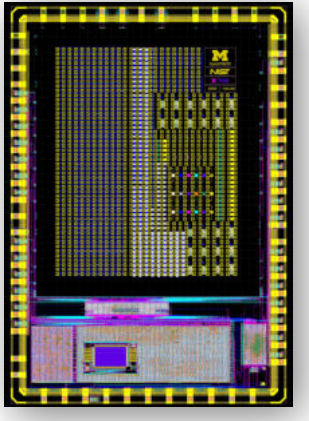
- Over 1400 Pads
- 400+ Transistor Structures
- 30 Capacitor Test Structures
- 24 Ring Oscillators
- 18 line and via chain modules
- 7 Diode Test Structures



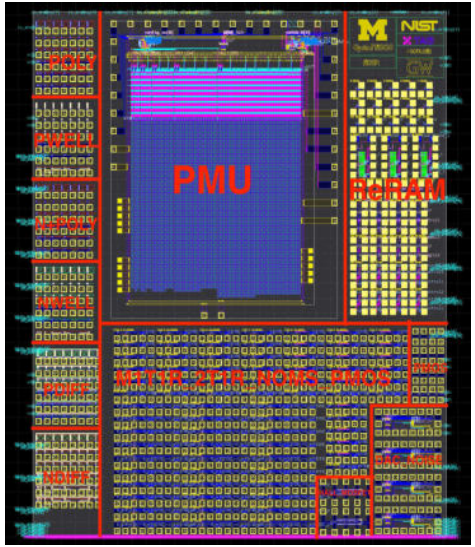



https://github.com/msaligane/openfasoc_cryo_caravel

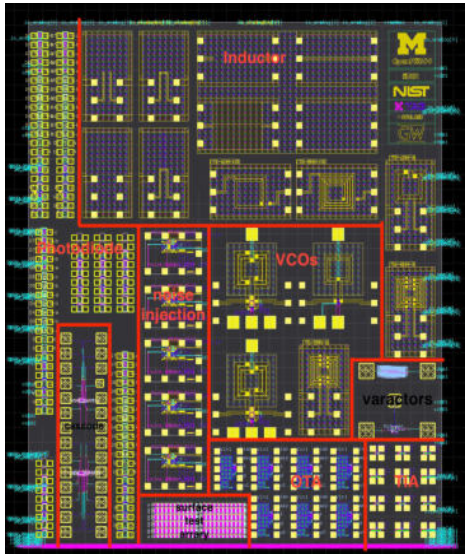
# 4 Tapeouts Already! Final Tapeout Loading...



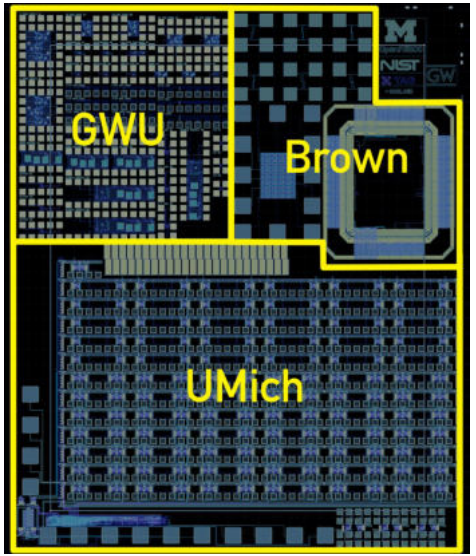
MPW-5




MPW-6



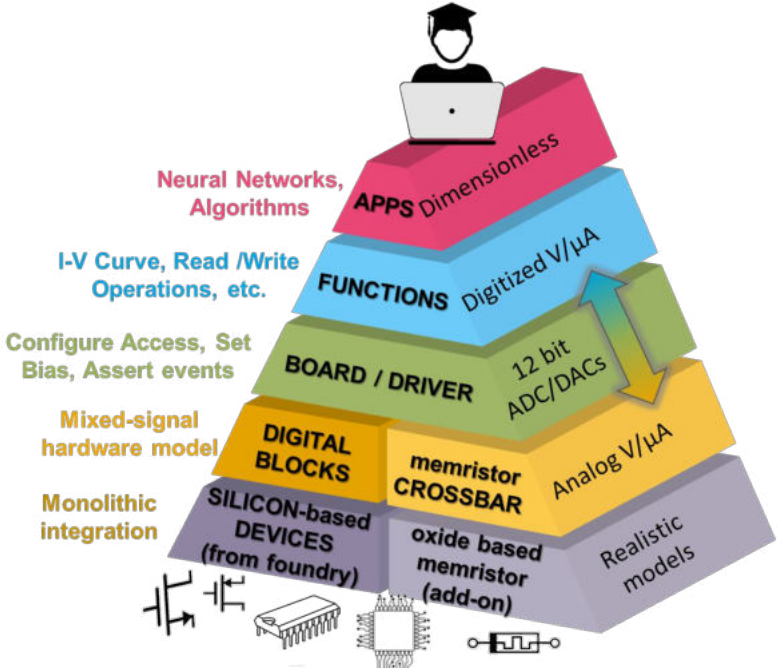

MPW-7

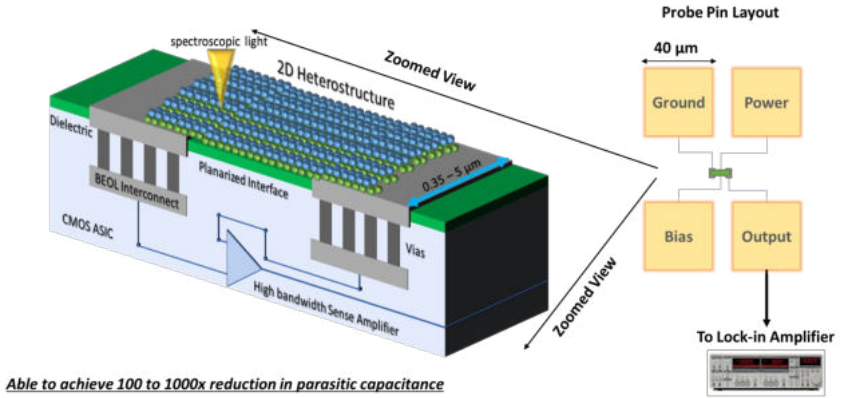



MPW-8

# Lowering Barrier to Chip Design

- Enabling Open Collaboration and other Research communities



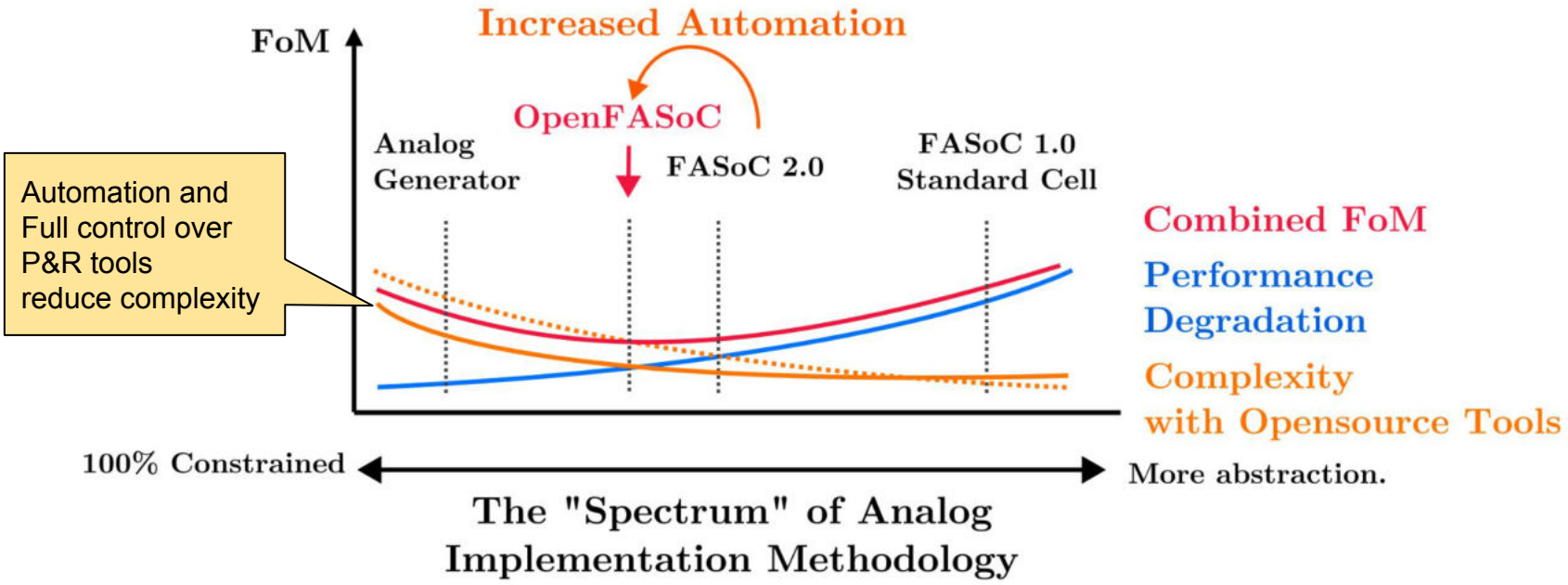




*Able to achieve 100 to 1000x reduction in parasitic capacitance*

*Source: Brian Hoskins, NIST*

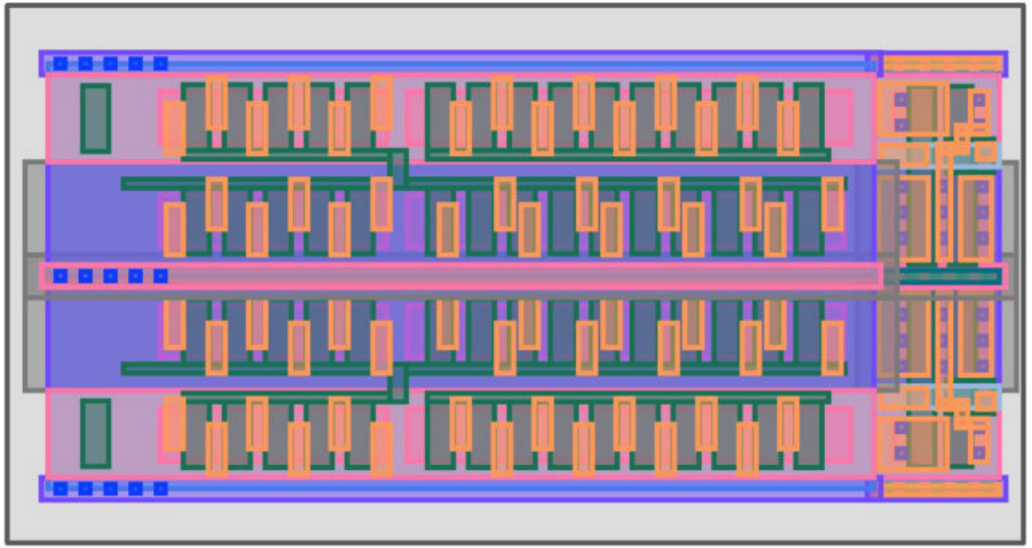
# Performance / Complexity Tradeoff

- FASoC augments digital flow with APR tool placement/routing constraints and minimizes the (performance loss * complexity)



# Generator with a Higher Control/Precision

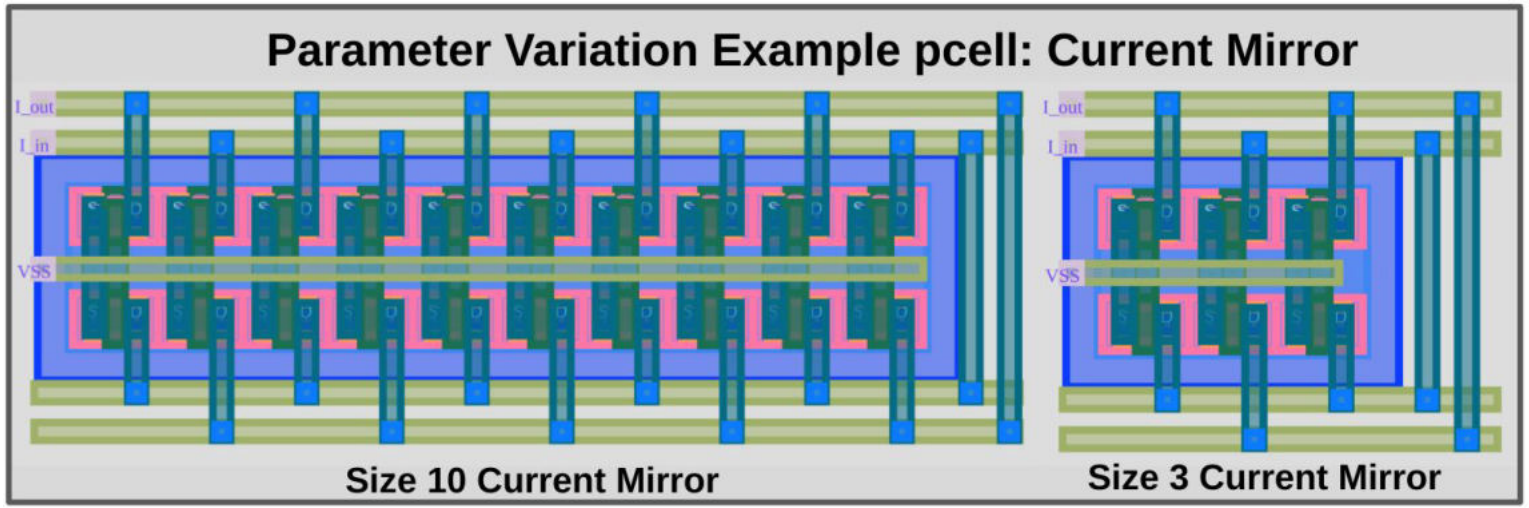
- Addresses porting Aux-cells to new PDK
- Programmatic layout provide fine control with automation



Auto-Generated Comparator Cell

# Generator with a Higher Control/Precision

- Object oriented code provides flexibility
- PDK -> py class
- Generators -> py function
- User codes hardware by importing py packages




Parameter Variation

# Integration with GDSfactory & OpenROAD

**OpenFASOC with GDSFactory Generator API**

**Python PDK**

**Technology Layers**
PDK.get_layer()

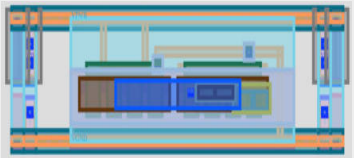
**DRC Rule Deck**

**Component Lib**
PDK.get_component()

**Generator**

```
# function interface
@gf.cell
def top(args, PDK):
        …
        return top
```

e.g Voltage Header Cell



**Imports**

**User Created PY Script**

```
import [PDK]
import openfasoc.[Generator]

cell = [Generator].top(args,PDK)
cell.write_gds()
```

**Integrating Cells**

1. **Defined cell placement**
2. **Auto route**

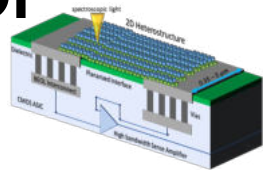
# On-Going Projects & Contributions

## Open-Source IC & tapeouts



➔ 1st *Open* Silicon Results

## NIST Nanofabrication Accelerator



➔ 1st *Open* Nanotechnology Platform

➔ Cryogenic Enablement & Design

## Low-Power IC Design



➔ *Rapid* Prototyping for Wearables

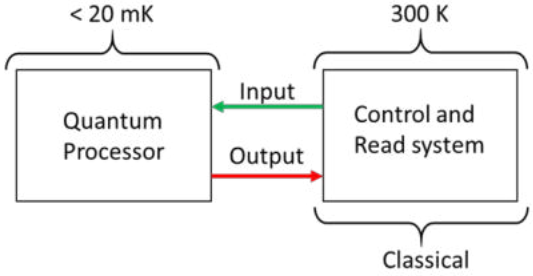
## Hardware Security

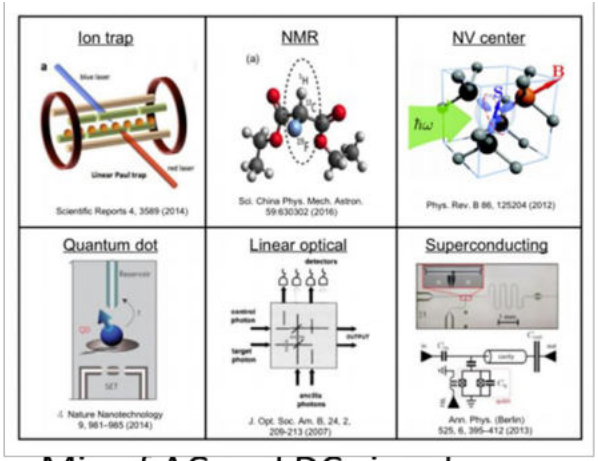


➔ 1st *Open* Root of Trust SoC

# Control Electronics for Quantum Computers

Quantum computer: < 20 mK



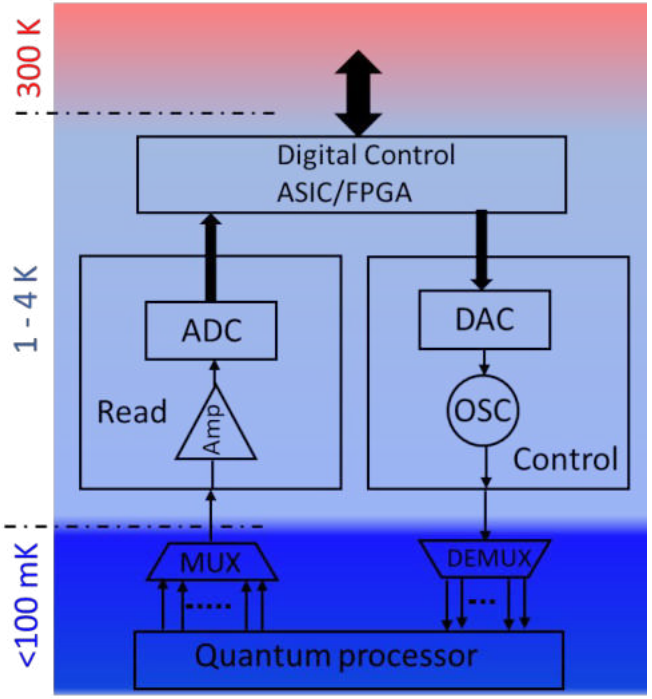

Mix of AC and DC signal required to control and read the Qubits

Digital

- Inverters, ring oscillators

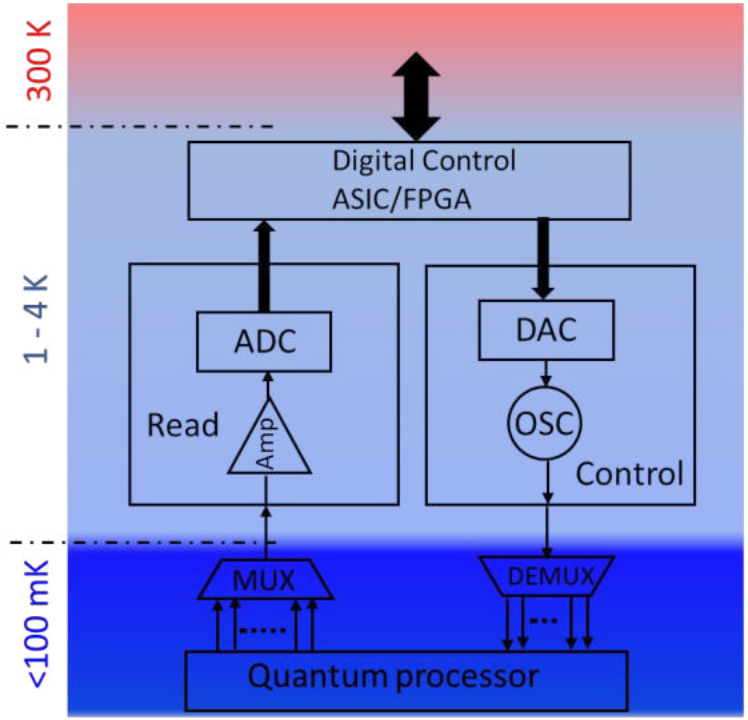
Analog

- Voltage reference, Low Noise Amplifiers

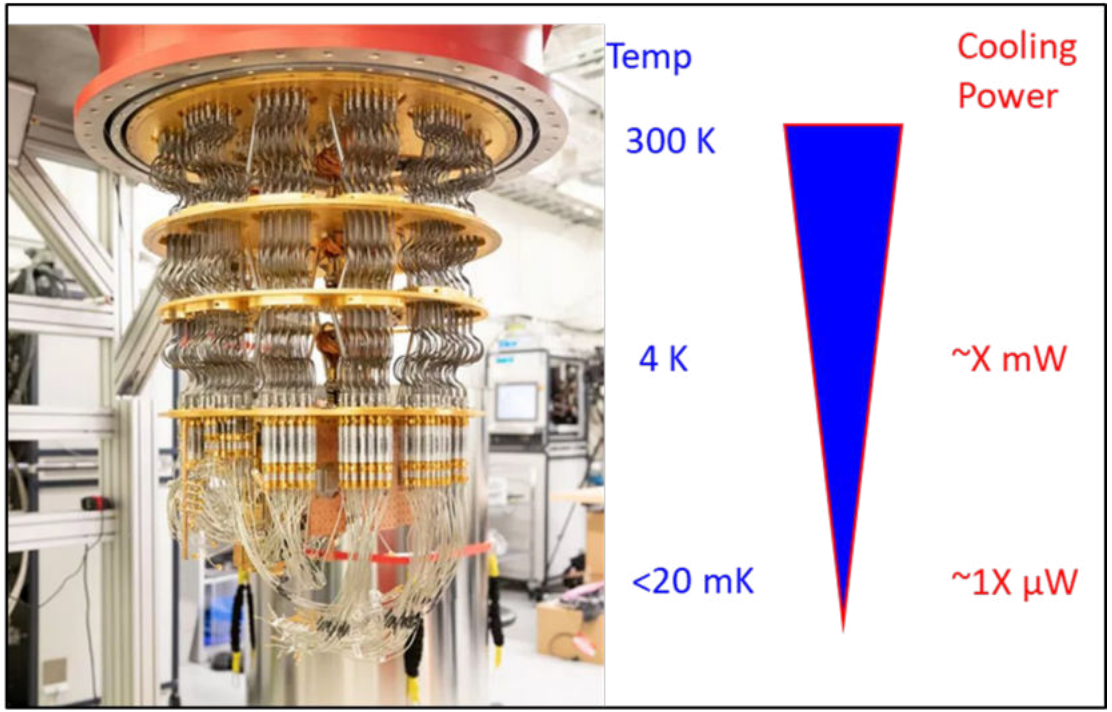



https://phys.org/news/2020-08-google-largest-chemical-simulation-quantum.html ; https://www.cnet.com/news/google-quantum-supremacy-only-first-taste-of-computing-revolution, Amundson, J.; Sexton-Kennedy, E. J. E. W. C., Quantum Computing. 2019

# Requirement of Low Operating Power

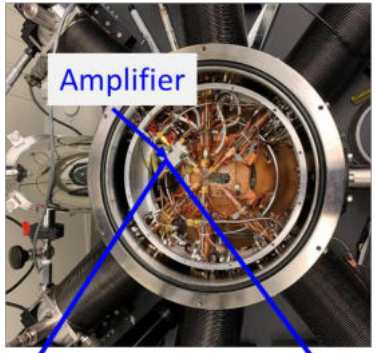


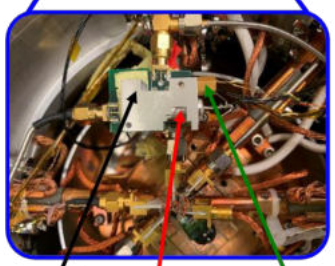

Low power operation



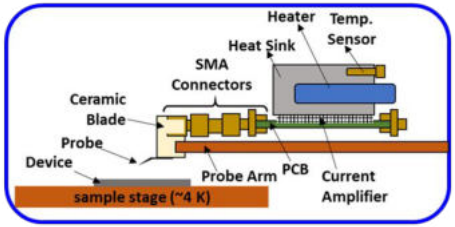

*Source: Brian Hoskins, NIST*

# *Open* Cryogenic CMOS



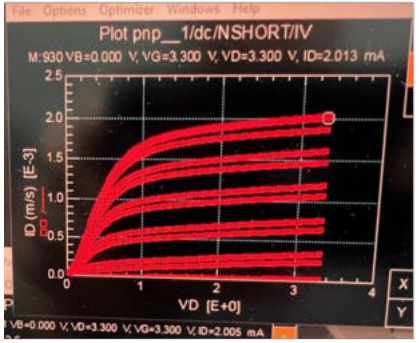




Time + Temperature dependent characterization

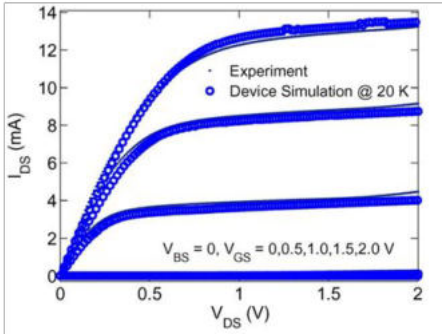



## Cryogenic Models and Data of Open Sky130

### Raw Data




### Fit Models



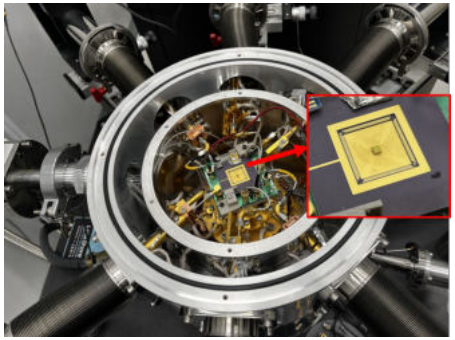

Google + NIST National Institute of Standards and Technology U.S. Department of Commerce

AIDSIR COOLCAD ELECTRONICS

skywater

# *Automated* PMU for Low-K Operation

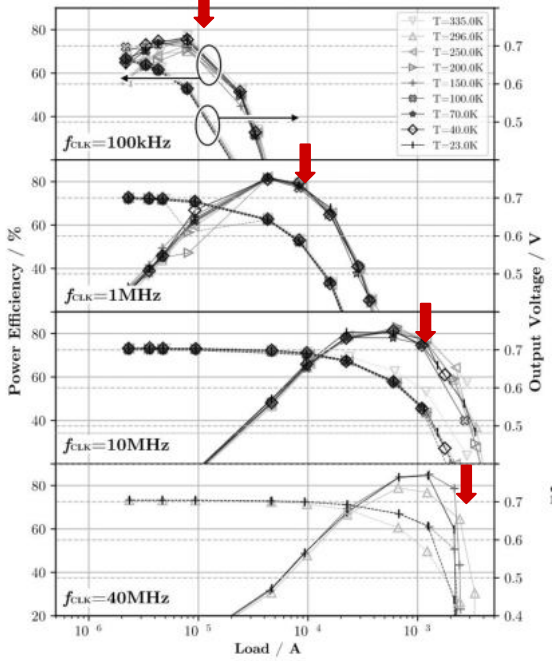
## Measurement Results



Cryogenic Test Setup

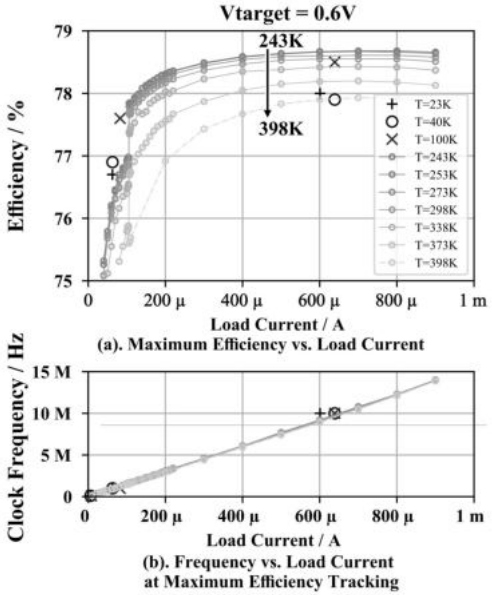
Experiments have shown constant behavior across a wide temperature range, down to cryogenic temperatures.

Maximum Eff. Point




Power Efficiency & Output Voltage
Versus Load Current, Clock Freq., and Temperature

Robust against Temperature Variation




Emulated Closed-Loop Response
At Maximum-Power Tracking