Autonomous platforms driven by MIPS multi-threaded, safety-capable, efficient RISC-V compute solutions

Cheol Kim, Product Marketing

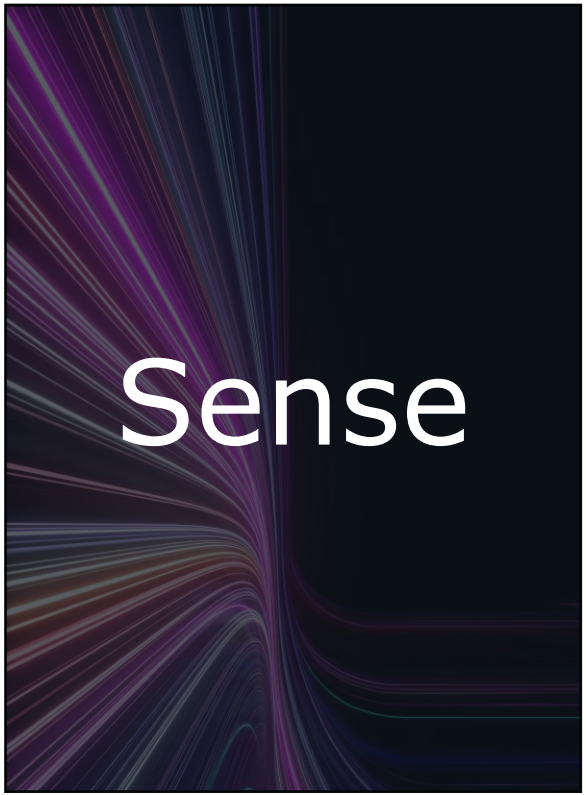
MIPS Technologies, Inc.

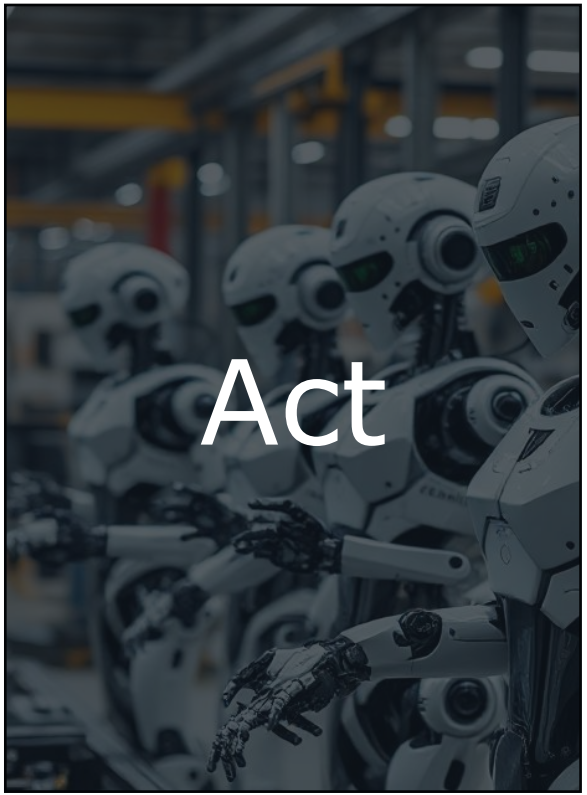
RISC-V Spring Day, Tokyo, Japan

40 Years of RISC Innovation

Mid-80's | Early 90's | Mid-90's | Mid 10's | Early 20's | Mid-20's

The Next Generation of Autonomous Platforms





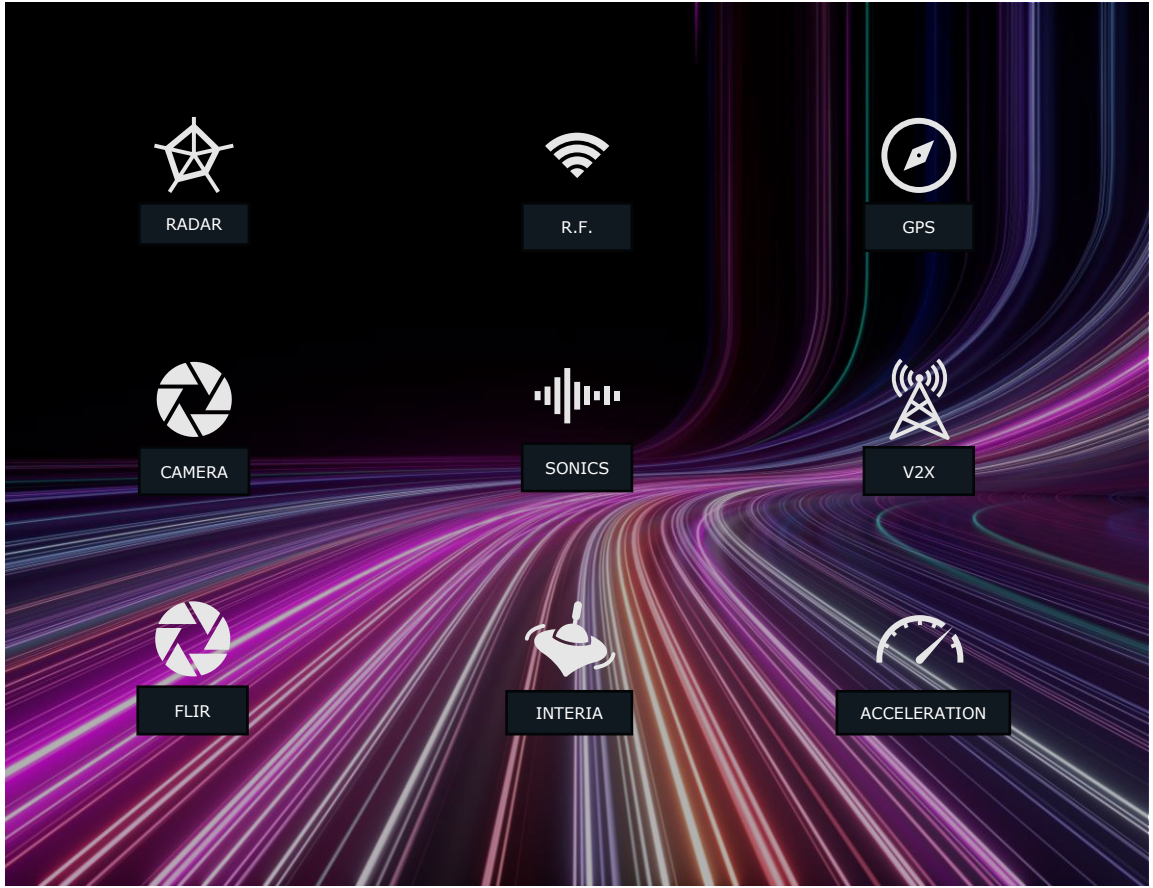
Sense

Autonomous platforms need senses to perceive the world around them.

Compute platforms for sensor fusion and data movement enable:

- ADAS & Autonomous Vehicles
- Smart Spaces
- Industrial Robots
- Factory Automation
- Healthcare Platforms
- Agricultural Production

These compute platforms combine different sensor data and prioritize critical information efficiently.

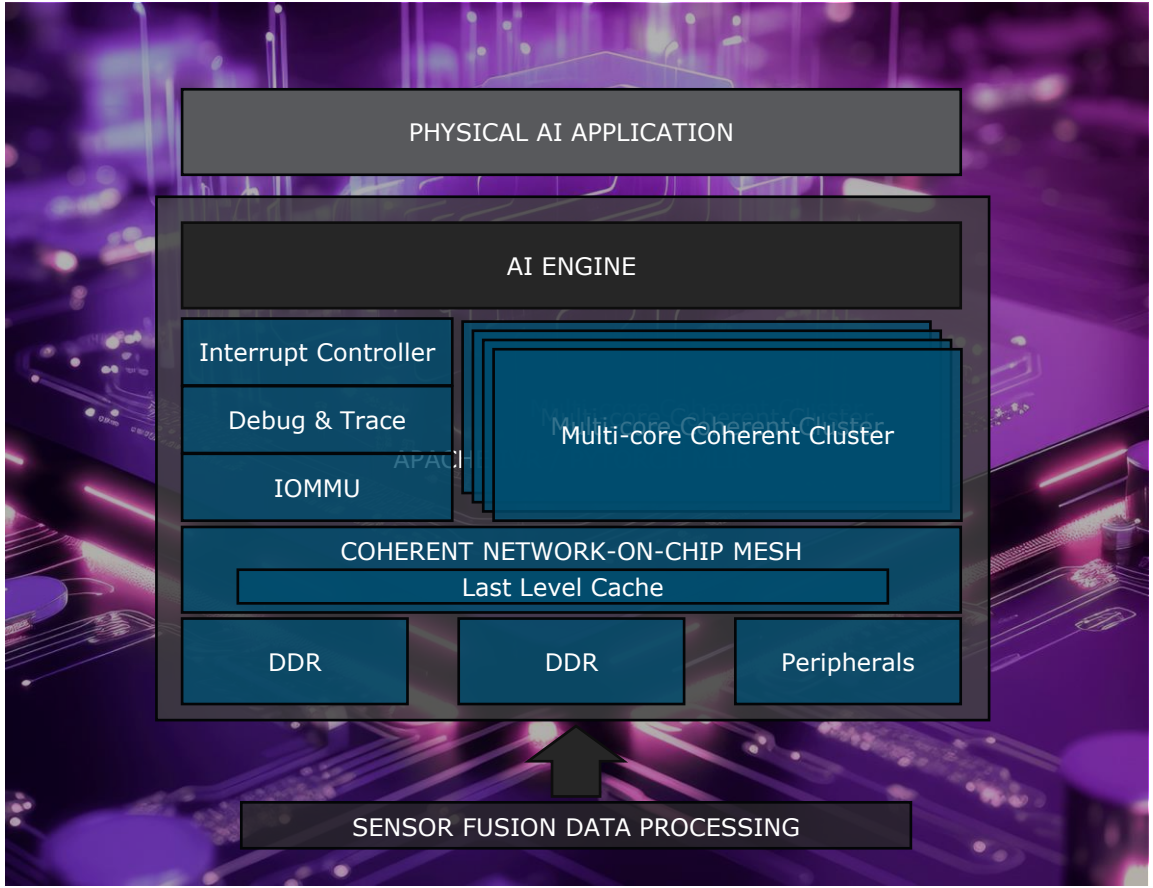


Think

Autonomous platforms make decisions based on the information provided by the compute platforms that sense. These decisions are made using Physical AI models and executed by AI decision engines.

Physical AI enables autonomous vehicles, smart spaces, or industrial machines to perceive the world, adapt to new challenges, and solve problems.

Today, MIPS data movement subsystems with multi-threaded multi-core coherent clusters can be tightly integrated into data processing and data movement flows with AI engines.



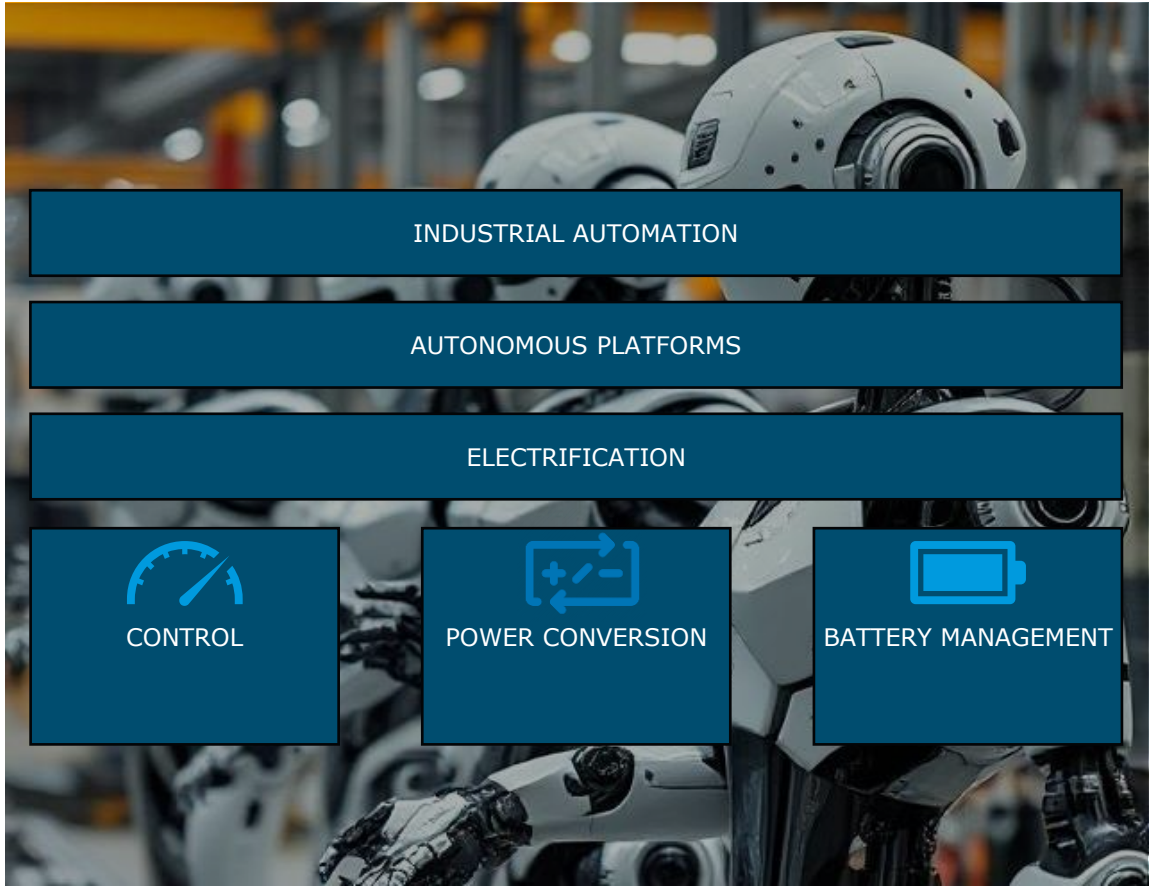
Act

The next frontier for technology is to solve safe deterministic, low-latency compute platforms.

An autonomous system can sense, perceive, plan and act without intervention.

The system will act only when it is safe to do so, avoiding situations that pose a risk to human safety, property, or the autonomous system itself.

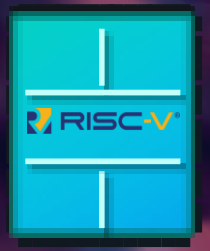
Safety certifications are crucial for the autonomous platforms of the future.



Application Processor Data Movement Subsystems

MIPS P8700 DMS

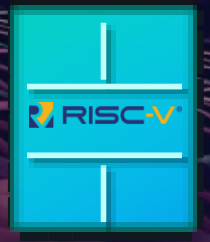
Industry First High-Performance Multi-threaded RISC-V CPU for Automotive



- The only multi-threaded RISC-V out-of-order core with ASIL-B certification
- Highly-scalable multi-core, multi-cluster coherent computing solution
- MIPS extensions for improved performance and functionality
- Targeting:
  - Embedded Data Center
  - Automotive Gateway
  - Automotive ADAS
  - Industrial & Embedded

MIPS I8500 DMS

Data Movement Engines for the Increasingly Connected World



- The only multi-threaded RISC-V core capable of executing four threads
- Highly-scalable multi-core, multi-cluster coherent computing solution
- MIPS extensions for improved performance and functionality
- Targeting:
  - Embedded Data Center
  - 5G/6G Networking
  - Automotive Gateway
  - Industrial & Embedded

Production Qualified – P8700 First 5nm RISC-V Automotive Processor Tape-out!

MIPS I8500 Data Movement Subsystem (DMS)

Cluster of multithreading processors inter-connected to enable cache coherence between all CPUs & I/O devices

CPU Cores

- 64-bit RISC-V ISA RV64A/B23 profile
- 3-Wide issue, In-Order, 9 stage pipeline
- Hardware multi-threading supports 1, 2 or 4 hardware threads per core

I/O Coherence Units

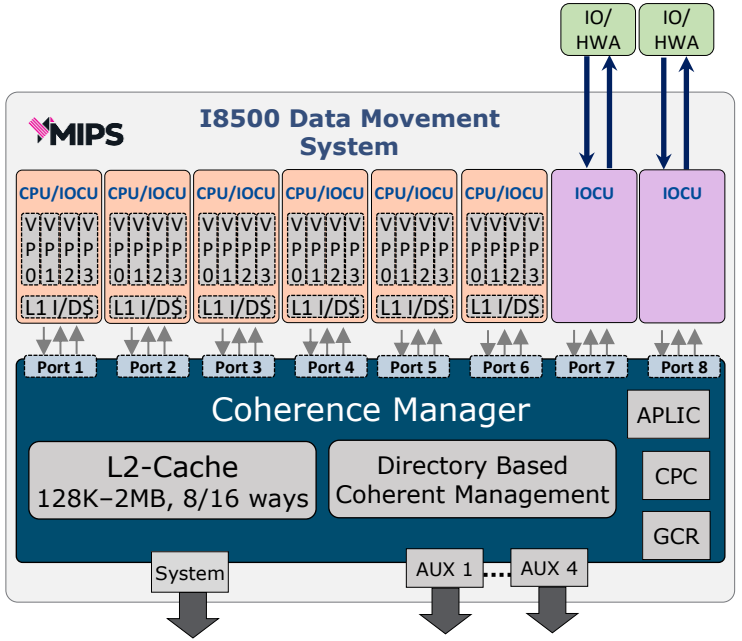
- Hardware I/O coherence is provided by the I/O Coherence Unit (IOCU)
- IOCU devices maintains coherence of the caches in all CPUs in the cluster

Coherence Manager

- Integrated L2$ contains both Data and Instruction
- Hardware L2$ prefetch controller significantly improves performance
- Directory-based coherent manager maintains coherence with the cores' L1-D$
- High performance data movement with 512-bit internal data-paths throughout.
- Up to 8 requestor Ports for up to 6x CPUs and up to 8x IOCUs

System-level Features

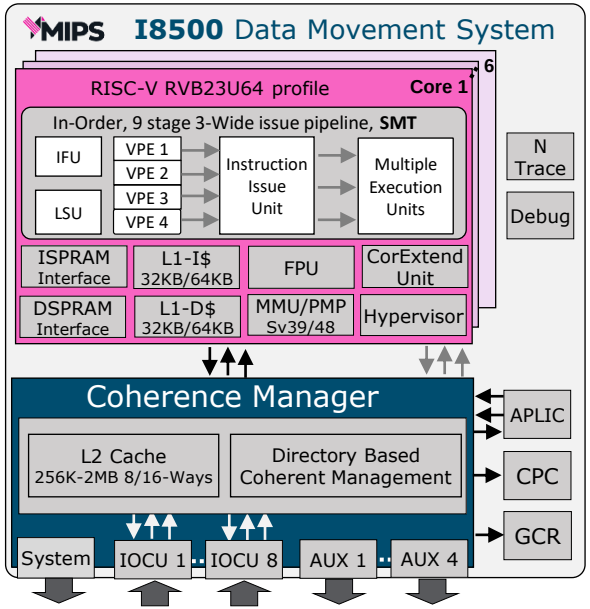
- Virtualization module support
- Cluster Power Controller (CPC) to shut down idle cores for power efficiency
- Advanced Platform Level Interrupt Controller (APLIC)Advanced Interrupt Architecture interrupt (AIA) controller



MIPS I8500 Core-Level Features

Fully synthesizable, low-power, performance- & area-efficient design

- 64-bit RISC-V ISA via RV64A/B23 profile
- 3-Wide issue, In-Order, 9 stage pipeline
- Hardware multi-threading supports one, two, or four threads per core (1T/2T/4T)
- 48-bit virtual & physical addresses
- Virtualization support
- Programmable Memory Management Unit (MMU)
- L1 caches with Error Correction Code (ECC) protection
- L2 cache support, implemented as shared L2 in the CM
- Double-pair Load or Store per cycle
- Unaligned load / store support in hardware
- Optional Instruction/Data Scratch Pad RAM (I/D-SPRAM)



MIPS Simultaneous Multi-threading (SMT)

Efficient Simultaneous Multithreading (SMT) supports 4 hardware threads (Harts) that can be classified as 1, 2, or 4 threads per core.

- Single-Thread (1T) 2-wide issue: 2 instructions can be issued from the same Harts.
- Multi-Thread (2T or 4T) 3-wide issue: 3 instructions can be issued from the same or different Harts

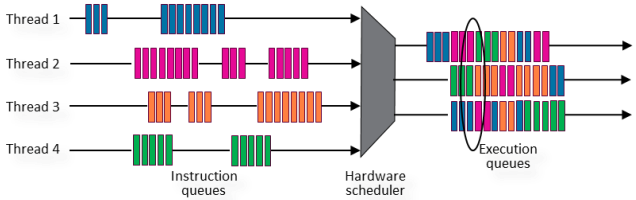
Zero overhead when switching between Harts

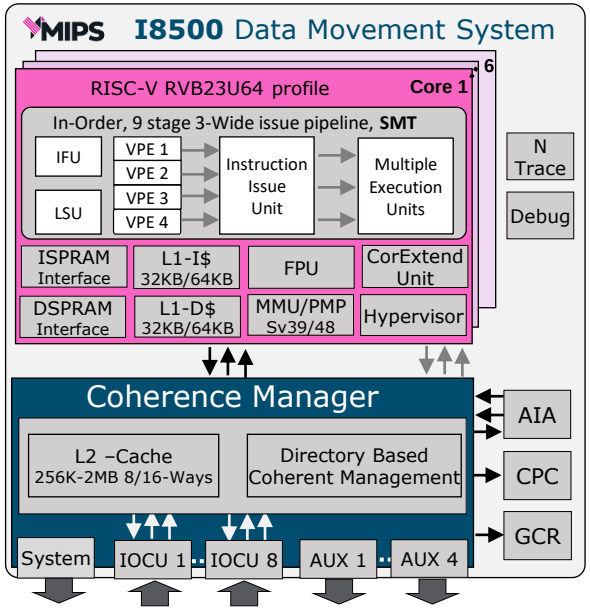
- Maximize utilization pf processors core
- Does not impact IPC

Wait For Event support:

- Software “WAIT” instruction pauses execution until event received at thread level for immediate execution resume

Take full advantage of CPU hardware for multiple threads of execution handling data movement and control





MIPS P8700 Data Movement Subsystem (DMS)

A cluster of multithreading processors interconnected to enable cache-coherence between all CPUs & I/O devices

CPU Cores

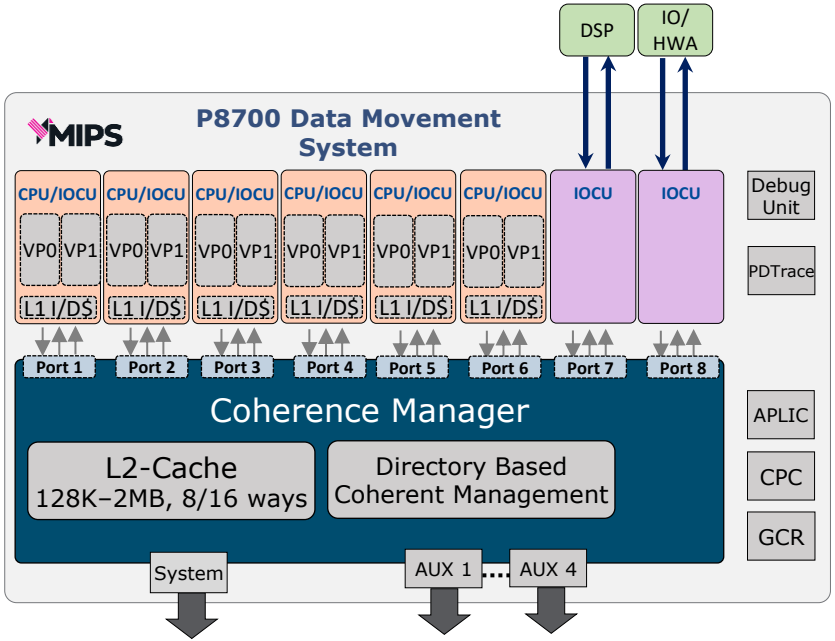
- 64-bit RISC-V ISA RV64IGC_Zba_Zbb profile (G = IMAFD)
- 4-Wide issue, Out-of-Order execution, 16 stage pipeline
- Hardware multi-threading supports 1 or 2 hardware threads per core

I/O Coherence Units

- Hardware I/O coherence is provided by the I/O Coherence Unit (IOCU).
- IOCU devices maintains coherence of the caches in all CPUs in the cluster.

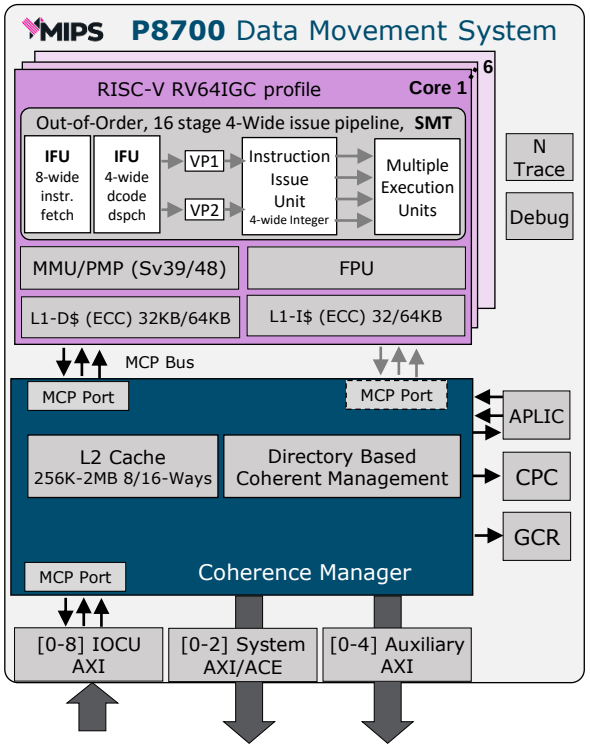
Safety

- Only RISC-V Out-of-order multi-threaded ASIL-B Certified Processor



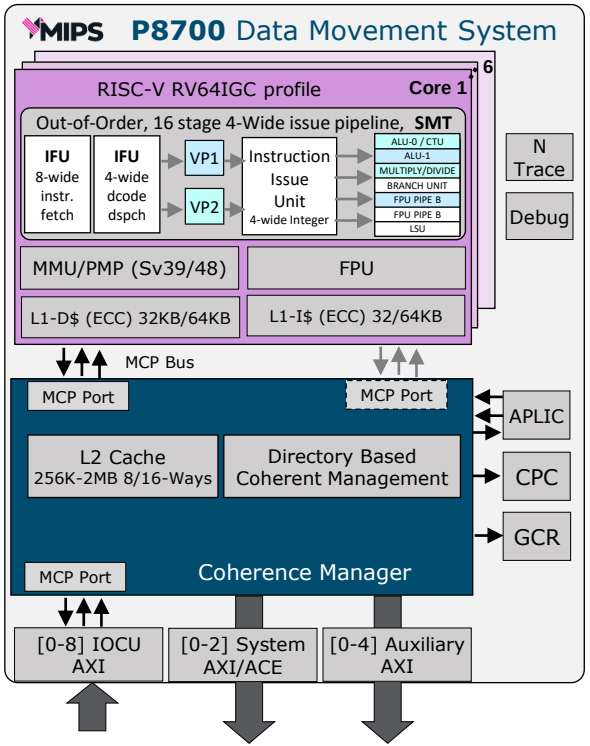
MIPS P8700 Core-Level Features

- Four-issue, Out-of-Order, 16-stage deep pipeline
  - 8-wide instruction fetch with 4-wide issue
  - 4-wide decode/rename/dispatch/graduation
  - 128-entry Reorder Buffer (ROB)
  - 32 Integer and 32 Floating Point Architecture Registers
- Hardware OoO Multi-threading supports 1 or 2 Threads per-core (**VP1**, **VP2**)
- Programmable Memory Management Unit (MMU)
  - 48-bit virtual and physical addresses
  - Shared FTLB across all hardware threads (HART) in a CPU
- FPU (Floating Point Extension)
  - Single Precision FP (F)
  - Double Precision FP (F & D)
- L1 caches with ECC (Error Correction Code) protection
- L2 cache support, implemented as shared L2 in the Coherence Manager
- Load and store bonding support
- Unaligned load / store support in hardware



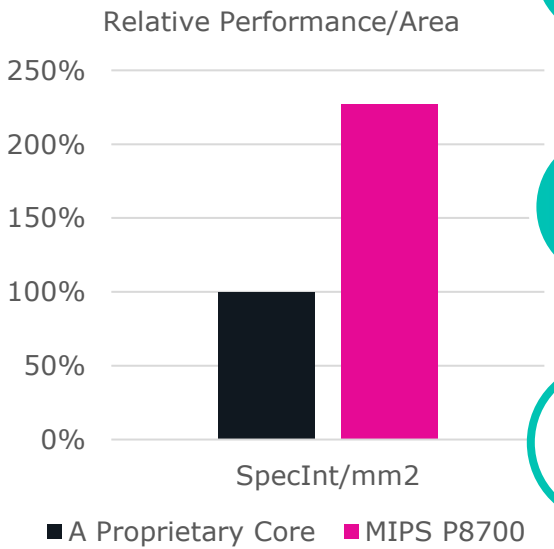
MIPS P8700 Single & Multi-Thread Issue

- A single thread (1T) can be issued from the same hardware thread (HART) and 2 threads (2T) from same or different harts
- Simultaneous Multi-Threading (SMT) with 2 Harts per core.
  - 1T can be issued from the same hart and 2T from the same or different harts
  - Multiple threads execute Floating-Point pipeline stage per cycle, or…
  - Superscalar execution on a single thread
  - Thread execution can switch dynamically per cycle
- 4 instruction issue per cycle with support to issue from both VPs on the same cycle
- 7 execution pipes :
  - 2x Integer Arithmetic and Logical Units (ALUs)
  - 1x Multiply / Divide Unit
  - 1x Branch Unit
  - 1x Load Store Unit
  - 1x Short Floating-Point Pipe
  - 1x Long Floating-Point Pipe



Boosting Data Movement with Multiple Execution Contexts in the Same Core

MIPS Simultaneous Multi-Threading of Out-of-Order Processors



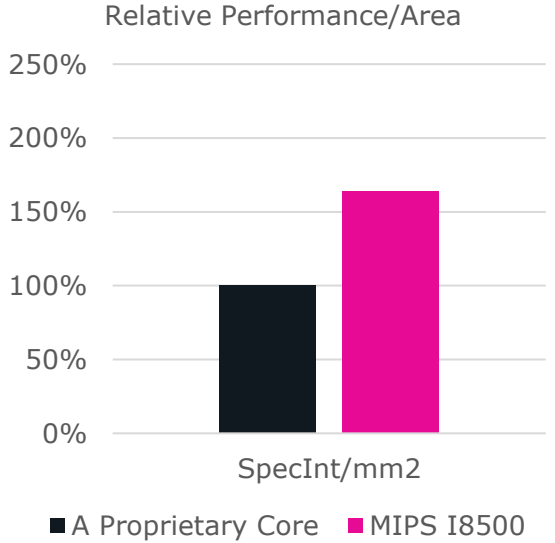
- Increased Compute Density
- Better Performance/$

- Quicker Responsiveness
- Higher Area Efficiency
- More Performance

- Open Specification ISA
- Easy Adoption
- Commercial & Open-Source S/W & Tools

Estimate by MIPS Engineering Team for MIPS P8700 (2T) vs A proprietary Core of SpecInt 2K6 per GHz, per mm², normalized for 2Ghz operation in TSMC N5. Higher is Better

MIPS Simultaneous Multi-Threading of In-Order Processors



Estimate by MIPS Engineering Team for MIPS I8500 (4T) vs A proprietary Core, of SpecInt 2K6 per GHz per mm², normalized for 2Ghz operation in TSMC N7. Higher is Better

MIPS Safety Package for P8700 & I8500

Achieve ISO 26262/ IEC 61508 Compliance

MIPS Safety Documents

Safety Requirement Specification [SRS]

- Details on Safety architecture, HW and SW safety mechanism as applied to the IP and recommended usage

Safety Plan [SP]

- Safety activities planning based on target project ASIL level and tailoring requirements

Functional safety Confirmation Measure Reports [CM]

- Safety related confirmation measures based on ASIL level independence
- Safety case confirmation reviews
- Functional safety Audits
- Functional safety assessment

Functional safety Analysis Report [FSA]

- Summary report of FMEDA analysis report based on equivalent [gate level] analysis
  at Part [IP] level

Safety Application Notes [SAN]

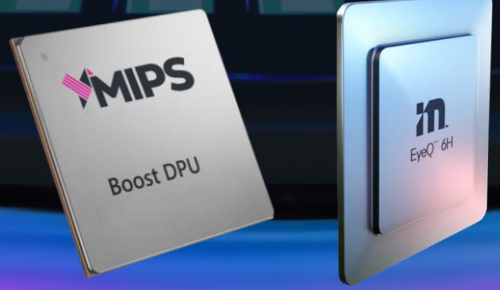
- Detailed description of all safety mechanism, its functionality and the protection offered, as implemented on the IP

MIPS Multi-Threaded Processing Systems Summary

Feature	I8500	P8700
Instruction Set Architecture (ISA)	RV64A/B23 + MIPS Extensions	RV64GC_Zba_Zbb + MIPS Extensions
Target Markets	Embedded, Data Center, Automotive Gateway, Industrial Gateway	Advanced Driver-Assistance Systems, Automotive Gateway
Instruction Pipeline	3-issue, In-Order, 9-Stage	4-issue, Out-of-Order, 16-Stage
Multi-Threaded Processing	SMT (Up to 4 threads per core)	SMT (Up to 2 threads per core)
Interrupts	AIA.w+m	AIA.w
IPC	✓✓	✓✓✓
Frequency	✓✓✓	✓✓✓
Area	✓✓	✓✓
Functional Safety	ASIL-B	ASIL-B
Cluster Coherence Manager	Yes	Yes
Level 2 Cluster Cache	Yes	Yes
Level 1 Scratchpads	Yes	No
Bus Interfaces	AXI, ACE, CHI, IOCU	AXI, ACE, IOCU
Debug and Trace	Ins. N-Trace, RISC-V Debug	Ins. N-Trace, RISC-V Debug

MIPS Is Driving Intelligence into Action

Success with leading cloud provider and automotive ADAS design wins



Built on industry standards to simplify adoption and drive technology forward with patented MIPS innovations for compute

MIPS Portfolio will enable autonomous platforms for the crucial Physical AI elements: Sense, Think, & Act

More at Embedded World 2025

Thank You